## IEEE P802.3da™/D2.0, 30th October 2024 1

(Amendment of IEEE Std 802.3™-2022 as amended by [list to be populated during publication process]) 2

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**IEEE P802.3da™/D2.0** 5

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**Draft Standard for Ethernet** 8

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**Amendment:** 10

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**Physical Layer Specifications and** 13

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**Management Parameters for** 15

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**Enhancement of 10 Mb/s Operation over** 17

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**Single Balanced Pair Multidrop Segments** 20

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Prepared by the 24

#### LAN/MAN Standards Committee 25

of the 26

#### IEEE Computer Society. 27

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This draft is an amendment of IEEE Std 802.3-2022 as amended by IEEE Std 802.3dd-2022, IEEE Std 29

802.3cs-2022, IEEE Std 802.3db-2022, IEEE Std 802.3ck-2022, IEEE Std 802.3de-2022, IEEE Std 30

802.3cx‐2023, IEEE Std 802.3cz‐2023, IEEE Std 802.3cy‐2023, and IEEE Std 802.3df‐2024. The purpose 31

of the amendment is to add Physical Layer (PHY) and management parameters for enhancement of 10 Mb/s 32

operation and optional provision of power over single balanced pair multidrop segments. Draft D2.0 is 33

prepared for Task Force review. This draft expires 6 months after the date of publication or when the next 34

version is published, whichever comes first. 35

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**Abstract:** This amendment to IEEE Std 802.3-2022 specifies additions and appropriate 1

modifications to the 10BASE-T1S Physical Layer (including reconciliation sublayers), 2

management parameters, Ethernet support for time synchronization protocols, and optional power 3

delivery to support multiple Powered Devices on the 10 Mb/s mixing segment. 4

**Keywords:** 10BASE-T1, 10BASE-T1S, 10BASE-T1M, copper, Ethernet, IEEE 802.3cg™, IEEE 5

802.3da™; Medium Dependent Interface, mixing segment, MPD, MPoE, MPSE, multidrop, 6

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Multidrop Power, Physical Coding Sublayer, physical layer, Physical Medium Attachment, PoDL, 8

PLCA, TCI 9

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**Introduction** 1

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**This introduction is not part of IEEE Std 802.3da-202x, IEEE Draft Standard for Ethernet. Amendment: Physical Layer Specifications and Management Parameters for Enhancement of 10 Mb/s Operation over Single Balanced Pair Multidrop Segments.**

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IEEE Std 802.3™ was first published in 1985. Since the initial publication, many projects have added 7

functionality or provided maintenance updates to the specifications and text included in the standard. Each 8

IEEE 802.3 project/amendment is identified with a suffix (e.g., IEEE Std 802.3ba™-2010). 9

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The half duplex Media Access Control (MAC) protocol specified in IEEE Std 802.3-1985 is Carrier Sense 11

Multiple Access with Collision Detection (CSMA/CD). This MAC protocol was key to the experimental 12

Ethernet developed at Xerox Palo Alto Research Center, which had a 2.94 Mb/s data rate. Ethernet at 13

10 Mb/s was jointly released as a public specification by Digital Equipment Corporation (DEC), Intel and 14

Xerox in 1980. “Local Area Networks: Carrier sense multiple access with collision detection (CSMA/CD) 15

access method and physical layer specifications” was approved as an IEEE standard by the IEEE Standards 16

Board in 1983 and subsequently published in 1985 as IEEE Std 802.3-1985. Since 1985, new media options, 17

new speeds of operation, and new capabilities have been added to IEEE Std 802.3. A full duplex MAC 18

protocol and the ability to use an EtherType to specify the MAC client protocol were added in 1997. The 19

title was changed to Standard for Ethernet with the 2012 Revision. 20

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Some of the major additions to IEEE Std 802.3 are identified in the marketplace with their project number. 22

This is most common for projects adding higher speeds of operation or new protocols. For example, 23

IEEE Std 802.3u™ added 100 Mb/s operation (also called Fast Ethernet), IEEE Std 802.3z™ added 24

1000 Mb/s operation (also called Gigabit Ethernet), IEEE Std 802.3ae™ added 10 Gb/s operation (also 25

called 10 Gigabit Ethernet), IEEE Std 802.3ah™ specified access network Ethernet (also called Ethernet in 26

the First Mile) and IEEE Std 802.3ba added 40 Gb/s operation (also called 40 Gigabit Ethernet) and 27

100 Gb/s operation (also called 100 Gigabit Ethernet). These major additions are all now included in and are 28

superseded by IEEE Std 802.3-2022 and are not maintained as separate documents. 29

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At the date of IEEE Std 802.3da-20xx publication, IEEE Std 802.3 was composed of the following 32

documents: 33

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IEEE Std 802.3-2022 35

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Section One—Includes Clause 1 through Clause 20 and Annex A through Annex K and Annex 4A. 37

Section One includes the specifications for 10 Mb/s operation and the MAC, frame formats and service 38

interfaces used for all speeds of operation. 39

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Section Two—Includes Clause 21 through Clause 33 and Annex 22A through Annex 33A. Section 41

Two includes management attributes for multiple protocols and speed of operation as well as 42

specifications for providing power over twisted pair cabling for multiple operational speeds. It also 43

includes general information on 100 Mb/s operation as well as most of the 100 Mb/s Physical Layer 44

specifications. 45

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Section Three—Includes Clause 34 through Clause 43 and Annex 36A through Annex 43C. Section 47

Three includes general information on 1000 Mb/s operation as well as most of the 1000 Mb/s Physical 48

Layer specifications. 49

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Section Four—Includes Clause 44 through Clause 55 and Annex 44A through Annex 55B. Section 51

Four includes general information on 10 Gb/s operation as well as most of the 10 Gb/s Physical Layer 52

specifications. 53

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Section Five—Includes Clause 56 through Clause 77 and Annex 57A through Annex 76A. Clause 56 1

through Clause 67 and Clause 75 through Clause 77, as well as associated annexes, specify subscriber 2

access and other Physical Layers and sublayers for operation from 512 kb/s to 10 Gb/s, and defines 3

services and protocol elements that enable the exchange of IEEE Std 802.3 format frames between 4

stations in a subscriber access network. Clause 68 specifies a 10 Gb/s Physical Layer specification. 5

Clause 69 through Clause 74 and associated annexes specify Ethernet operation over electrical 6

backplanes at speeds of 1000 Mb/s and 10 Gb/s. 7

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Section Six—Includes Clause 78 through Clause 95 and Annex 83A through Annex 93C. Clause 78 9

specifies Energy-Efficient Ethernet. Clause 79 specifies IEEE 802.3 Organizationally Specific Link 10

Layer Discovery Protocol (LLDP) type, length, and value (TLV) information elements. Clause 80 11

through Clause 95 and associated annexes include general information on 40 Gb/s and 100 Gb/s 12

operation as well as 40 Gb/s and 100 Gb/s Physical Layer specifications. Clause 90 specifies Ethernet 13

support for time synchronization protocols. 14

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Section Seven—Includes Clause 96 through Clause 115 and Annex 97A through Annex 115A. 16

Clause 96 through Clause 98, Clause 104, and associated annexes, specify Physical Layers and 17

optional features for 100 Mb/s and 1000 Mb/s operation over a single twisted pair. Clause 100 through 18

Clause 103, as well as associated annexes, specify Physical Layers for the operation of the EPON 19

protocol over coaxial distribution networks. Clause 105 through Clause 114 and associated annexes 20

include general information on 25 Gb/s operation as well as 25 Gb/s Physical Layer specifications. 21

Clause 99 specifies a MAC merge sublayer for the interspersing of express traffic. Clause 115 and its 22

associated annex specify a Physical Layer for 1000 Mb/s operation over plastic optical fiber. 23

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Section Eight—Includes Clause 116 through Clause 140 and Annex 119A through Annex 136D. 25

Clause 116 through Clause 124 and associated annexes include general information on 200 Gb/s and 26

400 Gb/s operation as well as 200 Gb/s and 400 Gb/s Physical Layer specifications. Clause 125 27

includes general information on 2.5 Gb/s and 5 Gb/s operation. Clause 126 through Clause 130 and 28

associated annexes include 2.5 Gb/s and 5 Gb/s Physical Layer specifications. Clause 131 provides 29

general information on 50 Gb/s operation. Clause 132 through Clause 140 and associated annexes 30

include 50 Gb/s Physical Layer specifications and additional 100 Gb/s, 200 Gb/s, and 400 Gb/s 31

Physical Layer specifications. 32

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Section Nine—Includes Clause 141 through Clause 160 and Annex 142A through Annex 154A. 34

Clause 141 through Clause 144 and associated annexes specify symmetric and asymmetric operation of 35

Ethernet passive optical networks over multiple 25 Gb/s channels. Clause 145 and associated annexes 36

specify increased power delivery using all four pairs in the structured wiring plant. Clause 146 through 37

Clause 149 and associated annexes specify Physical Layers for 10 Mb/s, 2.5 Gb/s, 5 Gb/s, and 10 Gb/s 38

operation over a single balanced pair of conductors. Clause 150 and Clause 151 include additional 39

400 Gb/s Physical Layer specifications. Clause 153 and Clause 154 specify 100 Gb/s operation over 40

DWDM channels. Clause 157 through Clause 160 include 10 Gb/s, 25 Gb/s, and 50 Gb/s bidirectional 41

Physical Layer specifications. 42

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IEEE Std 802.3dd™-2022 44

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Amendment 1—This amendment includes editorial and technical corrections, refinements, and 46

clarifications to Clause 104, Power over Data Lines of Single Pair Ethernet, and related portions of the 47

standard. 48

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IEEE Std 802.3cs™-2022 50

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Amendment 2—This amendment to IEEE Std 802.3-2022 defines Super-PON optical subscriber 52

access networks, in the family of Ethernet passive optical networks (EPONs). Super-PON has a reach 53

of up to 50 km and up to 1024 ONUs over a point-to-multipoint passive optical distribution network 54

(ODN) through wavelength division multiplexing (WDM). A Super-PON ODN contains a passive 1

wavelength router that determines the channels used by the ODN. This standard specifies the Super- 2

PON Reconciliation Sublayer (RS), Physical Coding Sublayer (PCS), Physical Medium Attachment 3

(PMA) sublayer, and Physical Medium Dependent (PMD) sublayer at a MAC data rate of 10 Gb/s in 4

the downstream direction and of 10 Gb/s or 2.5 Gb/s in the upstream direction. 5

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IEEE Std 802.3db™-2022 7

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Amendment 3—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 167. This 9

amendment adds Physical Layer specifications and management parameters for 100 Gb/s, 200 Gb/s, 10

and 400 Gb/s over one, two, and four pairs of multimode fiber based on 100 Gb/s optical signaling. 11

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IEEE Std 802.3ck™-2022 13

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Amendment 4—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 161 15

through Clause 163, Annex 120F, Annex 120G, Annex 162A through Annex 162D, Annex 163A, and 16

Annex 163B. This amendment includes Physical Layer specifications and management parameters for 17

100 Gb/s, 200 Gb/s, and 400 Gb/s electrical interfaces based on 100 Gb/s signaling. 18

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IEEE Std 802.3de™-2022 20

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Amendment 5—This amendment includes changes to IEEE Std 802.3-2022 to add 10 Mb/s Single-Pair 22

Ethernet point-to-point PHYs to the PHYs supporting the MAC Merge function and the Time 23

Synchronization Service Interface (TSSI). 24

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IEEE Std 802.3cx™-2023 26

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Amendment 6—This amendment to IEEE Std 802.3-2022 modifies Clause 30, Clause 45, and 28

Clause 90, and adds Annex 90A to enhance support for time synchronization protocols by providing 29

options for sub-nanosecond reporting of the transmit and receive path data delays, selection of the data 30

delay measurement point, and dynamic reporting of path data delay variation. 31

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IEEE Std 802.3cz™-2023 33

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Amendment 7—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 166. This 35

amendment adds 2.5 Gb/s, 5 Gb/s, 10 Gb/s, 25 Gb/s, and 50 Gb/s Physical Layer specifications and 36

management parameters for optical automotive Ethernet using graded-index glass optical fiber. 37

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IEEE Std 802.3cy™-2023 39

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Amendment 8—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 165 and 41

Annex 165A. This amendment adds Physical Layer specifications and management parameters for 42

operation at 25 Gb/s over a single balanced pair of conductors. 43

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IEEE Std 802.3df™-2024 45

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Amendment 9—This amendment includes changes to IEEE Std 802.3-2022 and adds Clause 169 47

through Clause 173, Annex 172A, and Annex 173A. This amendment includes Physical Layer 48

specifications and management parameters for 400 Gb/s and 800 Gb/s operation. 49

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IEEE Std 802.3da™-20xx 51

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Amendment X- This amendment includes changes to IEEE Std 802.3-2022 and adds [Clause 188](#_bookmark166) 53

through [Clause 189](#_bookmark299). This amendment adds Physical Layer specifications and management parameters 54

for enhancement of multidrop 10 Mb/s operation based on the 10BASE-T1S PHY specified in 1

Clause 147 of IEEE Std 802.3-2022, and specifies optional provision of power over single balanced 2

pair mixing segments. Additionally, this amendment includes additions and changes to Clause 148 to 3

automatically allocate node IDs (Dynamic PLCA). 4

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Two companion documents exist, IEEE Std 802.3.1 and IEEE Std 802.3.2. IEEE Std 802.3.1 describes 6

Ethernet management information base (MIB) modules for use with the Simple Network Management 7

Protocol (SNMP). IEEE Std 802.3.2 describes YANG data models for Ethernet. IEEE Std 802.3.1 and 8

IEEE Std 802.3.2 are updated to add management capability for enhancements to IEEE Std 802.3 after 9

approval of those enhancements. 10

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IEEE Std 802.3 will continue to evolve. New Ethernet capabilities are anticipated to be added within the 12

next few years as amendments to this standard. 13

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**Draft Standard for Ethernet** 1

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**Amendment X:** 3

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5

**Physical Layer Specifications and** 6

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**Management Parameters for** 8

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**Enhancement of 10 Mb/s Operation over** 10

11

12

**Single Balanced Pair Multidrop Segments** 13

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21

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##### <http://standards.ieee.org/IPR/disclaimers.html>. 26

27

NOTE—The editing instructions contained in this amendment define how to merge the material contained 28

therein into the existing base standard and its amendments to form the comprehensive standard. 29

30

The editing instructions are shown in ***bold italic***. Four editing instructions are used: change, delete, insert, 31

and replace. ***Change*** is used to make corrections in existing text or tables. The editing instruction specifies 32

the location of the change and describes what is being changed by using ~~strikethrough~~ (to remove old 33

material) and underscore (to add new material). ***Delete*** removes existing material. ***Insert*** adds new material 34

without disturbing the existing material. Deletions and insertions may require renumbering. If so, 35

renumbering instructions are given in the editing instruction. ***Replace*** is used to make changes in figures or 36

equations by removing the existing figure or equation and replacing it with a new one. Editing instructions, 37

change markings, and this NOTE will not be carried over into future editions because the changes will be 38

incorporated into the base standard. 39

40

Cross references that refer to clauses, tables, equations, or figures not covered by this amendment are 41

highlighted in green. 42

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44

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*TO BE REMOVED PRIOR TO FINAL PUBLICATION: Reviewers and the publication editor should note that editing instructions have been written to minimize the probability of changes being lost at publication from other IEEE 802.3 amendment projects running in parallel that modified the same text and tables.*

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**1. Introduction** 1

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## 1.4 Definitions 4

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##### Insert the following new definition after 1.4.63 10BASE-T1L: 6

7

**1.4.63a 10BASE-T1M:** IEEE 802.3 Physical Layer specification for a 10 Mb/s Ethernet local area network 8

using a single balanced pair of conductors as a shared medium. (See IEEE Std 802.3, [Clause](#_bookmark166) 188.) 9

10

##### Insert the following new definitions after 1.4.427 Multi-Channel Reconciliation Sublayer (MCRS): 11

12

**1.4.427a Multidrop Powered Device (MPD):** A device that is either drawing power or requesting power 13

from an MPSE (see IEEE Std 802.3, [Clause](#_bookmark299) 189). 14

15

**1.4.427b Multidrop Power Interface (MPI):** The mechanical and electrical interface between the 16

Multidrop Power Sourcing Equipment (MPSE) or Multidrop Powered Device (MPD) and the transmission 17

medium. 18

19

**1.4.427c Multidrop Power Sourcing Equipment (MPSE):** A device that provides power to a mixing 20

segment which may also carry data (see IEEE Std 802.3, [Clause 1](#_bookmark299)89). 21

22

##### Change 1.4.433 as follows: 23

24

**1.4.433** network interface device (NID): A device that contains an MDI, MPI, or a PI. 25

26

##### Insert the following new definition after 1.4.582 trunk cable: 27

28

**1.4.582a Trunk Connection Interface (TCI):** an MDI for shared transmission medium for single pair 29

Ethernet. 30

31

## 1.5 Abbreviations 32

33

##### Insert the following new abbreviations into the list, in alphanumeric order: 34

35

MPD MPoE Powered Device 36

MPI Multidrop Power Interface 37

MPSE MPoE Power Sourcing Equipment 38

MPoE Multidrop Power over Ethernet 39

TCI Trunk Connection Interface 40

TPS Transmit Power Signature 41

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**22.** **Reconciliation Sublayer (RS) and Media Independent Interface (MII)** 1

2

3

## 22.1 Overview 4

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##### Change Figure 22-1 as follows (see changes at the bottom of the right column):. 6

LAN 7

OSI REFERENCE MODEL LAYERS

CSMA/CD 8

LAYERS 9

HIGHER LAYERS 10

11



|  |
| --- |
| APPLICATION |
| PRESENTATION |
| SESSION |
| TRANSPORT |
| NETWORK |
| DATA LINK |
| PHYSICAL |

LLC (LOGICAL LINK CONTROL) OR OTHER MAC CLIENT 12

13

MAC CONTROL (OPTIONAL) 14

MAC—MEDIA ACCESS CONTROL 15

16

MAU

RECONCILIATION

MII

PLS

AUI

PMA

MDI

MEDIUM

10 Mb/s

RECONCILIATION

MII/GMII

PCS PMA PMD

MDI

MEDIUM

10BASE-T1L,10BASE-T1M~~S~~,

10BASE-T1S, 100 Mb/s, 1 Gb/s

17

18

19

PHY 20

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25

AUI = ATTACHMENT UNIT INTERFACE

GMII = GIGABIT MEDIA INDEPENDENT INTERFACE MAU = MEDIUM ATTACHMENT UNIT

MDI = MEDIUM DEPENDENT INTERFACE

MII = MEDIA INDEPENDENT INTERFACE

PCS = PHYSICAL CODING SUBLAYER 26

PHY = PHYSICAL LAYER DEVICE 27

PLS = PHYSICAL LAYER SIGNALING 28

PMA = PHYSICAL MEDIUM ATTACHMENT 29

PMD = PHYSICAL MEDIUM DEPENDENT

30

NOTE – The MDI for 10BASE-T1M is referred to as the TCI (see [Clause 1](#_bookmark166)88). 31

32

33

#### Figure 22–1—MII relationship to the ISO/IEC Open Systems Interconnection (OSI) 34

#### reference model and the IEEE 802.3 CSMA/CD LAN model 35

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**30. Management** 1

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## 30.2 Managed objects 4

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#### 30.2.5 Capabilities 6

7

##### Insert new rows to the end of Table 30–11 as follows (unchanged rows not shown): 8

9

10

#### Table 30–11—PLCA capabilities 11

12

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  |  |  |  |  |
|  |  |  |  | PLCA capability (optional) |
|  | aDPLCASoftAgingCycles | ATTRIBUTE | GET-SET | **X** |
|  | aDPLCAHardAgingCyclesStatus | ATTRIBUTE | GET-SET | **X** |
|  | aDPLCACoordinatorRoleAllowed | ATTRIBUTE | GET-SET | **X** |
|  | aDPLCAWaitBeaconTimer | ATTRIBUTE | GET-SET |  |
|  | aDPLCAAdminState | ATTRIBUTE | GET | **X** |
|  | acDPLCAAdminControl | ACTION |  | **X** |
|  | aPLCASupported | ATTRIBUTE | GET | **X** |
|  | aDPLCASupported | ATTRIBUTE | GET | **X** |

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## Layer management for DTEs 34

35

#### PHY device managed object class 36

37

#### PHY device attributes 38

39

* + - * 1. **aPhyType** 40

41

##### Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.2 after the entry for 42

***“10BASE-T1L”:*** 43

44

10BASE-T1M [Clause 188](#_bookmark166) 10 Mb/s DME 45

46

#### aPhyTypeList 47

48

##### Insert the following new entry in the APPROPRIATE SYNTAX section of 30.3.2.1.3 after the entry for 49

***“10BASE-T1L”:*** 50

51

10BASE-T1M [Clause 188](#_bookmark166) 10 Mb/s DME 52

53

54

## 30.5 Layer management for medium attachment units (MAUs) 1

2

#### 30.5.1 MAU managed object class 3

4

#### 30.5.1.1 MAU attributes 5

6

#### 30.5.1.1.2 aMAUType 7

8

##### Insert the following new entry in the APPROPRIATE SYNTAX section of 30.5.1.1.2 after the entry for 9

##### “10BASE-T1L”: 10

11

10BASE-T1M Single balanced pair PHY as specified in [Clause 188](#_bookmark166) 12

13

14

## 30.6 Management for link Auto-Negotiation 15

16

#### 30.6.1 Auto-Negotiation managed object class 17

18

#### 30.6.1.1 Auto-Negotiation attributes 19

20

#### 30.6.1.1.5 aAutoNegLocalTechnologyAbility 21

22

##### Insert the following new entry in the APPROPRIATE SYNTAX section of 30.6.1.1.5 after the entry for 23

##### “10BASE-T1L”: 24

25

10BASE-T1M Single balanced pair PHY as specified in [Clause 188](#_bookmark166) 26

27

## Management for PLCA Reconciliation Sublayer 28

29

#### PLCA managed object class 30

31

#### PLCA attributes 32

33

#### aPLCANodeCount 34

35

##### Change text of BEHAVIOUR DEFINED AS section of 30.16.1.1.3 as shown: 36

37

This value is assigned to define the number of nodes getting a transmit opportunity before a new BEACON 38

is generated. When D-PLCA is enabled, writes to this attribute are ignored. This parameter maps to the 39

local\_nodeID variable in [148.4.4.2](#_bookmark138). Valid range is 0 to 255, inclusive. The default value is 8.; 40

41

#### aPLCALocalNodeID 42

43

##### Change text of BEHAVIOUR DEFINED AS section of 30.16.1.1.4 as shown: 44

45

This value is assigned to define the ID of the local node on the PLCA network. This parameter maps to the 46

plca\_node\_count variable in [148.4.4.2](#_bookmark138). When D-PLCA is enabled, writes to this attribute are ignored. The 47

default value is 255. Value range is 0 to 255, inclusive.; 48

49

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##### Insert new subclauses 30.16.1.1.8 through 30.16.1.1.14 after 30.16.1.1.7 as follows: 1

2

#### aDPLCASoftAgingCycles 3

4

ATTRIBUTE 5

APPROPRIATE SYNTAX: 6

INTEGER 7

8

BEHAVIOUR DEFINED AS: 9

Controls the aging time in BEACON cycles of D-PLCA SOFT claims as defined by the 10

soft\_aging\_cycles variable in [148.4.7.2](#_bookmark149).; 11

12

#### aDPLCAHardAgingCycles 13

14

ATTRIBUTE 15

APPROPRIATE SYNTAX: 16

INTEGER 17

18

BEHAVIOUR DEFINED AS: 19

Controls the aging time in BEACON cycles of D-PLCA HARD claims as defined by the 20

hard\_aging\_cycles variable in [148.4.7.2](#_bookmark149).; 21

22

#### aDPLCACoordinatorRoleAllowed 23

24

ATTRIBUTE 25

APPROPRIATE SYNTAX: 26

BOOLEAN 27

28

BEHAVIOUR DEFINED AS: 29

Controls whether the D-PLCA enabled node is allowed to take the coordinator role, mapping to 30

the coordinator\_role\_allowed variable defined in [148.4.7.2.;](#_bookmark149) 31

32

#### aDPLCAAdminState 33

34

ATTRIBUTE 35

APPROPRIATE SYNTAX: 36

An ENUMERATED VALUE that has the following entries: 37

disabled 38

enabled 39

40

BEHAVIOUR DEFINED AS: 41

A read-only value that indicates whether the dynamic node ID allocation method for the PLCA 42

Reconciliation Sublayer (D-PLCA) is enabled. When D-PLCA is enabled, PLCA node IDs are 43

dynamically assigned as defined in [148.4.7.;](#_bookmark146) 44

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#### aDPLCAWaitBeaconTimer 1

2

ATTRIBUTE 3

APPROPRIATE SYNTAX: 4

INTEGER 5

6

BEHAVIOUR DEFINED AS: 7

Controls the time the D-PLCA state diagram waits for a node to indicate BEACON as defined by 8

the wait\_beacon\_timer in [148.4.7.4](#_bookmark152) specified in bit times (BT). The default value is 40 BT. The 9

value of this attribute is preserved across reset, including loss of power.; 10

11

#### aPLCASupported 12

13

ATTRIBUTE 14

APPROPRIATE SYNTAX: 15

An ENUMERATED VALUE that has the following entries: 16

TRUE 17

FALSE 18

19

BEHAVIOUR DEFINED AS: 20

A read-only value that indicates whether PLCA is supported by this station.; 21

22

#### aDPLCASupported 23

24

ATTRIBUTE 25

APPROPRIATE SYNTAX: 26

An ENUMERATED VALUE that has the following entries: 27

TRUE 28

FALSE 29

30

BEHAVIOUR DEFINED AS: 31

A read-only value that indicates whether D-PLCA is supported by this station.; 32

33

#### 30.16.1.2 PLCA device actions 34

35

##### Insert new subclause 30.16.1.2.3 after 30.16.1.2.2 as follows: 36

37

#### 30.16.1.2.3 acDPLCAAdminControl 38

39

ACTION 40

APPROPRIATE SYNTAX: 41

An ENUMERATED VALUE that has the following entries: 42

disabled 43

enabled 44

45

BEHAVIOUR DEFINED AS: 46

This action provides a means to alter aDPLCAAdminState. Setting this controls the state of 47

D-PLCA (see [148.4.7)](#_bookmark146) by modifying the variable dplca\_en (see [148.](#_bookmark149)4.7.2).; 48

49

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##### Insert new subclause 30.17 after 30.16 (and its subclauses) as follows: 1

2

3

* 1. **Layer management for Multidrop Power over Ethernet (MPoE)** 4

5

#### MPSE managed object class 6

7

This subclause formally defines the behaviors for the oMPSE managed object class attributes and actions. 8

9

#### MPSE attributes 10

11

#### aMPSEAdminState 12

13

ATTRIBUTE 14

APPROPRIATE SYNTAX: 15

An ENUMERATED VALUE that has one of the following entries: 16

enabled MPSE functions enabled 17

disabled MPSE functions disabled 18

19

BEHAVIOUR DEFINED AS: 20

A read-only value that identifies the operational state of the MPSE function. This maps to the 21

mpse\_enable variable specified in [189.4.4.2.](#_bookmark321) 22

The operational state of the MPSE function can be changed using the acMPSEAdminControl 23

action.; 24

25

#### aMPSEPowerState 26

27

ATTRIBUTE 28

APPROPRIATE SYNTAX: 29

An ENUMERATED VALUE that has one of the following entries: 30

unknown MPSE true state unknown 31

offline MPSE offline 32

idle MPSE idle 33

discovery MPSE discovery 34

inrush MPSE inrush 35

powering MPSE powering 36

error MPSE error 37

backoff MPSE backoff 38

39

BEHAVIOUR DEFINED AS: 40

A read-only value that indicates the state of MPSE as specified in [189.4.4.5.;](#_bookmark326) 41

42

#### aMPSETypeDiscovery 43

44

ATTRIBUTE 45

APPROPRIATE SYNTAX: 46

An ENUMERATED VALUE that has one of the following entries: 47

type0 Type 0 MPD(s) 48

type1 Type 1 MPD(s) 49

types01 Both Type 0 and Type 1 MPD(s) 50

51

BEHAVIOUR DEFINED AS: 52

A read-only value that indicates the MPD Class(es) of the detected MPD(s) as specified in1[89.4.6.;](#_bookmark334) 53

54

#### aMPSEPoweringCounter 1

2

ATTRIBUTE 3

APPROPRIATE SYNTAX: 4

Generalized nonresettable counter. 5

6

BEHAVIOUR DEFINED AS: 7

This counter is incremented when the MPSE transitions to the POWER\_ON state in from the MPI 8

as specified in [Figure 189–4](#_bookmark328).; 9

10

#### aMPSEOverloadCounter 11

12

ATTRIBUTE 13

APPROPRIATE SYNTAX: 14

Generalized nonresettable counter. 15

16

BEHAVIOUR DEFINED AS: 17

This counter is incremented when the MPSE detects an overload condition as specified in [189.4.9.;](#_bookmark339) 18

19

#### aMPSEShortCircuitCounter 20

21

ATTRIBUTE 22

APPROPRIATE SYNTAX: 23

Generalized nonresettable counter. 24

25

BEHAVIOUR DEFINED AS: 26

This counter is incremented when the MPSE detects a short circuit condition as specified in 27

[189.4.1](#_bookmark340)0.; 28

29

#### aMPSEActualPower 30

31

ATTRIBUTE 32

APPROPRIATE SYNTAX: 33

INTEGER 34

35

BEHAVIOUR DEFINED AS: 36

An integer value indicating present (actual) power being supplied by the MPSE as measured at the 37

MPI in milliwatts. The behavior is undefined if the state of aMPSEPowerState is anything other 38

than powering. The sampling frequency and averaging is vendor-defined.; 39

40

#### aMPSEPowerAccuracy 41

42

ATTRIBUTE 43

APPROPRIATE SYNTAX: 44

INTEGER 45

46

BEHAVIOUR DEFINED AS: 47

An integer value indicating the accuracy associated with aMPSEActualPower in ± milliwatts.; 48

49

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#### aMPSECumulativeEnergy 1

2

ATTRIBUTE 3

APPROPRIATE SYNTAX: 4

Generalized nonresettable counter. 5

6

BEHAVIOUR DEFINED AS: 7

A count of the cumulative energy supplied by the MPSE as measured at the MDI in kilojoules.; 8

#### 30.17.1.2 MPSE actions 9

10

#### 30.17.1.2.1 acMPSEAdminControl 11

12

ACTION 13

14

APPROPRIATES YNTAX: 15

Same as aMPSEAdminState 16

BEHAVIOUR DEFINED AS: 17

This action provides a means to alter [189.4.4.2](#_bookmark321) mpse\_enable.; 18

19

#### MPD managed object class 20

21

This subclause formally defines the behaviors for the oMPD managed object class attributes and actions. 22

23

#### MPD attributes 24

25

* + - * 1. **aMPDType** 26

27

ATTRIBUTE 28

29

APPROPRIATE SYNTAX: 30

An ENUMERATED VALUE that has one of the following entries: 31

type0 Type 0 only MPD 32

type1 Type 1 only MPD 33

types01 Type 0 and Type 1 MPD 34

BEHAVIOUR DEFINED AS: 35

A read-only value that indicates the MPD Type as specified in [189.3](#_bookmark311).; 36

37

#### aMPDAdminState 38

39

ATTRIBUTE 40

41

APPROPRIATE SYNTAX: 42

An ENUMERATED VALUE that has one of the following entries: 43

enabled MPD functions enabled 44

disabled MPD functions disabled 45

BEHAVIOUR DEFINED AS: 46

A read-only value that identifies the operational state of the MPD functions. An interface which 47

can provide the MPD functions specified in [Clause 189](#_bookmark299) will be enabled to do so when this attribute 48

has the enumeration “enabled”. When this attribute has the enumeration “disabled” the interface 49

will act as it would if it had no MPD function. This attribute reports disabled when in the OFFLINE 50

state in [189.5.3.5](#_bookmark355) and enabled otherwise. 51

The operational state of the MPD function can be changed using the acMPDAdminControl action.; 52

53

54

#### aMPDPowerState 1

2

ATTRIBUTE 3

APPROPRIATE SYNTAX: 4

An ENUMERATED VALUE that has one of the following entries: 5

unknown true state unknown 6

offline MPD offline 7

idle MPD idle 8

discovery MPD discovery 9

powered MPD powered 10

11

BEHAVIOUR DEFINED AS: 12

A read-only value that indicates the state of MPD state diagram specified in [189.5.3.5.;](#_bookmark355) 13

14

#### aMPDDiscoveryCounter 15

16

ATTRIBUTE 17

APPROPRIATE SYNTAX: 18

Generalized nonresettable counter. 19

20

BEHAVIOUR DEFINED AS: 21

This counter is incremented when the MPD enters the DO\_MARK1 state in [Figure 18](#_bookmark358)9–8.; 22

23

#### aMPDMismatchCounter 24

25

ATTRIBUTE 26

APPROPRIATE SYNTAX: 27

Generalized nonresettable counter. 28

29

BEHAVIOUR DEFINED AS: 30

This counter is incremented when the MPD enters the PON\_MISMATCHED\_TYPE state in 31

[Figure 189–](#_bookmark358)8.; 32

33

#### aMPDPoweredCounter 34

35

ATTRIBUTE 36

APPROPRIATE SYNTAX: 37

Generalized nonresettable counter. 38

39

BEHAVIOUR DEFINED AS: 40

This counter is incremented when the MPD enters the PON\_LOAD\_ON state in [Figure 18](#_bookmark358)9–8.; 41

42

#### aMPDNoPowerCounter 43

44

ATTRIBUTE 45

46

APPROPRIATE SYNTAX: 47

Generalized nonresettable counter. 48

BEHAVIOUR DEFINED AS: 49

50

This counter is incremented when the MPD enters the PON\_NO\_POWER state in [Figure 189–](#_bookmark358)8.; 51

52

53

54

#### aMPDActualPower 1

2

ATTRIBUTE 3

APPROPRIATE SYNTAX: 4

INTEGER 5

6

BEHAVIOUR DEFINED AS: 7

An integer value indicating present (actual) power being supplied to the MPD as measured at the 8

MPI in milliwatts. It reports the value 0 if the value of aMPDPowerState is not powered. The 9

sampling frequency and averaging is vendor-defined.; 10

11

#### aMPDPowerAccuracy 12

13

ATTRIBUTE 14

APPROPRIATE SYNTAX: 15

INTEGER 16

17

BEHAVIOUR DEFINED AS: 18

An integer value indicating the accuracy associated with aMPDActualPower in ± milliwatts.; 19

20

#### aMPDCumulativeEnergy 21

22

ATTRIBUTE 23

APPROPRIATE SYNTAX: 24

Generalized nonresettable counter. 25

26

BEHAVIOUR DEFINED AS: 27

A count of the cumulative energy supplied to the MPD as measured at the MDI in kilojoules.; 28

#### 30.17.2.2 MPD actions 29

30

#### 30.17.2.2.1 acMPDAdminControl 31

32

ACTION 33

34

APPROPRIATE SYNTAX: 35

Same as aMPDAdminState 36

BEHAVIOUR DEFINED AS: 37

This action provides a means to alter [189.5.3.3](#_bookmark351) mpd\_reset and dte\_power\_required. A “disabled” 38

to “enabled” transition sets mpd\_reset to FALSE and dte\_power\_required to TRUE. An “enabled” 39

to “disabled” transition sets mpd\_reset to TRUE and dte\_power\_required to FALSE.; 40

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**45.** **Management Data Input/Output (MDIO) Interface** 1

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## 45.2 MDIO Interface Registers 4

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#### 45.2.1 PMA/PMD registers 6

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##### Change the rows for 1.2297, 1.2298, and 1.229 in [Table 45–3](#_bookmark76) as follows (unchanged rows not shown): 8

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#### Table 45–3—PMA/PMD registers 10

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|  |  |  |
| --- | --- | --- |
| **Register address** | **Register name** | **Subclause** |
| … | | |
| 1.2297 | 10BASE-T1M / 10BASE-T1S PMA control | [45.2.1.234](#_bookmark82) |
| 1.2298 | 10BASE-T1M / 10BASE-T1S PMA status | [45.2.1.235](#_bookmark89) |
| 1.2299 | 10BASE-T1M / 10BASE-T1S test mode control | [45.2.1.236](#_bookmark97) |
| … | | |

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#### 45.2.1.16 BASE-T1 PMA/PMD extended ability register (1.18) 22

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##### Change the row for bits 1.18.15:8 in [Table 45–19](#_bookmark78) (as modified by IEEE Std 802.3cy-2023) and insert a 24

***new row below it as follows (unchanged rows not shown):*** 25

26

27

#### Table 45–19—BASE-T1 PMA/PMD extended ability register bit definitions 28

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|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Name** | **Description** | **R/Wa** |
| ~~1~~.18.15:89 | Reserved | Value always 0 | RO |
| 1.18.8 | 10BASE-T1M ability | 1 = PMA/PMD is able to perform 10BASE-T1M  0 = PMA/PMD is not able to perform 10BASE-T1M | RO |
| … | | | |

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aRO = Read only 36

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#### 45.2.1.214 BASE-T1 PMA/PMD control register (Register 1.2100) 1

2

##### Change [Table 45–178](#_bookmark80) (as modified by IEEE Std 802.3cy-2023) as follows (unchanged rows not shown): 3

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#### Table 45–178—BASE-T1 PMA/PMD control register bit definitions 6

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|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Name** | **Description** | **R/Wa** |
| … | | | |
| 1.2100.3:0 | Type Selection | 3 2 1 0  Other values reserved ~~1 x x x = Reserved~~  1 0 0 0 = 10BASE-T1M  0 1 1 1 = 25GBASE-T1  0 1 1 0 = 10GBASE-T1  0 1 0 1 = 5GBASE-T1  0 1 0 0 = 2.5GBASE-T1  0 0 1 1 = 10BASE-T1S  0 0 1 0 = 10BASE-T1L  0 0 0 1 = 1000BASE-T1  0 0 0 0 = 100BASE-T1 | R/W |

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aRO = Read only, R/W = Read/Write 21

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##### Change 45.2.1.214.2 (as modified by IEEE Std 802.3cy-2023) as follows: 24

25

#### 45.2.1.214.2 Type selection (1.2100.3:0) 26

27

Bits 1.2100.3:0 are used to set the mode of operation when Auto-Negotiation enable bit 7.512.12 is set to 28

zero, or if Auto-Negotiation is not implemented. ~~When these bits are set to 0000, the mode of operation is~~ 29

~~100BASE-T1. When these bits are set to 0001, the mode of operation is 1000BASE-T1. When these bits are~~ 30

~~set to 0010, the mode of operation is 10BASE-T1L. When these bits are set to 0011, the mode of operation is~~ 31

~~10BASE-T1S. When these bits are set to 0100, the mode of operation is 2.5GBASE-T1. When these bits are~~ 32

~~set to 0101, the mode of operation is 5GBASE-T1. When these bits are set to 0110, the mode of operation is~~ 33

~~10GBASE-T1. When these bits are set to 0111, the mode of operation is 25GBASE-T1.~~ These bits shall be 34

ignored when the Auto-Negotiation enable bit 7.512.12 is set to one. See description in [Table 45–178](#_bookmark80) for the 35

mapping of bits. 36

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##### Change 45.2.1.234 and the title of Table 45-196 (unchanged rows not shown) as follows: 1

2

#### 45.2.1.234 10BASE-T1M / 10BASE-T1S PMA control register (Register 1.2297) 3

4

The assignment of bits in the 10BASE-T1M / 10BASE-T1S PMA control register is shown in 5

[Table 45–19](#_bookmark83)6. 6

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8

#### Table 45–196—10BASE-T1M / 10BASE-T1S PMA control register bit definitions 9

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|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Name** | **Description** | **R/Wa** |
| … | | | |

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aRO = Read only, R/W = Read/Write, SC = Self-clearing 14

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##### Change 45.2.234.1 as follows: 17

18

#### 45.2.1.234.1 PMA reset (1.2297.15) 19

20

Resetting the 10BASE-T1M / 10BASE-T1S PMA is accomplished by setting bit 1.2297.15 to one. This 21

action shall set all the~~10BASE-T1S~~ PMA registers to their default states. As a consequence, this action may 22

change the internal state of the ~~10BASE-T1S~~ PMA and the state of the physical link. This action may also 23

initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 24

~~10BASE-T1S~~ PMA shall return a value of one in bit 1.2297.15 when a reset is in progress; otherwise, it shall 25

return a value of zero. The ~~10BASE-T1S~~ PMA is not required to accept a write transaction to any of its 26

registers until the reset process is completed. The control and management interface shall be restored to 27

operation within 0.5 s from the setting of bit 1.2297.15. 28

29

During a reset, the ~~10BASE-T1S~~ PMA shall respond to reads from bits 1.2297.15, 1.8.15:14, and 1.0.15. All 30

other register bits should be ignored. 31

32

NOTE—This operation may interrupt communication. 33

34

Bit 1.2297.15 is a copy of 1.0.15, and setting or clearing either bit shall set or clear the other bit. Setting 35

either bit shall reset the ~~10BASE-T1S~~ PMA. 36

37

##### Change 45.2.1.234.3 as follows: 38

39

#### 45.2.1.234.3 Low-power (1.2297.11) 40

41

When the low-power ability is supported, the 10BASE-T1M / 10BASE-T1S PMA may be placed into a low- 42

power mode by setting bit 1.2297.11 to one. This action may also initiate a low-power mode in any other 43

MMDs that are instantiated in the same package. The low-power mode is exited by resetting the ~~10BASE-~~ 44

~~T1S~~PMA. The behavior of the ~~10BASE-T1S~~ PMA in transition to and from the low-power mode is 45

implementation specific, and any interface signals should not be relied upon. While in the low-power mode, 46

the device shall respond to management transactions necessary to exit the low-power mode. The default 47

value of bit 1.2297.11 is zero. 48

49

NOTE—The time from low-power mode to full operation is implementation specific. 50

51

Bit 1.2297.11 is a copy of bit 1.0.11, and setting or clearing either bit shall set or clear the other bit. Setting 52

either bit shall put the ~~10BASE-T1S~~ PMA in low-power mode. 53

54

#### 45.2.1.234.4 Multidrop mode (1.2297.10) 1

2

##### Insert a new paragraph at the end of 45.2.1.234.4 as follows: 3

4

For 10BASE-T1M, this bit is always set to 1 and writing to bit 1.2297.10 shall have no effect. 5

6

##### Change 45.2.1.234.5 as follows: 7

8

#### 45.2.1.234.5 Loopback (1.2297.0) 9

10

The 10BASE-T1M / 10BASE-T1S PMA shall be placed in loopback mode of operation when loopback bit 11

1.2297.0 is set to one. When in loopback mode, the ~~10BASE-T1S~~ PMA shall accept data on the transmit 12

path and return it on the receive path. The default value of bit 1.2297.0 is zero. Bit 1.2297.0 is a copy of 13

1.0.0, and setting or clearing either bit shall set or clear the other bit. Setting either bit shall enable loopback. 14

15

##### Change 45.2.1.235 and the title of Table 45-197 (unchanged rows not shown) as follows: 16

17

#### 10BASE-T1M / 10BASE-T1S PMA status register (Register 1.2298) 18

19

The assignment of bits in the 10BASE-T1M / 10BASE-T1S PMA status register is shown in [Table 45–197.](#_bookmark90) 20

21

22

#### Table 45–197—10BASE-T1M / 10BASE-T1S PMA status register bit definitions 23

24

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Name** | **Description** | **R/Wa** |
| … | | | |

25

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27

aRO = Read only, LH = Latching high 28

29

30

##### Change 45.2.1.235.1 as follows: 31

32

#### 10BASE-T1M / 10BASE-T1S loopback ability (1.2298.13) 33

34

When read as a one, this bit indicates that the 10BASE-T1M / 10BASE-T1S PHY supports PMA loopback. 35

When read as a zero, this bit indicates that the ~~10BASE-T1S~~ PHY does not support PMA loopback. 36

37

##### Change 45.2.1.235.2 as follows: 38

39

#### Low-power ability (1.2298.11) 40

41

When read as a one, bit 1.2298.11 indicates that the 10BASE-T1M / 10BASE-T1S PMA supports the low- 42

power ability. When read as a zero, bit 1.2298.11 indicates that the ~~10BASE-T1S~~ PMA does not support the 43

low-power feature. If the ~~10BASE-T1S~~ PMA supports the low-power feature, then it is controlled using 44

either bit 1.2297.11 or bit 1.0.11. 45

46

#### Multidrop ability (1.2298.10) 47

48

##### Insert a new paragraph at the end of 45.2.1.235.3 as follows: 49

50

For 10BASE-T1M, this bit is always set to 1 and writing to bit 1.2297.10 shall have no effect. 51

52

53

54

##### Change 45.2.1.235.4 as follows: 1

2

#### Receive fault ability (1.2298.9) 3

4

When read as a one, bit 1.2298.9 indicates that the 10BASE-T1M / 10BASE-T1S PMA has the ability to 5

detect a fault condition on the receive path. When read as a zero, bit 1.2298.9 indicates that the ~~10BASE-~~ 6

~~T1S~~ PMA does not have the ability to detect a fault condition on the receive path. 7

8

##### Change 45.2.1.235.5 as follows: 9

10

#### 45.2.1.235.5 Receive fault (1.2298.1) 11

12

When read as a one, bit 1.2298.1 indicates that the 10BASE-T1M / 10BASE-T1S PMA has detected a fault 13

condition on the receive path. When read as a zero, bit 1.2298.1 indicates that the ~~10BASE-T1S~~ PMA has 14

not detected a fault condition on the receive path. Detection of a fault condition on the receive path is 15

optional, and the ability to detect such a condition is advertised by bit 1.2298.9. The ~~10BASE-T1S~~ PMA that 16

is unable to detect a fault condition on the receive path shall return a value of zero for this bit. This bit shall 17

be implemented with latching high behavior. 18

19

##### Change 45.2.1.236 and the title of Table 45-198 (unchanged rows not shown) as follows: 20

21

#### 45.2.1.236 10BASE-T1M / 10BASET1S test mode control register (Register 1.2299) 22

23

The assignment of bits in the 10BASE-T1M / 10BASE-T1S test mode control register is shown in 24

[Table 45–198.](#_bookmark98) The default values for each bit should be chosen so that the initial state of the device upon 25

power up or reset is a normal operational state without management intervention. 26

27

28

#### Table 45–198—10BASE-T1M / BASE-T1S test mode control register bit definitions 29

30

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Name** | **Description** | **R/Wa** |
| … | | | |

31

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aRO = Read only, R/W = Read/Write 34

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36

#### PCS registers 37

38

##### Change the rows for 3.2291, 3.2292, 3.2293, and 3.2294 in [Table 45–233](#_bookmark100) as follows (unchanged rows not 39

***shown):*** 40

41

#### Table 45–233—PCS registers 42

43

44

|  |  |  |
| --- | --- | --- |
| **Register address** | **Register name** | **Subclause** |
| … | | |
| 3.2291 | 10BASE-T1M /10BASE=T1S PCS control | [45.2.3.72](#_bookmark101) |
| 3.2292 | 10BASE-T1M /10BASE=T1S PCS status | [45.2.3.73](#_bookmark108) |
| 3.2293 | 10BASE-T1M /10BASE=T1S PCS diagnostic 1 | [45.2.3.74](#_bookmark112) |
| 3.2294 | 10BASE-T1M /10BASE=T1S PCS diagnostic 1 | [45.2.3.75](#_bookmark114) |
| … | | |

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##### Change 45.2.3.72 and the title of [Table 45–298](#_bookmark102) (unchanged rows not shown) as follows: 1

2

#### 10BASE-T1M / 10BASE-T1S PCS control register (Register 3.2291) 3

4

The assignment of bits in the 10BASE-T1M / 10BASE-T1S PCS control register is shown in [Table 45–298.](#_bookmark102) 5

The default value for each bit of the ~~10BASE-T1S~~ PCS control register should be chosen so that the initial 6

state of the device upon power up or reset is a normal operational state without management intervention. 7

8

9

#### Table 45–298—10BASE-T1M / 10BASE-T1S PCS control register bit definitions 10

11

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Name** | **Description** | **R/Wa** |
| … | | | |

12

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14

aRO = Read only, R/W = Read/Write, SC = Self-clearing 15

16

17

##### Change 45.2.3.72.1 as follows: 18

19

#### 45.2.3.72.1 PCS reset (3.2291.15) 20

21

Resetting the 10BASE-T1M / 10BASE-T1S PCS is accomplished by setting bit 3.2291.15 to one. This 22

action shall set all the~~10BASE-T1S~~ PCS registers to their default states. As a consequence, this action may 23

change the internal state of the ~~10BASE-T1S~~ PCS and the state of the physical link. This action may also 24

initiate a reset in any other MMDs that are instantiated in the same package. This bit is self-clearing, and the 25

~~10BASE-T1S~~ PCS shall return a value of one in bit 3.2291.15 when a reset is in progress; otherwise, it shall 26

return a value of zero. The ~~10BASE-T1S~~ PCS is not required to accept a write transaction to any of its 27

registers until the reset process is completed. The control and management interface shall be restored to 28

operation within 0.5 s from the setting of bit 3.2291.15. During a reset, ~~a~~the PCS shall respond to reads from 29

bits 3.0.15, 3.8.15:14, and 3.2291.15. Reads for all other bits shall be ignored. 30

31

NOTE—This operation may interrupt data communication. 32

33

Bit 3.2291.15 is a copy of 3.0.15, and setting or clearing either bit shall set or clear the other bit. Setting 34

either bit shall reset the ~~10BASE-T1S~~ PCS. 35

36

##### Change 45.2.3.72.2 as follows: 37

38

#### 45.2.3.72.2 Loopback (3.2291.14) 39

40

The 10BASE-T1M / 10BASE-T1S PCS shall be placed in a loopback mode of operation when bit 3.2291.14 41

is set to one. When in loopback mode, the ~~10BASE-T1S~~ PCS shall accept data on the transmit path and 42

return it on the receive path. 43

44

The default value of bit 3.2291.14 is zero. 45

46

~~Bit 3.2291.14 is a copy of 3.0.14, and setting or clearing either bit shall set or clear the other bit. Setting~~ 47

~~either bit shall enable loopback.~~ 48

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#### 45.2.3.72.3 Duplex mode (3.2291.8) 1

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##### Insert a new paragraph at the end of 45.2.3.72.3 as follows: 3

4

This bit shall be ignored for the 10BASE- T1M PCS. 5

6

##### Change 45.2.3.73 and the title of [Table 45–299](#_bookmark109) (unchanged rows not shown) as follows: 7

8

#### 10BASE-T1M / 10BASE-T1S PCS status register (Register 3.2292) 9

10

The assignment of bits in the 10BASE-T1M / 10BASE-T1S PCS status register is shown in [Table 45–299.](#_bookmark109) 11

All the bits in the ~~10BASE-T1S~~ PCS status register are read only; a write to the ~~10BASE-T1S~~ PCS status 12

register shall have no effect.. 13

14

15

#### Table 45–299—10BASE-T1M / 10BASE-T1S PCS status register bit definitions 16

17

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Name** | **Description** | **R/Wa** |
| … | | | |

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aRO = Read only, LH = Latching High 21

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23

##### Change 45.2.3.73.1 as follows: 24

25

#### 45.2.3.73.1 Fault (3.2292.7) 26

27

When read as a one, bit 3.2292.7 indicates that the 10BASE-T1M / 10BASE-T1S PCS has detected a fault 28

condition on either the transmit or receive path. When read as a zero, bit 3.2292.7 indicates that the 29

~~10BASE-T1S~~ PCS has not detected a fault condition. This bit shall be implemented with latching high 30

behavior. 31

32

##### Change 45.2.3.73.2 as follows: 33

34

#### 45.2.3.73.2 Full duplex capability (3.2292.6) 35

36

When read as a one, bit 3.2292.6 indicates that the 10BASE-T1S PHY is capable of full- duplex operation. 37

When read as a zero, bit 3.2292.6 indicates that the 10BASE-T1S PHY is not capable of full- duplex 38

operation. 10BASE-T1M PHYs do not have full duplex capability. 39

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##### Change 45.2.3.74 and the title of [Table 45–300](#_bookmark113) (unchanged rows not shown) as follows: 1

2

#### 10BASE-T1M / 10BASE-T1S PCS diagnostic 1 (Register 3.2293) 3

4

The assignment of bits in the 10BASE-T1M / 10BASE-T1S PCS diagnostic 1 register is shown in Table 5

45–300. All the bits in the ~~10BASE-T1S~~ PCS diagnostic 1 register are read only and self-clear on read; a 6

write to the ~~10BASE-T1S~~ PCS diagnostic 1 register shall have no effect.. 7

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#### Table 45–300—10BASE-T1M / 10BASE-T1S PCS diagnostic 1 register bit definitions 10

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|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Name** | **Description** | **R/Wa** |
| … | | | |

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aRO = Read only, SC = Self-clearing 15

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17

##### Change 45.2.3.75 and the title of [Table 45–301](#_bookmark115) (unchanged rows not shown) as follows: 18

19

#### 10BASE-T1M / 10BASET1-S PCS diagnostic 2 (Register 3.2294) 20

21

The assignment of bits in the 10BASE-T1M / 10BASE-T1S PCS diagnostic 2 register is shown in 22

[Table 45–30](#_bookmark115)1. All the bits in the ~~10BASE-T1S~~ PCS diagnostic 2 register are read only and self-clear on 23

read; a write to the ~~10BASE-T1S~~ PCS diagnostic 2 register shall have no effect.. 24

25

26

#### Table 45–301—10BASE-T1M / 10BASE-T1S PCS diagnostic 2 register bit definitions 27

28

29

|  |  |  |  |
| --- | --- | --- | --- |
| **Bit(s)** | **Name** | **Description** | **R/Wa** |
| … | | | |

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aRO = Read only, SC = Self-clearing 33

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**79. IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol** 1

**(LLDP) type, length, and value (TLV) information elements** 2

3

4

## 79.3 IEEE 802.3 Organizationally Specific TLVs 5

6

##### Change the row for subtypes 10 to 255 in [Table 79–1](#_bookmark118) and insert a new row above it as follows (unchanged 7

##### rows not shown): 8

9

#### Table 79–1—IEEE 802.3 Organizationally Specific TLVs 10

11

|  |  |  |
| --- | --- | --- |
| **IEEE 802.3 subtype** | **TLV name** | **Subclause reference** |
| … | | |
| 9 | PLCA | [79.3.9](#_bookmark119) |
| ~~9~~10 to 255 | Reserved | — |

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##### Insert new subclause 79.3.9 (including [Figure 79–1](#_bookmark120)0, [Table 79–21](#_bookmark124), 79.3.9.1, 79.3.9.2, and 79.3.9.3) after 19

##### 79.3.8 (and its subclauses) as follows: 20

21

#### 79.3.9 PLCA TLV 22

23

The PLCA TLV is an optional TLV that indicates capabilities and status of [Clause 148](#_bookmark134) PLCA. [Figure 79–10](#_bookmark120) 24

shows the format of this TLV. 25

26

27

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| TLV type = 127 | TLV information string length = 9 | 802.3 OUI 00-12-0F | 802.3  subtype = 9 | PLCA support/ status | PLCA  nodeID |

28

29

30

7 bits

9 bits

3 octets

1 octet 2 octets

1 octet 31

### TLV header

### TLV information string 32

33

34

#### Figure 79–10—Link Aggregation TLV format 35

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37

#### PLCA support/status 38

39

The PLCA support/status field shall contain a bitmap that identifies the PLCA and D-PLCA support and 40

status of the local IEEE 802.3 LAN station as defined in [Table 79–21.](#_bookmark124) 41

42

* + - 1. **PLCA nodeID** 43

44

The PLCA nodeId field contains an integer value indicating the PLCA nodeId of the local IEEE 802.3 LAN 45

station. 46

47

#### PLCA TLV usage rules 48

49

An LLDPDU should contain no more than one PLCA TLV. Since this TLV is intended to inform a link 50

partner of capabilities, the PLCA TLV should be sent in an LLDPDU addressed to the Nearest Bridge group 51

address (see IEEE 802.1Q). If PLCA is not enabled, this field reports 255. 52

53

54

#### Table 79–21—PLCA support/status 1

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3

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Field** | **Length (Octets)** | **Format** | **Field definitions** | **Value/Values** | **Notes** |
| PLCA support/status | 2 | Bitmap | Bit 0 – PLCA supported | 1 = supported  0 = not supported | [30.16.1.1.13](#_bookmark38) |
| Bit 1 – PLCA status | 1 = TRUE  0 = FALSE | 30.16.1.1.2 |
| Bit 2 – PLCA admin state | 1 = enabled  0 = disabled | 30.16.1.1.1 |
| Bit 3 – D-PLCA sup- ported | 1 = supported  0 = not supported | [30.16.1.1.14](#_bookmark40) |
| Bit 4 – D-PLCA admin state | 1 = enabled  0 = disabled | [30.16.1.1.11](#_bookmark35) |
| Bits 5 to 15 | Reserved |  |
| PLCA nodeID | 1 | Unsigned Integer | 0 to 255 | 0 to 255 | 30.16.1.1.4 |

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## 79.5 Protocol implementation conformance statement (PICS) proforma for IEEE 802.3 1

## Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and 2

## value (TLV) information elements 3

4

#### 79.5.3 Major capabilities/options 5

6

##### Insert new row to the end of the protocol implementation conformance statement (PICS) proforma as 7

##### follows (unchanged rows and unchanged footnote number 142 in subclause 79.5 not shown): 8

9

10

11

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| \*PL | PLCA TLV | [79.3.9](#_bookmark119) |  | O | Yes [ ]  No [ ] |

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##### Insert new subclause 79.5.13 after 79.5.12 as follows: 17

18

#### 79.5.13 PLCA TLV 19

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22

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| PLC1 | PLCA support/status field | [79.3.9.1](#_bookmark121) | Contains a bitmap identifying PLCA and D-PLCA support defined in [Table 79–21](#_bookmark124) | PL:M | Yes [ ]  N/A [ ] |
| PLC2 | PLCA nodeID field | [79.3.9.2](#_bookmark122) | Contains an integer value indi- cating the PLCA nodeId | PL:M | Yes [ ]  N/A [ ] |
| PLC3 | PLCA TLV usage rules | [79.3.9.3](#_bookmark123) | PLCA support/status TLV should contain no more than one PLCA TLV | PL:O | Yes [ ]  No [ ]  N/A [ ] |

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**90. Ethernet support for time synchronization protocols** 1

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## 90.1 Introduction 4

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##### Change the second paragraph of 90.1, as modified by IEEE Std 802.3de-2022, as follows: 6

7

The TSSI is defined for 10BASE-T1S (see [Clause 147](#_bookmark131)) in full- duplex and point-to-point half- duplex 8

modes of operation, as well as 10BASE-T1M (Cl[ause 188](#_bookmark166)) and 10BASE-T1S ([Clause 147)](#_bookmark131) in half duplex 9

multidrop operation, and for other PHY types in full- duplex mode. It supports MAC operation at various 10

data rates. The MII [(Clause 22](#_bookmark6)), GMII (Clause 35), XGMII (Clause 46), 25GMII (Clause 106), XLGMII 11

(Clause 81), CGMII (Clause 81), 200GMII (Clause 117), and 400GMII (Clause 117) specifications are all 12

compatible with the gRS sublayer defined in 90.5. 13

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1. **Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA)** 1

**sublayer and baseband medium, type 10BASE-T1S** 2

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## 147.1 Overview 5

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##### Insert the following new paragraph into 147.1 after the second paragraph (“The 10BASE-T1S PHY is 7

##### specified ...”): 8

9

The PMA and PCS specifications of the 10BASE-T1S PHY when operating in multidrop mode are refined 10

in the 10BASE-T1M [Clause 188](#_bookmark166) PHY, which only supports multidrop mode. 10BASE-T1S and 11

10BASE-T1M PHYs use the same PMA and PCS control, status, and test registers. 12

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1. **PLCA Reconciliation Sublayer (RS)** 1

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## 148.2 Overview 4

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##### Change the first paragraph of 148.2 as shown: 6

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~~The working principle of PLCA is that transmit opportunities on a mixing segment are granted in sequence~~ 8

~~based on a node ID unique to the local collision domain (set by the management entity). The method of~~ 9

~~determination of the node ID and to\_timer by the management entity is beyond the scope of this standard.~~ 10

~~Proper operation of the~~ [~~Clause 148~~](#_bookmark133) ~~functionality assumes that the assigned node ID is unique in the local~~ 11

~~collision domain.~~PLCA grants transmit opportunities on a mixing segment in sequence based on a node ID 12

unique to the local collision domain. This defines a worst-case access time to each node and enables the 13

mixing segment to operate collision free, which allows full utilization of the media. The node ID is not 14

contained within the frames on the media. The node ID may be set by management or allocated using 15

Dynamic PLCA (see [148.4.7).](#_bookmark147) 16

17

## 148.4 PLCA Reconciliation Sublayer operation 18

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#### 148.4.4 PLCA Control 20

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#### 148.4.4.2 PLCA Control variables 22

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##### Insert new variables COL, dplca\_en, dplca\_txop\_claim, dplca\_txop\_end, dplca\_txop\_id, and 24

##### dplca\_txop\_node\_count into the list, in alphabetical order: 25

26

COL 27

The MII signal COL. 28

Values:TRUE or FALSE 29

30

dplca\_en 31

The dplca\_en signal controls the optional D-PLCA function. This signal maps to TRUE when 32

aDPLCAAdminState is enabled and to FALSE when aDPLCAAdminState is disabled. 33

Values:TRUE or FALSE 34

dplca\_txop\_claim 35

Notifies the D-PLCA state diagrams whether the transmit opportunity indicated by 36

dplca\_txop\_id was claimed by a node. Additionally, it specifies the type of claim. 37

See [148.4.7.2](#_bookmark150) definitions at txop\_claim\_table. 38

Values: 39

SOFT: A packet not including a COMMIT indication was received; SOFT claims may be 40

issued implicitly by nodes not supporting D-PLCA 41

HARD: A packet including a COMMIT indication was received; HARD claims may be issued 42

by D-PLCA enabled nodes, and occasionally by statically configured PLCA enabled nodes 43

NONE: The transmit opportunity is available to be claimed 44

45

dplca\_txop\_end 46

Notifies the D-PLCA state diagrams that the transmit opportunity indicated by the 47

dplca\_txop\_id variable has expired. 48

Values:TRUE or FALSE 49

dplca\_txop\_id 50

Copy of the curID variable, synchronized with dplca\_txop\_end. 51

Values:integer from 0 to 255 52

53

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dplca\_txop\_node\_count 1

Copy of PLCA node count synchronized with PLCA SYNCING cycle. 2

Values:integer from 0 to 255 3

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#### 148.4.4.4 Timers 5

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##### Insert new timer append\_commit\_timer in the list, in alphabetical order: 7

8

append\_commit\_timer 9

Timer used by D-PLCA to append a COMMIT to each transmitted packet. 10

Duration: 22 bit times. 11

Tolerance: ± 1 bit time. 12

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#### 148.4.4.6 State diagram 14

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##### Change [Figure 148–3](#_bookmark142) and [Figure 148–4](#_bookmark143) as shown: 16

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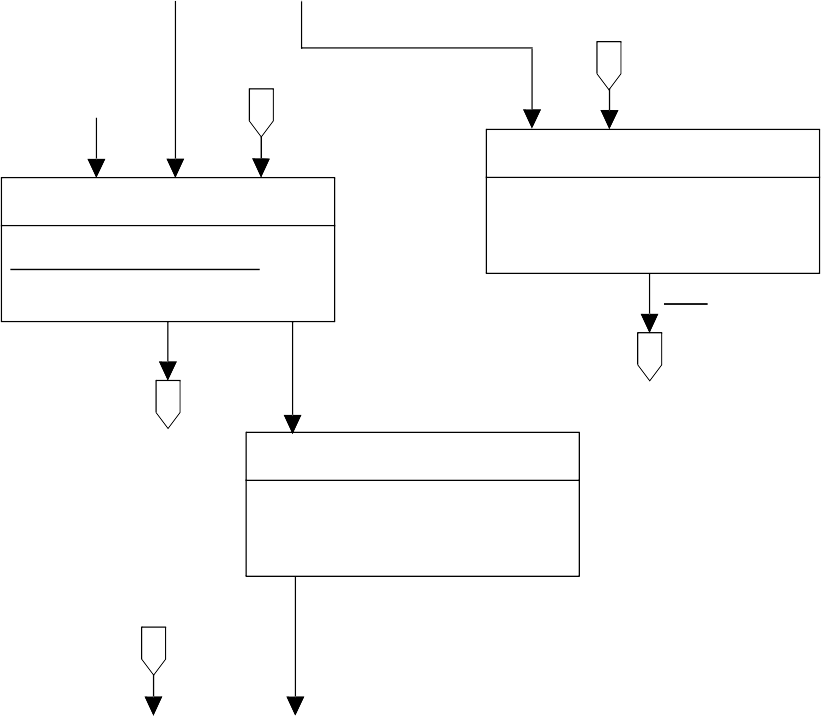
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plca\_reset + 4

(!plca\_en) + (local\_nodeID = 255) \* (!dplca\_en) 5



6

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DISABLE 8

9

tx\_cmd NONE 10

committed FALSE 11

curID 0

plca\_active FALSE 12

dplca\_txop\_claim NONE 13

dplca\_txop\_end FALSE

dplca\_txop\_id 0 14

dplca\_txop\_node\_count plca\_node\_count 15

16

plca\_en \* (local\_nodeID 0) \*

( (local\_nodeID 255) + dplca\_en )

invalid\_beacon\_timer\_done

plca\_en \* (local\_nodeID 0)

B

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C 18

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RECOVER 21

RESYNC

plca\_active FALSE dplca\_txop\_end FALSE

(local\_nodeID 0) \* CRS

E

plca\_active FALSE 22

23

24

UCT 25

26

PMCD \* (!CRS) \* (!TX\_EN) \* A 27

(local\_nodeID = 0) 28

29

SEND\_BEACON 30

31

start beacon\_timer tx\_cmd BEACON

32

plca\_active TRUE 33

34

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D 36

beacon\_timer\_done 37

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|  |  |
| --- | --- |
| SYNCING | |
| curID 0 tx\_cmd NONE  plca\_active TRUE  IF (local\_nodeID 0\* rx\_cmd BEACON) THEN start invalid\_beacon\_timer  END  dplca\_txop\_node\_count dplca\_txop\_id | |
| !CRS |  |

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#### Figure 148–3—PLCA Control state diagram, part a 51

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WAIT\_TO

start to\_timer dplca\_txop\_claim NONE dplca\_txop\_end FALSE dplca\_txop\_id curID

to\_timer\_done \*

(curID local\_nodeID) \* (!CRS)

COMMIT

YIELD

tx\_cmd COMMIT committed TRUE stop to\_timer

bc 0

IF COL THEN

dplca\_txop\_claim SOFT END

TX\_EN

(!TX\_EN) \*

(!packetPending)

BURST

TRANSMIT

bc bc + 1

tx\_cmd COMMIT start burst\_timer

IF max\_bc > 0 THEN start burst\_timer

ELSE

start append\_commit\_timer END

tx\_cmd NONE

IF bc max\_bc THEN committed FALSE

END

IF COL THEN

dplca\_txop\_claim SOFT END

EARLY\_RECEIVE

stop to\_timer

start beacon\_det\_timer dplca\_txop\_claim SOFT

RECEIVE

IF rx\_cmd = COMMIT THEN dplca\_txop\_claim HARD

END

CRS

NEXT\_TX\_OPPORTUNITY

curID curID + 1 committed FALSE dplca\_txop\_end TRUE

A

E

CRS

(curID = local\_nodeID) \* ((!packetPending) + (!plca\_active)) \* (!CRS)

plca\_active \*

(curID = local\_nodeID) \* packetPending \* (!CRS)

(!CRS) \*

(local\_nodeID 0)

C

B

(!CRS) \*

(local\_nodeID 0) \* (rx\_cmd BEACON) \* beacon\_det\_timer\_done

to\_timer\_done

(local\_nodeID 0) \* (!receiving) \*

((rx\_cmd = BEACON) + ((!CRS) \*

beacon\_det\_timer\_not\_done))

D

COL

(!TX\_EN)

packetPending

\*

\*

CRS \*

to\_timer\_not\_done

receiving \* CRS

COL \*

(TX\_EN + CRS)

!CRS

(!TX\_EN) \*

(!CRS) \*

(bc max\_bc)

TX\_EN \* (max\_bc > 0)

(!TX\_EN) \*

(!TX\_EN) \*

((bc max\_bc) + dplca\_en)

(burst\_timer\_done + append\_commit\_timer\_done)

((local\_nodeID 0) \*

(curID plca\_node\_count)) + (curID = 255)

ELSE

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BURST

bc bc + 1

tx\_cmd COMMIT start burst\_timer

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| --- | --- | --- | --- |
|  | | ABORT | |
|  |  |
| tx\_cmd NONE committed FALSE | |
| !CRS | |  |

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#### Figure 148–4—PLCA Control state diagram, part b 54

#### 148.4.5 PLCA DATA state diagram 1

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#### 148.4.5.7 State diagram 3

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##### Change Figure 148-5 and Figure 148-6 as shown: 5

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plca\_reset + (!plca\_en) + (plca\_status OK)

MCD \* (!CRS)

\* (!committed)

C

MCD \* CRS \*

plca\_txen \* committed

1

2

3

WAIT\_IDLE

packetPending FALSE CARRIER\_STATUS CARRIER\_OFF SIGNAL\_STATUS NO\_SIGNAL\_ERROR

TXD ENCODE\_TXD(tx\_cmd\_sync) TX\_EN FALSE

TX\_ER ENCODE\_TXER(tx\_cmd\_sync) a 0

b 0

NORMAL

packetPending FALSE IF CRS THEN

CARRIER\_STATUS CARRIER\_ON

ELSE

CARRIER\_STATUS CARRIER\_OFF

END

TXD plca\_txd TX\_EN plca\_txen TX\_ER plca\_txer IF COL THEN

SIGNAL\_STATUS SIGNAL\_ERROR

ELSE

SIGNAL\_STATUS NO\_SIGNAL\_ERROR

END

ABORT

packetPending FALSE

TX\_ER ENCODE\_TXER(tx\_cmd\_sync) TXD ENCODE\_TXD(tx\_cmd\_sync)

RECEIVE

IF CRS \* (rx\_cmd COMMIT) THEN CARRIER\_STATUS CARRIER\_ON

ELSE

CARRIER\_STATUS CARRIER\_OFF

END

TXD ENCODE\_TXD(tx\_cmd\_sync) TX\_ER ENCODE\_TXER(tx\_cmd\_sync)

IDLE

packetPending FALSE CARRIER\_STATUS CARRIER\_OFF SIGNAL\_STATUS NO\_SIGNAL\_ERROR

TXD ENCODE\_TXD(tx\_cmd\_sync) TX\_EN FALSE

TX\_ER ENCODE\_TXER(tx\_cmd\_sync) a 0

b 0

HOLD

packetPending TRUE CARRIER\_STATUS CARRIER\_ON

a a + 1

TX\_ER ENCODE\_TXER(tx\_cmd\_sync) TXD ENCODE\_TXD(tx\_cmd\_sync)

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ELSE 14

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B 16

ELSE

(!receiving) \* (!plca\_txen)

receiving \* (!plca\_txen) \* (tx\_cmd = NONE)

plca\_txen

plca\_en \*

(!plca\_reset) \* (!CRS) \* (plca\_status = OK)

plca\_txen

ELSE

MCD \* (!committed) \* (!plca\_txer) \* (!receiving) \* (a < delay\_line\_length)

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ELSE 27

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MCD \* D 43

plca\_txer 44

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(!plca\_txer) \* (receiving + (a delay\_line\_length))

A

B ELSE

49

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!plca\_txen

MCD \* committed \* (!receiving) \* 51

(!plca\_txer) \* (a < delay\_line\_length) 52

53

#### Figure 148–5—PLCA Data state diagram, part a 54

ELSE

ELSE

ELSE

B

A

COLLIDE

packetPending FALSE CARRIER\_STATUS CARRIER\_ON SIGNAL\_STATUS SIGNAL\_ERROR

a 0

b 0

TXD ENCODE\_TXD(tx\_cmd\_sync) TX\_ER ENCODE\_TXER(tx\_cmd\_sync) start pending\_timer

!plca\_txen

DELAY\_PENDING

SIGNAL\_STATUS NO\_SIGNAL\_ERROR

TXD ENCODE\_TXD(tx\_cmd\_sync) TX\_ER ENCODE\_TXER(tx\_cmd\_sync)

pending\_timer\_done

PENDING

packetPending TRUE start commit\_timer

TXD ENCODE\_TXD(tx\_cmd\_sync) TX\_ER ENCODE\_TXER(tx\_cmd\_sync)

committed

WAIT\_MAC

CARRIER\_STATUS CARRIER\_OFF

TXD ENCODE\_TXD(tx\_cmd\_sync)

ELSE

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plca\_txen \* plca\_txer 11

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D 14

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TX\_ER ENCODE\_TXER(tx\_cmd\_sync)

MCD \* plca\_txen

TRANSMIT

packetPending FALSE CARRIER\_STATUS CARRIER\_ON

TXD plca\_txdn–a TX\_EN TRUE

TX\_ER plca\_txer IF COL THEN

SIGNAL\_STATUS SIGNAL\_ERROR

a 0

36

(!plca\_txen) \* commit\_timer\_done 26

27

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MCD \* plca\_txen

ELSE

SIGNAL\_STATUS NO\_SIGNAL\_ERROR

END 37

38

MCD \* (!plca\_txen) \* (a > 0)

FLUSH

CARRIER\_STATUS CARRIER\_ON

TXD plca\_txdn–a TX\_EN TRUE

TX\_ER plca\_txer b b + 1

IF COL THEN

MCD \* (!plca\_txen) \* (a = 0) 39

40

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MCD \* (a b)

ELSE END

SIGNAL\_STATUS SIGNAL\_ERROR 46

SIGNAL\_STATUS NO\_SIGNAL\_ERROR 47

48

MCD \* (b = a) 49

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C 52

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#### Figure 148–6—PLCA Data state diagram, part b 54

##### Insert new subclause 148.4.7 (and Figures 148-8 and 148-9) after 148.4.6 (and its subclauses) as follows: 1

2

#### Dynamic (D-PLCA) 3

4

#### D-PLCA state diagram overview 5

6

D-PLCA is an optional feature of the PLCA RS that reduces the amount of configuration required to use 7

PLCA. D-PLCA enables nodes to select unique node IDs automatically and defines a method to designate a 8

single node with ID = 0 (coordinator). If the D-PLCA option is implemented, it shall comply with the state 9

diagrams in [Figure 148–8](#_bookmark155) and [Figure 148–9.](#_bookmark157) 10

11

D-PLCA adjusts aPLCANodeCount and aPLCALocalNodeID based on transmit opportunity claims 12

observed on a mixing segment. When a mixing segment contains a mixture of nodes with D-PLCA active 13

and not active, the D-PLCA nodes select IDs outside the space of the statically assigned IDs. When D-PLCA 14

is active, PHYs detect collisions as part of the nodeId assignment process. 15

16

D-PLCA keeps track of claimed transmit opportunities, distinguishing between HARD claims (with 17

COMMIT requests) and SOFT claims (without explicit COMMITs). The aging algorithm assigns two 18

different aging times for HARD and SOFT claims to avoid the case where non PLCA-enabled nodes may 19

prevent D-PLCA from converging. The variables hard\_aging\_cycles and soft\_aging\_cycles can be 20

configured to optimize convergence time and stability over time in different situations. The value of 21

hard\_aging\_cycles should be sufficiently greater than the value of soft\_aging\_cycles to maintain stability of 22

the D-PLCA process as well as interoperability with statically configured PLCA nodes. 23

24

#### D-PLCA variables 25

26

coordinator\_role\_allowed 27

This variable controls whether the local node is allowed to take the coordinator role 28

(local\_nodeID = 0) during the D-PLCA node assignment procedure. This variable maps on the 29

aDPLCACoordinatorRoleAllowed attribute in [30.16.1.1.10](#_bookmark33). 30

Values: TRUE or FALSE 31

dplca\_aging 32

This variable controls the state of the D-PLCA aging state diagram. 33

Values: ON or OFF 34

35

dplca\_en 36

See [148.4.4.2](#_bookmark139). 37

dplca\_new\_age 38

Internal variable used to synchronize the D-PLCA Control State Diagram with the D-PLCA 39

Aging State Diagram so that changes in the node ID allocation occur at the end of a cycle of 40

transmit opportunities. 41

Values: TRUE or FALSE 42

43

dplca\_txop\_claim 44

See [148.4.4.2](#_bookmark139). 45

dplca\_txop\_end 46

See [148.4.4.2](#_bookmark139). 47

48

dplca\_txop\_id 49

See [148.4.4.2](#_bookmark139). 50

dplca\_txop\_node\_count 51

See [148.4.4.2](#_bookmark139). 52

53

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dplca\_txop\_table\_upd 1

Synchronization variable set by the D-PLCA aging state diagram to notify the D-PLCA control 2

state diagram that the table of transmit opportunity has been updated. 3

Values: TRUE or FALSE 4

hard\_aging\_cycles 5

Defines the number of BEACON cycles before the HARD claims over the transmit opportuni- 6

ties expire. This variable maps to the aDPLCAHardAgingCycles attribute defined in 7

[30.16.1.1.9](#_bookmark31). 8

Values: positive integer number 9

10

local\_nodeID 11

See [148.4.4.2](#_bookmark139). 12

long\_cnt 13

Counter of BEACON cycles for the long aging time (HARD claims). 14

Values: positive integer number 15

16

plca\_en 17

See [148.4.4.2](#_bookmark139). 18

plca\_node\_count 19

See [148.4.4.2](#_bookmark139). 20

21

plca\_reset 22

See [148.4.4.2](#_bookmark139) 23

plca\_status 24

See 148.4.6.2. 25

26

rx\_cmd 27

See [148.4.4.2](#_bookmark139). 28

short\_cnt 29

Counter of BEACON cycles for the short aging time (SOFT claims). 30

Values: positive integer number 31

32

soft\_aging\_cycles 33

Defines the number of BEACON cycles before the SOFT claims over the transmit opportuni- 34

ties expire. This variable maps to the aDPLCASoftAgingCycles attribute defined in 35

[30.16.1.1.8](#_bookmark29). 36

Values: positive integer number 37

txop\_claim\_table 38

This variable contains the claim state of the 256 transmit opportunities IDs. The claim state of 39

each ID can be: 40

41

NONE, meaning that the transmit opportunity ID is available to be returned by the 42

PICK\_FREE\_TXOP function. 43

SOFT, meaning the ID is currently claimed by a node transmission that did not include a 44

COMMIT indication. 45

46

HARD, meaning the ID is currently claimed by a node transmission that included a COMMIT 47

indication at the beginning or at the end of the carrier event. 48

The transmit opportunity table is maintained by the D-PLCA aging state diagram defined in 49

[Figure 148–](#_bookmark157)9. 50

Values: Array of 256 elements, each having a value of NONE, SOFT or HARD. 51

52

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txop\_claim\_table\_new 1

Copy of txop\_claim\_table used by the D-PLCA Aging State Diagram to handle the expiration 2

of HARD claims. 3

Values: same as txop\_claim\_table 4

5

#### Functions 6

7

CLEAR\_SOFT\_CLAIMS 8

This function takes as an argument either the txop\_claim\_table or the txop\_claim\_table\_new 9

variable. When invoked, it reverts all of the array elements that have been marked as SOFT 10

claims to NONE. 11

CLEAR\_TXOP\_TABLE 12

This function takes as an argument either the txop\_claim\_table or the txop\_claim\_table\_new 13

variable. When invoked, it sets all of the 256 elements of the specified table to the NONE 14

claim state. 15

16

HARD\_CLAIMING 17

This function takes as parameter “ID”, a transmit opportunity integer number in the range of 0 18

to 255. It returns the result of the following boolean expression: 19

dplca\_txop\_end \* (dplca\_txop\_claim = HARD) \* (dplca\_txop\_id = ID) 20

MAX\_HARD\_CLAIM 21

This function takes as parameter the txop\_claim\_table defined in [148.4.7.2.](#_bookmark150) 22

It returns the highest ID in the table which is marked as HARD claimed. Note that the ID 23

claimed by the local node does not count as claimed. 24

25

PICK\_FREE\_TXOP 26

This function takes as parameter the txop\_claim\_table defined in [148.4.7.2.](#_bookmark150) 27

It returns any ID that is not marked as HARD or SOFT claimed in the table, with the following 28

exceptions: 29

* + - * 1. it shall not return zero, which is reserved for the PLCA coordinator 30

31

* + - * 1. it shall not return an ID greater than the highest HARD claimed in the table, unless this is the 32

only one available. 33

Note that it is allowed for this function to return the ID currently being claimed by the local 34

node, unless it is claimed by another node. The actual criteria for choosing among the avail- 35

able, allowed IDs is implementation defined. 36

37

SOFT\_CLAIMING 38

This function takes as parameter “ID”, a transmit opportunity integer number in the range of 0 39

to 255. It returns the result of the following boolean expression: 40

dplca\_txop\_end \* (dplca\_txop\_claim = SOFT) \* (dplca\_txop\_id = ID) 41

42

* + - 1. **Timers** 43

44

wait\_beacon\_timer 45

Represents the time the D-PLCA state diagram waits for a BEACON indication. 46

Duration: the duration of this timer is defined by the aDPLCAWaitBeaconTimer configuration 47

parameter. 48

Tolerance: 1 BT 49

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#### D-PLCA Control state diagram 1

plca\_reset + (!dplca\_en) + (!plca\_en) 2

3

LEARNING

local\_nodeID 255 dplca\_aging ON

FOLLOWER

local\_nodeID PICK\_FREE\_TXOP(txop\_- claim\_table)

WAIT\_BEACON

local\_nodeID 255

plca\_node\_count 8

REDUCE\_NODE\_COUNT

plca\_node\_count MAX\_HARD\_CLAIM(txop\_claim\_table)

+ 2

INCREASE\_NODE\_COUNT

plca\_node\_count plca\_node\_count + 1

COORDINATOR

local\_nodeID 0 dplca\_aging ON

wait\_beacon\_timer\_done \* (!coordinator\_role\_allowed) \* (plca\_status = FAIL)

plca\_status = OK

wait\_beacon\_timer\_done \* coordinator\_role\_allowed \* (plca\_status = FAIL)

(!HARD\_CLAIMING(0)) \*

(rx\_cmd BEACON) \* dplca\_txop\_table\_upd \* (!HARD\_CLAIMING(plca\_node\_count - 1)) \* (plca\_node\_count > 8) \*

dplca\_new\_age

( dplca\_txop\_table\_upd \* HARD\_CLAIMING(0) ) +

(rx\_cmd = BEACON)

!dplca\_new\_age

(!HARD\_CLAIMING(0)) \*

(rx\_cmd BEACON) \* dplca\_txop\_table\_upd \* HARD\_CLAIMING(plca\_node\_count - 1) \* (plca\_node\_count < 255) \* dplca\_new\_age

plca\_status = FAIL

dplca\_txop\_table\_upd \* dplca\_new\_age \* (plca\_status = OK)

!dplca\_new\_age

dplca\_txop\_table\_upd \* (plca\_status = OK) \* (

HARD\_CLAIMING(local\_nodeID) + SOFT\_CLAIMING(local\_nodeID) +

( (dplca\_txop\_id = 0) \* (dplca\_txop\_node\_count local\_nodeID) ) +

plca\_status = FAIL

4

|  |  |
| --- | --- |
| DISABLED | |
| start wait\_beacon\_timer dplca\_aging OFF | |
|  | UCT |

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( dplca\_new\_age \* 50

(local\_nodeID > MAX\_HARD\_CLAIM(txop\_claim\_table)) )

51

)

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#### Figure 148–8—D-PLCA Control State Diagram 53

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#### D-PLCA Aging state diagram

1

dplca\_aging = OFF 2

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|  |  |
| --- | --- |
| DISABLED | |
| CLEAR\_TXOP\_TABLE(txop\_claim\_table) CLEAR\_TXOP\_TABLE(txop\_claim\_table\_new) short\_cnt 0  long\_cnt 0 dplca\_new\_age FALSE  dplca\_txop\_table\_upd FALSE | |
|  | UCT |

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TXOP\_END

IF dplca\_txop\_id = 0 THEN

IF short\_cnt = SOFT\_AGAIN\_CYCLES THEN CLEAR\_SOFT\_CLAIMS(txop\_claim\_table) CLEAR\_SOFT\_CLAIMS(txop\_claim\_table\_new) short\_cnt 0

ELSE

short\_cnt short\_cnt + 1 END

IF long\_cnt = HARD\_AGING\_CYCLES THEN txop\_claim\_table txop\_claim\_table\_new clear\_txop\_table(txop\_claim\_table\_new) dplca\_new\_age TRUE

long\_cnt 0 ELSE

long\_cnt long\_cnt + 1 END

END

dplca\_txop\_claim = SOFT

dplca\_txop\_claim = NONE dplca\_txop\_claim = HARD

12

|  |  |
| --- | --- |
| WAIT\_TXOP\_END | |
| dplca\_new\_age FALSE dplca\_txop\_table\_upd FALSE | |
|  | dplca\_txop\_end |

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| --- | --- | --- |
| UPDATE\_SOFT | | |
| IF txop\_claim\_table[dplca\_txop\_id] = NONE THEN txop\_claim\_table[dplca\_txop\_id] SOFT  END  IF txop\_claim\_table\_new[dplca\_txop\_id] = NONE THEN txop\_claim\_table\_new[dplca\_txop\_id] SOFT  END | | |
|  | UCT | |
|  | |  |

|  |  |  |
| --- | --- | --- |
| UPDATE\_HARD | | |
| txop\_claim\_table[dplca\_txop\_id] HARD txop\_claim\_table\_new[dplca\_txop\_id] HARD | | |
|  | | UCT |
|  |  | |

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| --- | --- |
| NOTIFY | |
| dplca\_txop\_table\_upd TRUE | |
|  | !dplca\_txop\_end |

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#### Figure 148–9—D-PLCA Aging State Diagram 51

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## Protocol implementation conformance statement (PICS) proforma for 1

## [Clause 148](#_bookmark133), PLCA Reconciliation Sublayer (RS)6 2

3

#### Introduction 4

5

The supplier of a protocol implementation that is claimed to conform to [Clause 148](#_bookmark133), PLCA Reconciliation 6

Sublayer (RS), shall complete the following protocol implementation conformance statement (PICS) 7

proforma. 8

9

A detailed description of the symbols used in the PICS proforma, along with instructions for completing the 10

PICS proforma, can be found in Clause 21. 11

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#### Identification 13

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#### Implementation identification 15

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| --- | --- |
| Supplier1 |  |
| Contact point for inquiries about the PICS1 |  |
| Implementation Name(s) and Version(s)1,3 |  |
| Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)2 |  |
| NOTE 1—Required for all implementations.  NOTE 2—May be completed as appropriate in meeting the requirements for the identification.  NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier’s terminology (e.g., Type, Series, Model). | |

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#### Protocol summary 31

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| --- | --- |
| Identification of protocol standard | IEEE Std 802.3da-202x, [Clause 148,](#_bookmark133) PLCA Reconciliation Sublayer (RS) |
| Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS |  |
| Have any Exception items been required? No [ ] Yes [ ]  (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3da-202x.) | |

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Date of Statement

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6*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can 53

be used for its intended purpose and may further publish the completed PICS. 54

#### PICS proforma tables for PLCA Reconciliation Sublayer (RS) 1

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##### Insert new subclause 148.5.3.a before 148.5.3.1 3

4

#### 148.5.3.a Major capabilities/options 5

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| \*DP | Dynamic PLCA (D-PLCA) capability | [148.4.7](#_bookmark147) |  | O | Yes [ ] |

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##### Insert new subclause 148.5.3.7 after 148.5.3.6 14

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#### 148.5.3.7 D-PLCA 16

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| --- | --- | --- | --- | --- | --- |
| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| DP1 | D-PLCA Control | [148.4.7.5](#_bookmark154) | Conforms to [Figure 148–8](#_bookmark155) | DP:M | Yes [ ] |
| DP2 | D-PLCA Aging | [148.4.7.6](#_bookmark156) | Conforms to [Figure 148–9](#_bookmark157) | DP:M | Yes [ ] |

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##### Insert Clause 188 to Clause 189 in numeric order: 1

2

3

1. **Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA)** 4

**sublayer and baseband medium, type 10BASE-T1M** 5

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## Overview 8

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This clause defines the type 10BASE-T1M Physical Coding Sublayer (PCS) and type 10BASE-T1M 10

Physical Medium Attachment (PMA) sublayer. Together, the PCS and PMA sublayers comprise a 11

10BASE-T1M Physical Layer device (PHY). Functional and electrical specifications for the type 12

10BASE-T1M PCS, PMA, and the interface to the medium, referred to as the Trunk Connection Interface 13

(TCI) are provided in this clause. 14

15

The 10BASE-T1M PHY is specified to be capable of operating at 10 Mb/s using a single balanced pair of 16

conductors as a shared medium. The 10BASE-T1M PHY operates half duplex on a shared medium (i.e., a 17

mixing segment). The performance requirements for the mixing segment are specified in [188.8.](#_bookmark254) This allows 18

implementers to specify their own media to use with the 10BASE-T1M PHY as long as the normative 19

requirements included in this clause are met. 20

21

The 10BASE-T1M PHY is interoperable with the [Clause 147](#_bookmark131) 10BASE-T1S PHY when the 10BASE-T1S 22

PHY is in multidrop mode and the mixing segment is compliant with 147.8. The PMA and PCS 23

specifications of the 10BASE-T1S PHY when operating in multidrop mode are refined in the 10BASE-T1M 24

[Clause 188](#_bookmark167) PHY, which only supports multidrop mode. 10BASE-T1S and 10BASE-T1M PHYs use the 25

same PMA and PCS control, status, and test registers. 26

27

10BASE-T1M PHYs optionally support PHY Level Collision Avoidance (PLCA), described in [Clause 148](#_bookmark134). 28

29

10BASE-T1M follows an integrated PCS and PMA architecture and therefore does not support an AUI (see 30

Figure 1–1). 31

32

#### Relationship of 10BASE-T1M to other standards 33

34

The relationship between the 10BASE-T1M PHY, the ISO Open Systems Interconnection (OSI) Reference 35

Model, and the IEEE 802.3 Ethernet model are shown in [Figure 188–1.](#_bookmark170) The PHY sublayers (shown shaded) 36

in [Figure 188–1](#_bookmark170) connect one Clause 4 Media Access Control (MAC) layer to the medium. Auto- 37

Negotiation, as defined in Clause 98, is not available for the 10BASE-T1M PHY. A Management Entity is 38

required using MDIO or equivalent functionality. Optional MDIO is defined in [Clause 45.](#_bookmark73) 39

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OSI REFERENCE MODEL LAYERS

APPLICATION PRESENTATION SESSION TRANSPORT

NETWORK

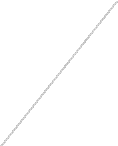
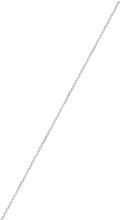
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ETHERNET 3

LAYERS 4

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HIGHER LAYERS

6

LLC - LOGICAL LINK CONTROL

7

OR OTHER MAC CLIENT

8

MAC CONTROL (OPTIONAL)

9

MAC - MEDIA ACCESS CONTROL 10

RECONCILIATION 11

12

MII1 13

14

DATA LINK PHYSICAL

TCI

PCS

PMA

MEDIUM 10BASE-T1M

PHY 15

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TCI = TRUNK CONNECTION INTERFACE MII = MEDIA INDEPENDENT INTERFACE

NOTE 1—MII is optional

PCS = PHYSICAL CODING SUBLAYER 22

PMA = PHYSICAL MEDIUM ATTACHMENT 23

PHY = PHYSICAL LAYER DEVICE 24

25

#### Figure 188–1—Relationship of 10BASE-T1M PHY 26

#### to the ISO/IEC OSI reference model and the IEEE 802.3 Ethernet model 27

28

#### Conventions in this clause 29

30

The body of this clause contains state diagrams including definitions of variables, constants, and functions. 31

Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. 32

33

#### State diagram notation 34

35

The conventions of 21.5 are adopted with the extension that some states in the state diagrams use an 36

IF-THEN-ELSE-END construct to condition which actions are taken within the state. If the logical 37

expression associated with the IF evaluates TRUE, then all the actions listed between THEN and ELSE will 38

be executed. In the case where ELSE is omitted, the actions listed between THEN and END will be 39

executed. If the logical expression associated with the IF evaluates FALSE, then the actions listed between 40

ELSE and END will be executed. After executing the actions listed between THEN and ELSE, between 41

THEN and END, or between ELSE and END, the actions following the END, if any, will be executed. 42

43

#### State diagram timer specifications 44

45

All timers operate in the manner described in 40.4.5.2. 46

47

#### Service specifications 48

49

The method and notation used in the service specification follows the conventions of 1.2.2. 50

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## Operation of 10BASE-T1M 1

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The 10BASE-T1M PHY supports only shared media (i.e., multidrop) half duplex communications over a 3

mixing segment comprised of a single balanced pair of conductors. The 10BASE-T1M PHY builds on the 4

operation of the 10BASE-T1S PHY defined in [Clause 147](#_bookmark131) when running half duplex in multidrop mode. 5

The mixing segment supports interconnecting up to at least 16 PHYs on a trunk of up to at least 50 m. PHYs 6

are attached to the mixing segment using the Trunk Connection Interface (TCI) specified in [188.9.](#_bookmark263) An 7

overall effective data rate of 10 Mb/s is shared among the nodes. Larger PHY count and reach can be 8

achieved provided the mixing segment specifications in [188.8](#_bookmark254) are met. 9

10

The 10BASE-T1M PHY utilizes two level Differential Manchester Encoding (DME). A 17-bit self- 11

synchronizing scrambler is used to improve the EMC performance. Following scrambling of the data, 4B/5B 12

encoding is performed (see [188.4.2.4).](#_bookmark197) DME is a self-clocked and intrinsically balanced line coding with 13

very low DC baseline wander and allows for robust clock and data recovery in noisy environments. The 14

4B/5B mapping and the scrambler are contained within the PCS (see [188.4)](#_bookmark190) while the DME 15

encoder/decoder is contained in the PMA (see [188.5).](#_bookmark223) 16

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## Service primitives and interfaces 1

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The 10BASE-T1M PHY uses the service primitives and interfaces in 40.2, with exception of the following 3

clarifications and differences noted in this subclause. [Figure 188–2](#_bookmark177) shows the relationship of the service 4

primitives and interfaces used by the 10BASE-T1M PHY. 5

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MANAGEMENT

PCS

PMA

MDC

MDIO

TX\_CLK

PMA\_UNITDATA.indication

TXD<3:0>

PMA\_UNITDATA.request

TX\_EN

PMA\_CARRIER.indication

TX\_ER

PCS\_STATUS.indication

COL

CRS

RX\_CLK RXD<3:0> RX\_DV

RX\_ER

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BI\_DA+

BI\_DA– 21

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31

MEDIA INDEPENDENT INTERFACE (MII)

PMA SERVICE INTERFACE



PHY

#### Figure 188–2—10BASE-T1M PHY interfaces

TRUNK 32

CONNECTION

33

INTERFACE

(TCI) 34

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39

The 10BASE-T1M PHY uses the Media Independent Interface (MII) as specified in [Clause 22.](#_bookmark6) 40

41

As shown in [Figure 188–2,](#_bookmark177) 10BASE-T1M uses the following service primitives to exchange symbol 42

vectors, status indications, and control signals across the PMA service interface: 43

44

PMA\_UNITDATA.indication (rx\_sym) 45

PMA\_UNITDATA.request (tx\_sym) 46

47

PMA\_CARRIER.indication (pma\_crs) 48

PMA\_LINK.indication (link\_status) 49

PMA\_LINK.request (link\_control) 50

PCS\_STATUS.indication (pcs\_status) 51

52

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54

#### PMA\_UNITDATA.indication 1

2

This primitive defines the transfer of one 5B symbol in the form of the rx\_sym parameter from the PMA to 3

the PCS. 4

5

#### Semantics of the primitive 6

7

PMA\_UNITDATA.indication (rx\_sym) 8

9

During reception, the PMA\_UNITDATA.indication conveys to the PCS, via the parameter rx\_sym, the 10

value of the 5B symbol detected on the TCI during each cycle of the recovered clock. 11

12

#### When generated 13

14

The PMA generates PMA\_UNITDATA.indication (rx\_sym) messages synchronously for every 5B symbol 15

received at the TCI. The nominal rate of the PMA\_UNITDATA.indication primitive is 2.5 MHz, as 16

governed by the recovered clock. 17

18

#### Effect of receipt 19

20

The effect of receipt of this primitive is specified in [188.4.3](#_bookmark207). 21

22

#### PMA\_UNITDATA.request 23

24

This primitive defines the transfer of one symbol in the form of the tx\_sym parameter from the PCS to the 25

PMA. 26

27

The symbol is obtained in the PCS Transmit function using the encoding rules defined in [188.4.2](#_bookmark192) to 28

represent 4B/5B encoded MII data or special out of band signaling. 29

30

#### Semantics of the primitive 31

32

PMA\_UNITDATA.request (tx\_sym) 33

34

During transmission, the PMA\_UNITDATA.request conveys the value of the symbol to be sent over the 35

TCI, via the parameter tx\_sym. 36

37

The tx\_sym parameter is one of the allowed 5B codes specified in [Table 188–1](#_bookmark198). 38

39

#### When generated 40

41

The PCS generates PMA\_UNITDATA.request (tx\_sym) synchronously with every symb\_timer expiration. 42

The symb\_timer is defined in [188.4.2.6.](#_bookmark200) 43

44

#### Effect of receipt 45

46

Upon receipt of this primitive the PMA transmits on the TCI the signals corresponding to the indicated 5B 47

symbol after processing it with DME following the rules in [188.](#_bookmark223)5. 48

49

#### Mapping of PMA\_CARRIER.indication 50

51

Reports whether a signal compatible with Differential Manchester Encoding (DME) encoding rules 52

specified in [188.5.2](#_bookmark226) is detected on the medium. 53

54

#### Function 1

2

Maps the primitive PMA\_CARRIER.indication to the MII CRS signal. 3

4

#### Semantic of the service primitive 5

6

PMA\_CARRIER.indication (pma\_crs) 7

8

The pma\_crs parameter can take one of two values: CARRIER\_ON or CARRIER\_OFF. 9

10

The pma\_crs parameter is set to CARRIER\_ON if a signal compatible with DME encoding rules specified 11

in [188.5.2](#_bookmark226) is present on the medium. Otherwise, the pma\_crs parameter is set to CARRIER\_OFF. 12

13

#### When generated 14

15

The PMA\_CARRIER.indication primitive is generated continuously by the PMA sublayer. 16

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## Physical Coding Sublayer (PCS) functions 18

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The Physical Coding Sublayer (PCS) consists of PCS Reset, PCS Transmit, and PCS Receive functions as 21

shown in [Figure 188–3.](#_bookmark194) The PCS Reset function is explained in [188.4.1,](#_bookmark191) the PCS Transmit function is 22

explained in [188.4.2,](#_bookmark192) the PCS Receive function is explained in [188.4.3,](#_bookmark207) and the PCS Loopback function is 23

explained in [188.4.4.](#_bookmark220) 24

25

#### PCS Reset function 26

27

PCS Reset initializes all PCS functions. The PCS Reset function shall be executed whenever any of the 28

following conditions occur: 29

30

1. Power on causes power\_on = TRUE (see 36.2.5.1.3) while pcs\_reset = FALSE. 31
2. The receipt of a request for reset from the management entity (bit 3.2291.15 defined in [45.2.3.72](#_bookmark103).1), 32

independently from the current state of pcs\_reset. 33

34

All state diagrams take the open-ended pcs\_reset branch upon execution of PCS Reset. PCS Reset shall keep 35

pcs\_reset = TRUE until the complete execution of the PCS Reset function, after which it is set to 36

pcs\_reset = FALSE. The reference diagrams do not explicitly show the PCS Reset function. 37

38

#### PCS Transmit 39

40

#### PCS Transmit overview 41

42

The PCS Transmit function shall conform to the PCS Transmit state diagram in [Figure 188–4](#_bookmark202) and 43

[Figure 188–](#_bookmark203)5, and the associated state variables, functions, timers, and messages. 44

45

At each symbol period, PCS Transmit generates a symbol tx\_sym conveyed to the PMA through the 46

PMA\_UNITDATA.request service primitive, where tx\_sym is a 5B symbol. The PMA encodes tx\_sym, 47

LSB first, into a DME stream over the conductor pair BI\_DA as defined in [Table 188–2.](#_bookmark229) 48

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Technology Dependent Interface (optional) 1

2



MANAGEMENT

PCS TRANSMIT

PMA\_UNITDATA.request

COLLISION DETECTION

PMA\_CARRIER.indication

MDC

MDIO

TX\_CLK

TXD<3:0>

TX\_EN

TX\_ER

(tx\_sym)

COL

CRS

(pma\_crs)

RX\_CLK

PMA\_UNITDATA.indication (rx\_sym)

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pcs\_reset

link\_control

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transmitting

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| --- | --- |
|  | PCS RECEIVE |
| RXD<3:0> |
| RX\_DV |
| RX\_ER |
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#### Figure 188–3—PCS reference diagram 38

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Upon assertion of TX\_EN, the PCS Transmit function passes two SYNC symbols to the PMA, followed by 41

two SSD symbols that replace the first 16 bits of the packet preamble. Following the second SSD, 42

TXD<3:0> is encoded into 5B symbols using the encoding rules specified in [Table 188–1,](#_bookmark198) until TX\_EN is 43

deasserted. 44

45

Following the deassertion of TX\_EN, the PCS Transmit generates a special code ESD. When there is no 46

transmit error, ESD is followed by ESDOK. When there is a transmit error, ESD is followed by ESDERR. 47

When a jabber condition is detected, ESD is followed by ESDJAB. 48

49

The 10BASE-T1M PHY has one special 5B symbol 'I' (see [Table 188](#_bookmark198)–1) which represents SILENCE. 50

SILENCE represents an indication for the PMA to change the output according to [188.5.2.](#_bookmark226) 51

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#### Variables 1

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err 3

This variable is set in the PCS Transmit state, as described in [Figure 188–4](#_bookmark202) and 4

[Figure 188–5.](#_bookmark203) 5

This variable is used to detect and latch a TX\_ER = TRUE condition during data 6

transmission; if such error is detected, an ESDERR symbol is sent at the end of 7

transmission. 8

Values: TRUE or FALSE 9

link\_control 10

This variable is generated by the Auto-Negotiation function. When Auto-Negotiation is 11

not present or Auto-Negotiation is disabled, link\_control has a default value of 12

ENABLE and may be provided by implementation-dependent functionality. When set to 13

DISABLE, all PCS functions are switched off and no data can be sent or received. 14

Values: ENABLE or DISABLE 15

16

pcs\_reset 17

The pcs\_reset parameter set by the PCS Reset function. 18

Values: TRUE or FALSE 19

transmitting 20

This variable is set in the PCS Transmit state, as described in [Figure 188–4](#_bookmark202). 21

When this variable is set to TRUE, it indicates a transmission is ongoing. 22

Values: TRUE or FALSE 23

24

tx\_cmd 25

Encoding present on TXD<3:0>, TX\_ER, and TX\_EN as defined in Table 22–1. 26

Values: 27

BEACON: PLCA BEACON indication encoding present on TXD<3:0>, TX\_ER, and 28

TX\_EN. 29

COMMIT: PLCA COMMIT indication encoding present on TXD<3:0>, TX\_ER, and 30

TX\_EN. 31

SILENCE: TXD<3:0> does not encode any of the above requests, or TX\_ER = FALSE, 32

or TX\_EN = TRUE. 33

TX\_EN 34

The TX\_EN signal of the MII as specified in 22.2.2.3. 35

When set to FALSE transmission is disabled. 36

When set to TRUE transmission is enabled. 37

Values: TRUE or FALSE 38

39

TX\_ER 40

The TX\_ER signal of the MII as specified in 22.2.2.5. 41

When set to FALSE it indicates a non-errored transmission. 42

When set to TRUE it indicates an errored transmission. 43

Values: TRUE or FALSE 44

tx\_sym 45

5B symbol to be conveyed to the PMA Transmit function by the means of the 46

PMA\_UNITDATA.request primitive specified in [188.3.2](#_bookmark182). 47

48

TXD 49

The TXD signal of the MII as specified in 22.2.2.4. 50

This signal represents a 4B data nibble to be transmitted. 51

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#### Constants 1

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ESD 3

5B symbol defined as 'T' in 4B/5B encoding. 4

ESDERR 5

5B symbol defined as 'K' in 4B/5B encoding. 6

7

ESDJAB 8

5B symbol defined as 'S' in 4B/5B encoding. 9

ESDOK / ESDBRS 10

5B symbol defined as 'R' in 4B/5B encoding. 11

12

SILENCE 13

5B symbol defined as 'I' in 4B/5B encoding. 14

SSD 15

5B symbol defined as 'H' in 4B/5B encoding. 16

17

SYNC / COMMIT 18

5B symbol defined as 'J' in 4B/5B encoding. 19

20

* + - 1. **Functions** 21

22

ENCODE 23

This function takes a 4 bit input parameter Scn<3:0> and returns a 5B symbol according 24

to the following procedure: 25

* + - * 1. Convert Scn<3:0> into Sdn<3:0> as specified in [188.4.2.8.](#_bookmark204) 26
        2. Convert Sdn<3:0> (4B symbol) into the corresponding 5B symbol defined 27

in [Table 188–](#_bookmark198)1. 28

29

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#### Table 188–1—4B/5B encoding 31

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|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **4B** | **5B** | **Special function** |
| 0 | 0000 | 11110 | — |
| 1 | 0001 | 01001 | — |
| 2 | 0010 | 10100 | — |
| 3 | 0011 | 10101 | — |
| 4 | 0100 | 01010 | — |
| 5 | 0101 | 01011 | — |
| 6 | 0110 | 01110 | — |
| 7 | 0111 | 01111 | — |
| 8 | 1000 | 10010 | — |
| 9 | 1001 | 10011 | — |
| A | 1010 | 10110 | — |
| B | 1011 | 10111 | — |
| C | 1100 | 11010 | — |

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TXCMD\_ENCODE

**Table 188–1—4B/5B encoding *(continued)*** 1

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| --- | --- | --- | --- |
| **Name** | **4B** | **5B** | **Special function** |
| D | 1101 | 11011 | — |
| E | 1110 | 11100 | — |
| F | 1111 | 11101 | — |
| I | N/A | 11111 | SILENCE |
| J | N/A | 11000 | SYNC / COMMIT |
| K | N/A | 10001 | ESDERR |
| T | N/A | 01101 | ESD |
| R | N/A | 00111 | ESDOK / ESDBRS |
| H | N/A | 00100 | SSD |
| N | N/A | 01000 | BEACON |
| S | N/A | 11001 | ESDJAB |

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In the PCS transmit process, this function takes as its argument the value of the tx\_cmd 24

variable and returns a 5B symbol based on the following mapping: 25

'N' when the tx\_cmd variable is set to BEACON, 26

'J' when the tx\_cmd variable is set to COMMIT, 27

'I' otherwise. 28

29

#### Abbreviations 30

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STD Alias for symb\_timer\_done. 32

33

* + - 1. **Timers** 34

35

symb\_timer 36

A continuous free-running timer. PMA\_UNITDATA.request messages are issued by the 37

PCS concurrently with symb\_timer\_done (see [188.3.2).](#_bookmark182) TX\_CLK (see 22.2.2.1) shall be 38

generated from symb\_timer with the rising edge of TX\_CLK generated synchronously 39

with symb\_timer\_done. 40

Continuous timer: The condition symb\_timer\_done becomes true upon timer expiration. 41

Restart time: Immediately after expiration. 42

Duration: 400 ns ± 100 ppm (see 22.2.2.1) 43

44

unjab\_timer 45

Optionally times the minimum duration the PHY suppresses any transmission before 46

reverting to normal operations. 47

Duration: 16 ms ± 100 s 48

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xmit\_max\_timer

1

Defines the maximum time the PCS Transmit state diagram can stay in DATA state. 2

The xmit\_max\_timer shall be implemented in such a way that, upon expiration, an even 3

number of nibbles has been sent to prevent the MAC from counting false alignment 4

errors. 5

Duration: 2 ms ± 100 s 6

NOTE—This is approximately 25% greater than maxEnvelopeFrameSize specified in 4.2.7.1. 7

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#### State diagram

STD \* (!TX\_EN) \*

pcs\_reset +

(link\_control = DISABLE)

**B**

SILENT

transmitting FALSE err FALSE

tx\_sym TXCMD\_ENCODE(tx\_cmd)

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STD \* 11

(!TX\_EN) \*

(tx\_cmd = COMMIT) 12

13

COMMIT 14

(tx\_sym TXCMD\_ENCODE(tx\_cmd)

STD \* TX\_EN

STD \* TX\_EN

|  |  |
| --- | --- |
| SYNC1 | |
| transmitting TRUE tx\_sym SYNC  err err + TX\_ER | |
|  | STD |

|  |  |
| --- | --- |
| SYNC2 | |
| err err + TX\_ER | |
|  | STD |

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18

STD \* (!TX\_EN) \*

19

(tx\_cmd = SILENCE) 20

21

**C** 22

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**A**

|  |  |
| --- | --- |
| SSD2 | |
| err err + TX\_ER start xmit\_max\_timer | |
|  | STD |

#### Figure 188–4—PCS Transmit state diagram, part a 53

|  |  |
| --- | --- |
| SSD1 | |
| tx\_sym SSD  err err + TX\_ER | |
|  | STD |

54

1

**A** 2

3

DATA 4

5

6

STD \*

tx\_sym ENCODE(TXD) err err + TX\_ER

7

8

TX\_EN \* xmit\_max\_timer\_not\_done

|  |  |  |  |
| --- | --- | --- | --- |
| BAD\_ESD | | |  |
| IF err THEN  tx\_sym ESDERR ELSE  tx\_sym ESDJAB  END | | |
|  | STD \* (!err) \* xmit\_max\_timer\_done | STD \* err | |
| JAB\_WAIT | |

STD \* (!TX\_EN) \*

|  |  |  |  |
| --- | --- | --- | --- |
| UN | | |  |
| tx\_sym SILENCE start unjab\_timer | |  |
|  |
|  |  | | |

unjab\_timer\_done

**C** STD \* 9

((!TX\_EN) +

xmit\_max\_timer\_done) 10

11

|  |  |  |
| --- | --- | --- |
| ESD | | |
| IF tx\_cmd COMMIT THEN tx\_sym ESD  ELSE  tx\_sym ESDBRS END | | |
|  | STD \*  (err + xmit\_max\_timer\_done) | S (!  x |

12

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16

TD \* 17

err) \*

mit\_max\_timer\_not\_done 18

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|  |  |  |
| --- | --- | --- |
|  | GOOD\_ESD | |
| tx\_sym ESDOK | |
| STD | |  |

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**B**

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Optional Implementation 34

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#### Figure 188–5—PCS Transmit state diagram, part b 36

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#### Self-synchronizing scrambler 39

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The PCS Transmit function shall implement multiplicative scrambling using the following generator 41

polynomial *g**x*

= *x*17

+ *x*14

+ 1 . 42

43

An implementation of a self-synchronizing scrambler by a linear-feedback shift register is shown 44

in [Figure 188–6.](#_bookmark205) The bits stored in the shift register delay line at time n are denoted by Scrn<16:0>. 45

The '+' symbol denotes the exclusive-OR logical operation. When Scn<3:0> is presented at the input of the 46

scrambler, Sdn<3:0> is produced by shifting in each bit of Scn<3:0> as Scn<i>, with i ranging from 0 to 3 47

(i.e., LSB first). The scrambler is reset upon execution of the PCS Reset function. If the PCS Reset is 48

executed, all bits of the 17-bit vector representing the self-synchronizing scrambler state are arbitrarily set. 49

The initialization of the scrambler state is left to the implementer. In no case shall the scrambler state be 50

initialized to all zeros. At every STD, if no data is presented at the scrambler input via Scn<3:0>, the 51

scrambler may be fed with arbitrary inputs. 52

53

54

Scn<i> **+**

Scrn<0>

# T

Sdn<i>

Scrn<1>

# T

Scrn<13>

# T

Scrn<14>

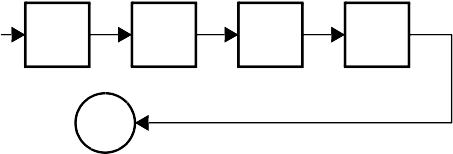
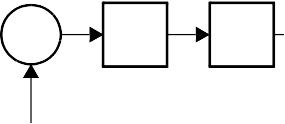
# T

Scrn<15>

# T

1

Scrn<16> 2



3

T 4

5

6

+ 7

8

Figure 188–6—Self-synchronizing scrambler 9

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* + - 1. Jabber functional requirements 12

13

The PCS Transmit function contains the capability to interrupt a transmission that exceeds a time duration 14

determined by xmit\_max\_timer. If the packet being transmitted continues longer than the specified time 15

duration, the PCS Transmit sends an ESD, ESDJAB symbol sequence to notify the receivers then inhibits 16

further transmissions for at least the duration of unjab\_timer. The PCS Transmit may return to normal 17

operation automatically after unjab\_timer elapsed and the error condition has been cleared or it may keep 18

silent until reset. 19

20

* + 1. PCS Receive 21

22

* + - 1. PCS Receive overview 23

24

The PCS Receive function shall conform to the PCS Receive state diagram in [Figure 188–7](#_bookmark215) and 25

[Figure 188–](#_bookmark216)8, and associated state variables. 26

27

The state diagram defined in [Figure 188–7](#_bookmark215) is triggered by the reception of a SYNC symbol from the PMA 28

Receive function and waits for two SSD symbols to start regenerating the packet preamble whose start has 29

been replaced with the SYNC, SYNC, SSD, SSD sequence by the PCS Transmit function as described 30

in [Figure 188–4.](#_bookmark202) After the second SSD is received, the PCS Receive function discards the next nine 31

symbols. These symbols can be used to achieve lock of the self-synchronizing descrambler. 32

33

During the descrambler locking time, the preamble nibble value (1010 in binary) is conveyed to the MII via 34

the RXD variable in order to rebuild the original preamble transmitted by the MAC (see 22.2.3.2.2 for 35

treatment of preamble nibbles). 36

37

The DATA state, in which 5B symbols are decoded into MII data, is left when ESD or ESDBRS followed by 38

either ESDOK, ESDERR, or ESDJAB symbol is encountered or when the PMA detects SILENCE on the 39

media (e.g., the transmitter prematurely stops data transmission). 40

41

During the WAIT\_SYNC state, the PCS notifies the RS of a received BEACON indication by the means of 42

the MII as specified in 22.2.2.8. When a sequence of at least two consecutive 'N' symbols is received, the 43

MII signals RX\_DV, RX\_ER, and RXD<3:0> are set to the BEACON indication as shown in Table 22–2. 44

Additionally, the PCS notifies the RS of a received COMMIT indication by the means of the MII as 45

specified in 22.2.2.8. When a sequence of at least two consecutive SYNC is received, the MII signals 46

RX\_DV, RX\_ER, and RXD<3:0> are set to the COMMIT indication as shown in Table 22–2. 47

48

* + - 1. Variables 49

50

link\_control 51

See [188.4.2.2.](#_bookmark195) 52

53

54

pcs\_reset precnt rx\_cmd RX\_DV RX\_ER RXD

RXn

transmitting

1

See [188.4.2.2.](#_bookmark195) 2

3

Counter for preamble regeneration. 4

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PLCA signalling decoded by the PCS. 7

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The RX\_DV signal of the MII as specified in 22.2.2.7. 9

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The RX\_ER signal of the MII as specified in 22.2.2.10. 12

13

PCS decoded data synchronous to RX\_CLK as specified in 22.2.2.8. 14

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The rx\_sym parameter of the PMA\_UNITADATA.indication primitive defined 17

in [188.3.1.](#_bookmark178) 18

The 'n' subscript denotes the rx\_sym conveyed in the most recent 19

recv\_symb\_conv\_timer cycle. 20

The 'n-x' subscript indicates the rx\_sym conveyed 'x' cycles before the most recent one. 21

22

See [188.4.2.2.](#_bookmark195) 23

24

* + - 1. **Constants** 25

26

BEACON 27

5B symbol defined as 'N' in 4B/5B encoding. 28

See also [188.4.2.3.](#_bookmark196) 29

30

FC\_SUPPORTED 31

Indicates whether the optional False Carrier detection is supported. 32

Values: TRUE or FALSE 33

34

* + - 1. **Functions** 35

36

DECODE 37

This function takes a 5B symbol input parameter and returns a 4 bit value Dcn<3:0> 38

value according to the following procedure: 39

* + - * 1. Convert the 5B input symbol into Drn<3:0> by performing a reverse lookup 40

in [Table 188–](#_bookmark198)1. If no 4B value is associated to the given 5B symbol, the PCS Receive 41

function shall assert RX\_ER for at least one symbol period and Drn<3:0> may be set 42

arbitrarily. 43

* + - * 1. Convert Drn<3:0> to Dcn<3:0> as specified in [188.4.3.8](#_bookmark217). 44

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#### Abbreviations 46

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RSCD Alias for recv\_symb\_conv\_timer\_done. 48

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* + - 1. **Timers** 1

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recv\_symb\_conv\_timer 3

A continuous timer which expires when the PMA\_UNITDATA.indication message is 4

generated (see [188.3.1).](#_bookmark178) 5

Continuous timer: The condition recv\_symb\_conv\_timer\_done becomes true upon timer 6

expiration. 7

Restart time: Immediately after expiration. 8

Duration: timed by the PMA\_UNITDATA.indication message generation. 9

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#### State diagrams

RSCD \*

((RXn = ESD) + ((RXn SSD) \* (RXn SYNC) \*

(!fc\_supported)))

RSCD \*

(RXn = SYNC)

pcs\_reset + (transmitting ) +

(link\_control = DISABLE)

**B**

WAIT\_SYNC

RX\_DV FALSE RX\_ER FALSE RXD 0000

rx\_cmd NONE

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RSCD \* 13

(RXn = BEACON) 14

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16

RSCD \*

(RX*n* SYNC) \* (RX*n* SSD) \* (RX*n* ESD) \* fc\_supported

SYNCING

RSCD \*

(RX*n* = SYNC)

COMMIT

RSCD \*

(RXn = SSD)

RSCD \*

(RXn = SSD)

**D** 17

18

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RSCD \* 25

(RXn = SSD) 26

27

WAIT\_SSD 28

RX\_ER TRUE RXD 0011

rx\_cmd COMMIT

RSCD \*

((RXn = ESD) + ((RXn SSD) \* (RXn SYNC) \*

(!fc\_supported)))

RSCD \*

RXD 0000

precnt 0 RX\_ER FALSE

rx\_cmd NONE

RSCD \*

(RXn = SSD)

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30

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33

RSCD \* 34

(RX SSD) \*

n

(!fc\_supported) 35

36

RSCD \*

(RX*n* SYNC) \* (RX*n* SSD) \* (RX*n* ESD) \* fc\_supported

BAD\_SSD

RSCD \*

(RXn = SILENCE + (RXn = ESD)

RX\_ER TRUE RXD 1110

rx\_cmd NONE

RSCD \*

((RX*n* = SILENCE) + (RX*n* = ESD))

(RX*n* SSD)\* fc\_supported

PRE

RX\_DV TRUE RXD 0101

IF precnt > 3 THEN precnt precnt + 1 DECODE(RXn-3)

ELSE

precnt precnt + 1 END

RSCD \*

(precnt = 9)

**A**

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RSCD 

precnt = 9

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RSCD \*

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(precnt 9)

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#### Figure 188–7—PCS Receive state diagram, part a 51

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RSCD \*

**A**

DATA

RXD DECODE(RXn–3)

1

2

RSCD \* 3

(!((((RXn–2 = ESD) + 4

(RXn–2 = ESDBRS)) \*

(RXn–1 ESDOK) \* 5

(RXn–3 ESD) \* 6

(RXn–3 ESDBRS)) +

(RXn–3 SILENCE))) \* 7

(!(((RXn–3 = ESD) + 8

(RXn–3 = ESDBRS)) \*

(RXn–2 = ESDOK))) 9

((((RXn–2 = ESD) + (RXn–2 = ESDBRS)) \* (RXn–1 ESDOK) \* (RXn–3 ESD) \* (RXn–3 ESDBRS)) + (RXn–3 SILENCE))

|  |  |
| --- | --- |
| BAD\_ESD | |
| RX\_ER TRUE RXD 0000 | |
|  |  |

RSCD

RSCD \*

((RXn–3 = ESD) + (RXn–3 = ESDBRS)) \* (RXn–2 = ESDOK)

RSCD

**B**

**D**

(RXn BEACON)

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14

|  |  |
| --- | --- |
| GOOD\_ESD | |
| RX\_DV FALSE RXD 0000 | |
|  |  |

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| --- | --- | --- |
| BEACON1 | | |
|  | | |
| RSCD \* |  |  |
| **B** | |

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RSCD \* 34

(RXn = BEACON) 35

36

37

|  |  |
| --- | --- |
| BEACON2 | |
| RX\_ER TRUE RXD 0010  rx\_cmd BEACON | |
|  | RSCD \* |

38

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(RXn BEACON) 44

**B**

45

#### Figure 188–8—PCS Receive state diagram, part b 46

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#### Self-synchronizing descrambler 1

2

The PCS Receive function descrambles the 5B/4B decoded data stream and returns the value of RXD<3:0> 3

to the MII. The descrambler shall employ the polynomial *g**x*defined in [188.4.2.8](#_bookmark204). The implementation of 4

the self-synchronizing descrambler by linear-feedback shift register is shown in [Figure 188–9](#_bookmark218). The bits 5

stored in the shift register delay line at time n are denoted by Dcrn<16:0>. The '+' symbol denotes the 6

exclusive-OR logical operation. 7

8

When Drn<3:0> is presented at the input of the descrambler, Dcn<3:0> is produced by shifting in each bit of 9

Drn<3:0> as Drn<i>, with i ranging from 0 to 3 (i.e., LSB first). The descrambler is reset upon execution of 10

the PCS Reset function. If PCS Reset is executed, all the bits of the 17-bit vector representing the self- 11

synchronizing descrambler state are arbitrarily set. The initialization of the descrambler state is left to the 12

implementer. At every RSCD, if no data is presented at the descrambler input via Drn<3:0>, the descrambler 13

may be fed with arbitrary inputs. 14

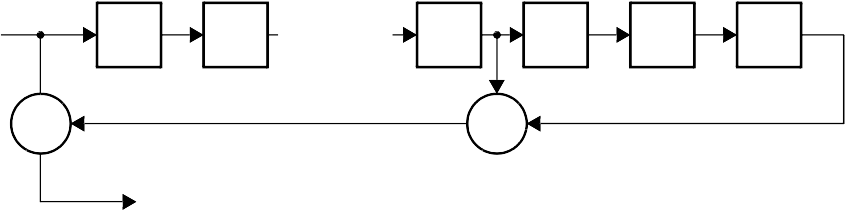
15

Dcrn<0>

Dcrn<1>

Dcrn<13> Dcrn<14> Dcrn<15> Dcrn<16> 16

17



Drn<i>

**+**

T T

Dcn<i>

T T T T 18

19

20

**+** 21

22

23

24

#### Figure 188–9—Self-synchronizing descrambler 25

26

27

#### Jabber diagnostics 28

29

The ESDJAB symbol informs the PCS Receiver that a frame was terminated by the jabber function. The 30

number of received ESDJAB events can be reported to the management entity be the means of MDIO 31

register 3.2293 or similar functionality if MDIO is not implemented. 32

33

#### 188.4.4 PCS loopback 34

35

The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.2291.14, defined in 36

[45.2.3.72.2](#_bookmark105) is set to one (or PCS loopback mode is enabled by a similar functionality if MDIO is not 37

implemented). In this mode, the PCS shall accept data on the transmit path from the MII and return it on the 38

receive path to the MII. Additionally, the PHY receive circuitry shall be isolated from the network medium, 39

and the assertion of TX\_EN at the MII shall not result in the transmission of data on the network medium. 40

41

#### Collision detection 42

43

The 10BASE-T1M PHY shall detect when a transmission initiated locally results in a corrupted signal at the 44

TCI as a collision. When collisions are detected, the PHY shall assert the signal COL on the MII for the 45

duration of the collision or until TX\_EN signal is FALSE. 46

47

The method for detecting a collision is implementation dependent but the following requirements have to be 48

fulfilled: 49

50

* + - 1. The PHY shall assert COL when it is transmitting and one or more other stations are also 51

transmitting at the same time. 52

* + - 1. The PHY shall assert CRS in the presence of a signal resulting from a collision between two or more 53

other stations. 54

#### Carrier sense 1

2

The 10BASE-T1M PHY senses when the media is busy and conveys this information to the MAC by 3

asserting the signal CRS on the MII as specified in 22.2.2.11. 4

5

CRS is generated by mapping the PMA\_CARRIER.indication (pma\_crs) primitive to the MII signal CRS: 6

7

* + - 1. CRS shall be asserted when the pma\_crs parameter is CARRIER\_ON. 8
      2. CRS shall be deasserted when the pma\_crs parameter is CARRIER\_OFF. 9

10

* 1. **Physical Medium Attachment (PMA) sublayer** 11

12

13

PMA functions are illustrated in [Figure 188–10](#_bookmark224). 14

15

16

PMA TRANSMIT

PMA\_UNITDATA.request (tx\_sym)

PMA\_UNITDATA.indication (rx\_sym)

17

18

19

BI\_DA+ 20

BI\_DA– 21

|  |  |  |
| --- | --- | --- |
|  | PMA RECEIVE | |
| PMA\_CARRIER.indication (pma\_crs) |
|  |
|  | | recei |

22

23

24

ved\_clock 25

26

CLOCK RECOVERY

27

TRUNK

PMA SERVICE INTERFACE

#### Figure 188–10—PMA functional block diagram

CONNECTION 28

INTERFACE 29

(TCI) 30

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35

The reference diagrams do not explicitly show the PMA Reset function. 36

37

The PMA couples messages from the PMA service interface specified in [188.4.1](#_bookmark191) onto the 10BASE-T1M 38

physical medium. The PMA provides half duplex communications to and from the medium. The interface 39

between PMA and the baseband medium is the Trunk Connection Interface (TCI), which is specified 40

in [188.9.](#_bookmark263) 41

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#### PMA Reset function 1

2

The PMA Reset function shall be executed whenever one of the two following conditions occur: 3

4

— Power on (see 36.2.5.1.3). 5

— The receipt of a request for reset from the management entity. 6

7

The PMA Reset function carries out the following tasks: 8

9

* PMA Transmit output is set to high-impedance state. 10
* PMA\_UNITDATA.indication is cleared. 11

12

#### PMA Transmit function 13

14

During transmission, PMA\_UNITDATA.request conveys the tx\_sym variable to the PMA. The value of the 15

tx\_sym variable is sent over the single balanced pair of conductors, BI\_DA. 16

17

The tx\_sym variable is a 5B symbol, to be encoded LSB first, using DME rules defined below: 18

19

If the tx\_sym parameter value is the special 5B symbol 'I', the PMA shall, in the following order: 20

21

* + - 1. Transmit an additional DME encoded 0 if the previous value of the tx\_sym parameter was anything 22

but the 5B symbol 'I'. 23

* + - 1. Meet the insertion loss specified from TC1 to TC2 in [188.9.1.1](#_bookmark266) and the return loss specified in 24

[188.9.2](#_bookmark268) at TC1 and TC2. This shall happen within 40 ns after the additional DME encoded 0 has 25

been transmitted. 26

27

If tx\_sym value is anything other than 'I', the following rules apply: 28

29

* A “clock transition” shall always be generated at the start of each bit. 30
* A “data transition” in the middle of a nominal bit period shall be generated if the bit to be 31

transmitted is a logical '1'. Otherwise, no transition shall be generated until the next bit. 32

33

See [Figure 188–11](#_bookmark227) and [Table 188–2](#_bookmark229). 34

35

36

T2

T3

37

38

39

clock

transition

data

transition

clock

transition 40

41

42

first transmission

high-Z or

diff. 0V

next transmission

T1

43

44

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48

#### Figure 188–11—DME encoding scheme 49

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#### 188.5.3 PMA Receive function

**Table 188–2—DME timings** 1

2

3

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Parameter name** | **Description** | **Minimum value** | **Nominal value** | **Maximum value** | **Unit of measure** |
| T1 | Delay between transmissions | 480 | — | — | ns |
| T2 | Clock transition to clock transition | –100 ppm | 80 | +100 ppm | ns |
| T3 | Clock transition to data transition (data = 1) | 38 | 40 | 42 | ns |

4

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The 10BASE-T1M PMA Receive function comprises a single receiver (PMA Receive) for DME modulated 14

signals on a single balanced pair of conductors, BI\_DA. PMA Receive has the ability to translate the 15

received signals on the single balanced pair of conductors into the PMA\_UNITDATA.indication parameter 16

rx\_sym. It detects 5B symbols from the signals received at the TCI and presents these sequences to the PCS 17

Receive function. 18

19

The PMA Receive function recovers encoded clock and data information from the DME encoded stream 20

received at the TCI. The clock recovery provides a synchronous clock for sampling the signal on the pair. 21

While it may not drive the MII directly, the clock recovery function is the underlying source of RX\_CLK. In 22

order to meet the specifications of [188.6.5](#_bookmark249).1, the PMA Receive function must achieve proper 23

synchronization on both the DME stream and the 5B boundary within 800 ns. 24

25

The PMA Receive function interprets the signals at the TCI using the inverse mapping described in [188.5.2](#_bookmark226) 26

for the PMA Transmit function and transfers the 5B code groups by the means of the 27

PMA\_UNITDATA.indication. When the PMA Receive function does not detect activity on the line, it shall 28

convey the symbol 'I' (meaning SILENCE.) 29

30

## PMA electrical specifications 31

32

33

This subclause defines the electrical characteristics of the PMA for a 10BASE-T1M PHY. 34

35

* + 1. **EMC tests** 36

37

Direct Power Injection (DPI) and 150 emission tests for noise immunity and emission as per [188.6.1.1](#_bookmark232) 38

and [188.6.1.2](#_bookmark233) may be used to establish a baseline for PHY EMC performance. These tests provide a high 39

degree of repeatability and a good correlation to immunity and emission measurements. Operational 40

requirements of the transceiver during the test are determined by the manufacturer. 41

42

Applications for the specified device commonly have additional requirements that limit its conducted radio 43

frequency emission and its susceptibility to electromagnetic interference. Such requirements are beyond the 44

scope of this standard. 45

46

#### Immunity—DPI test 47

48

In a real application, radio frequency (RF) common mode (CM) noise at the PHY is the result of 49

electromagnetic interference coupling to the cabling system. Additional differential mode (DM) noise at the 50

PHY is generated from the CM noise by mode conversion of all parts of the cabling system and the TCI. The 51

sensitivity of the PMA's receiver to RF CM noise may be tested according to the DPI method of 52

IEC 62132-4. 53

54

#### Emission—Conducted emission test 1

2

The emission of the PMA transmitter to its electrical environment may be tested according to the 150  3

direct coupling method of IEC 61967-4, and may need to comply with more stringent requirements. 4

5

#### Test modes 6

7

The test modes described in this subclause shall be provided to allow testing of the transmitter. The test 8

modes can be enabled by setting bits 1.2299.15:13 (10BASE-T1M / 10BASE-T1S test mode control 9

register) of the PHY Management register set as described in [45.2.1.236](#_bookmark96). If MDIO is not implemented, a 10

similar functionality shall be provided by equivalent means. These test modes shall not alter the electrical 11

and jitter characteristics of the transmitter and receiver from those that can appear in normal (i.e., non-test 12

mode) operation. 13

14

* + - 1. Test mode 1—Transmitter output voltage, timing jitter 15
      2. Test mode 2—Transmitter output droop test mode 16
      3. Test mode 3—Transmitter PSD mask 17
      4. Test mode 4—Transmitter high impedance mode 18

19

When test mode 1 is enabled, the PHY shall repeatedly transmit DME encoded ones. 20

21

When test mode 2 is enabled, the PHY shall transmit a positive differential voltage for 1.6 s followed by a 22

negative differential voltage level for 1.6 s. This sequence is repeated continually. 23

24

When test mode 3 is enabled, the PHY shall transmit continually a pseudo-random sequence of positive and 25

negative voltage levels generated by the scrambler defined in [188.4.2.8](#_bookmark204) and encoded using DME as 26

in [188.5.2.](#_bookmark226) 27

28

When test mode 4 is enabled, the transmitter shall output the 'I' symbol. This permits the requirements 29

of [188.5.2](#_bookmark226) to be tested. 30

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#### Test fixtures 1

2

The following fixtures (illustrated by [Figure 188–12](#_bookmark236) and [Figure 188–](#_bookmark237)13), or their functional equivalents, can 3

be used for measuring the transmitter specifications described in [188.6.4](#_bookmark238). 4

5

TC1 Transmitter load: 6

Transmitter Under Test

TX\_CLK

TCI TC2

High Impedance Differential Probe with resistance > 100 k and capacitance < 10 pF

of 100  7

8

9

Transmitter load: of 100 

10

11

12

13

14

15

Digital Oscilloscope 16

17

or 18

Data Acquisition 19

module 20

(Testing at TC2 shown, probe at TC1 for testing at TC1) 21

22

#### Figure 188–12—Transmitter test fixture 1 for transmitter voltage, 23

#### transmitter droop, and transmitter timing jitter 24

25

26

27

Transmitter Under Test

TC1

TCI

TC2

100 

load

Balun with diff. input impedance

0 of 100 

180

Spectrum Analyzer

28

29

30

31

(Testing at TC2 shown, balun connections interchange with load for testing at TC1) 32

33

#### Figure 188–13—Transmitter test fixture 2 for power spectral density (PSD) 34

**measurement** 35

36

To facilitate synchronization of the measurement equipment, it is recommended that the PHY provide 37

access to TX\_CLK. 38

39

#### Transmitter electrical specification 40

41

The PMA shall operate with AC coupling to the TCI. 42

43

Where a load is not specified, the transmitter shall meet the requirements of this subclause with a 50  44

resistive differential load connected to the transmitter output. Transmitter electrical tests are specified with a 45

load tolerance of ± 0.1%. Transmitter electrical specifications shall be measured at both TC1 and TC2. 46

When both TC1 and TC2 are terminated, the 50 resistive differential load should be implemented as a 47

100 termination on each of TC1 and TC2. 48

49

#### Transmitter output voltage 50

51

When tested using the test fixture shown in [Figure 188–12](#_bookmark236) with the transmitter in test mode 1, the 52

transmitter output voltage shall be 1 V ± 20% peak-to-peak differential. 53

54

#### Transmitter output droop 1

2

When tested using the test fixture shown in [Figure 188–12](#_bookmark236) with the transmitter in test mode 2, the magnitude 3

of both the positive and negative droop measured with respect to the initial peak value after the zero crossing 4

and the value 800 ns after the initial peak, depicted as Vd in [Figure 188–14](#_bookmark241), shall be less than 30%. 5

6

7

800 ns

Vd

Vpk

Droop = 100 x (Vd / Vpk) [%]

8

9

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11

12

13

14

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#### Figure 188–14—Transmitter output droop 25

26

27

#### Transmitter timing jitter 28

29

When measured using the test fixture shown in [Figure 188–12](#_bookmark236) with the transmitter in test mode 1, the 30

maximum jitter at the transmitter side shall be less than 5 ns symbol-to-symbol. 31

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#### Transmitter Power Spectral Density (PSD) 1

2

The upper and lower limits of the transmitter Power Spectral Density (PSD) are given in [Equation (188–1)](#_bookmark244) 3

and [Equation (188–2),](#_bookmark245) and shown in [Figure 188–15](#_bookmark246). 4

5

When measured using test mode 3 and the test fixture shown in [Figure 188–13,](#_bookmark237) or equivalent, the transmitter 6

Power Spectral Density (PSD) shall be between the upper and lower masks specified in [Equation (188–1)](#_bookmark244) 7

and [Equation (188–2).](#_bookmark245) 8

9

  10

–61

0.3 *f* 15  11

UpperPSD*f*= 

– 40 – 1.4 *f*

15 *f* 25 

dBm/Hz

(188–1) 12

 

where

–75

25 *f* 40  13

14

15

*f* is the frequency in MHz; 0.3 *f* 40 16

17

18

19

  20

– 77 + 10 *f* – 2.5

2.5 *f* 7  21







LowerPSD*f*= 

–67

------ 4.5



7 *f* 10





 dBm/Hz

22

(188–2) 23

 

 – -1---0---*f* – 10

10 *f* 16.5  24

– 67

6.5   25

  26

where 27

28

*f* is the frequency in MHz; 2.5 *f* 16.5 29

30

31

32

33

-55 34

35

-60 36

-65 37

38

-70 39

dBm/Hz

-75 40

41

-80 42

-85 43

44

-90 45

-95 46

0 5 10 15 20 25 30 35 40 47

48

Frequency (MHz) 49

50

#### Figure 188–15—PSD upper and lower limits 51

52

53

54

#### Transmitter high impedance mode 1

2

In test mode 4, the PCS shall continuously present the special 5B symbol 'I' to the PMA (see [188.5.2](#_bookmark226)). 3

4

#### Receiver electrical specifications 5

6

#### Receiver differential input signals 7

8

Differential signals received at the TCI that were transmitted from a remote transmitter within the 9

specifications of [188.6.4](#_bookmark238) and have passed through a mixing segment specified in [188.8](#_bookmark254) shall be received 10

with a Bit Error Ratio (BER) of less than 10–10 and sent to the MII during normal data transmission. This 11

specification can be verified by a frame error ratio less than 10–7 for 125 octet frames. 12

13

#### Alien crosstalk noise rejection 14

15

The test is performed with a noise source such that noise with a Gaussian distribution bandwidth of 40 MHz, 16

and magnitude of –101 dBm/Hz is present at the TCI. 17

18

The receive DUT is connected to these noise sources through a resistive network as shown in [Figure 188–16](#_bookmark251) 19

with mixing segment as defined in [188.8.](#_bookmark254) The BER shall be less than 10–10. This specification may be 20

considered satisfied when the frame loss ratio is less than 10–7 for 125 octet frames measured at MAC/PLS 21

service interface. 22

23

Edge

TC1

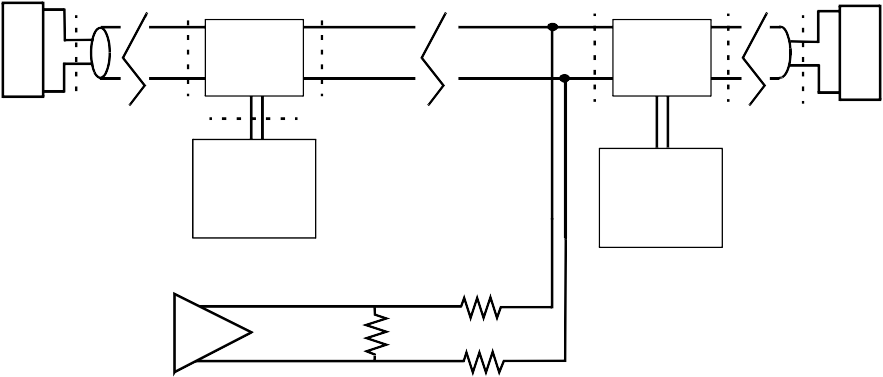
TC2

TC1

TC2

24

Edge 25



termination

TCI TCI

termination 26

100  100  27

28

Noise Source

Transmit DTE

Rs 

500 \*

500 \*

Receive 29

DTE 30

(DUT) 31

32

33

< 0.1 m 34

35

\*Resistor matching 36

to 1 part in 1000 37

NOTE - The combination of Rs and the two 500 resistors matches the 38

source impedance of the noise source. 39

40

#### Figure 188–16—Alien crosstalk noise rejection test set-up 41

42

#### 188.6.6 PMA local loopback 43

44

The PMA local loopback function is optional. If supported, the PMA shall be placed in local loopback mode 45

when the PMA local loopback bit in MDIO register 1.0.0, defined in 45.2.1.1, or the PMA loopback bit 46

in MDIO register 1.2297.13, defined in [45.2.1.234.5](#_bookmark87), is set to one (or PMA loopback mode is enabled by a 47

similar functionality if MDIO is not implemented). 48

49

The PMA and PCS Receive functions shall pass the data decoded from the signal to the MII RX. This data is 50

normally received during a transmission and may be used to detect collisions. 51

52

53

54

A MAC client can compare the packets sent through the MII Transmit function to the packets received from 1

the MII Receive function to validate the 10BASE-T1M PCS and PMA functions. 2

3

## Management interface 4

5

6

10BASE-T1M uses the management interface as specified in [Clause 45.](#_bookmark73) The [Clause 45](#_bookmark73) MDIO electrical 7

interface is optional. Where no physical embodiment of the MDIO exists, provision of an equivalent 8

mechanism to access the registers is recommended. 9

10

## Mixing segment characteristics 11

12

10BASE-T1M PHYs are designed to operate over media that meet the requirements specified in this 13

subclause. The 10BASE-T1M mixing segment (1.4.403) is a single balanced pair of conductors that may 14

have more than two DTEs attached. The trunk connection interface (TCI) [(1.4.582](#_bookmark3)a) is an MDI for the 15

shared transmission medium (single balanced pair of conductors). The cable media is referred to as "trunk” 16

cable. 17

18

The mixing segment shall be a linear topology, with DTE attached to a trunk at a TCI. Each TCI has two 19

connections, TC1 and TC2, on the mixing segment, one facing in each direction toward an edge termination. 20

Additionally, each TCI has a two-conductor connection facing the DTE (see [Figure 188–18](#_bookmark264)). See [188.9](#_bookmark263) for 21

more information on the TCI, which may be integrated within the DTE. If implemented with an associated 22

stub or service loop, that wiring is part of the DTE, and compliance of the attached DTE is specified at 23

points TC1 and TC2, including any effects of the stub or service loop. The TCI is part of the mixing 24

segment, and the requirements of the mixing segment are met with TCIs in place with or without attached 25

DTEs. Like the MDI, the specification of the TCI is not a device, but rather a (set of) interface planes. 26

27

The TCI is specified in [188.9](#_bookmark263) to enable the mixing segment specifications in [188.8](#_bookmark254) to be met. 28

29

[Figure 188–17](#_bookmark255) shows an example mixing segment with reference points. The mixing segment specifications 30

in [188.8](#_bookmark254) are referenced to these designated points and are to be met without the DTE or other loads attached. 31

The mixing segment specifications provide for a trunk-stub configuration, extended from the TCI. The 32

electrical parameters in [188.8](#_bookmark254) include all TCIs in the mixing segment, but do not include external 33

connections such as stubs or service loops from the TCI to the DTE hardware. The trunk is terminated at 34

each end into 100 , at the point designated the ‘edge termination’. 35

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Edge termination

TC1

TCI

TC2

TC1

TCI

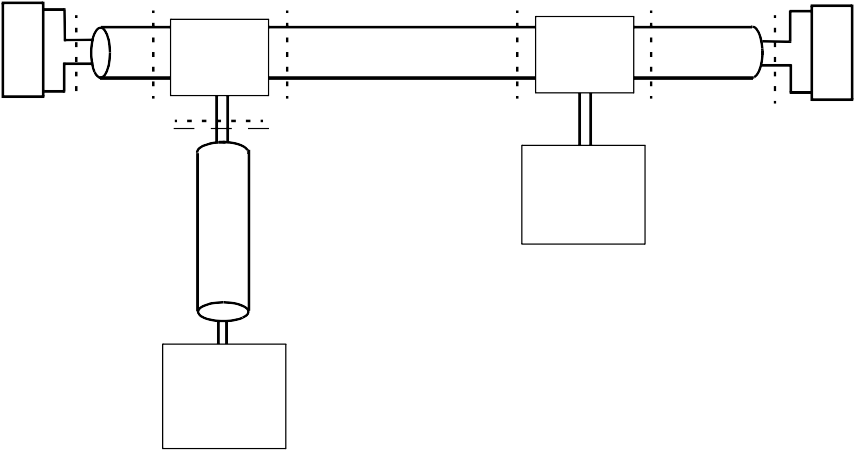
TC2

1

2

3

4



Edge 5

termination 6

100  100  7

8

stub (external to device, but considered specific to device)

DTE

PMA

9

DTE 10

11

12

13

14

NOTE – PMA transmit and receive 15

specifications are met at TC1 and TC2. This

applies whether or not an external stub is 16

present. 17

18

#### Figure 188–17—Example mixing segment and reference points 19

20

#### Insertion loss 21

22

Mixing segment insertion loss includes any TCI insertion loss. See [188.9.1.1](#_bookmark266) for specification of TCI 23

insertion loss. 24

25

The mixing segment insertion loss, with DTEs or representative simulated DTE loads attached, shall meet 26

the values determined using [Equation (188–3)](#_bookmark257) between edge termination attachment points. The reference 27

impedance is 100 If the mixing segment includes TCI connectors which are specified to use a simulated 28

DTE load, this requirement may be met with the simulated DTE load attached. 29

30

31

 



Insertion loss*f*





where

35 – 14.54 *f*

– 27 – 53log10*f*

– 1.7

-------

*f* 

+ 52 *f* – 8.9 *f* + 0.163 *f* 2

0.3

1.5

*f* 1.5 



*f* 40 



32

dB (188–3) 33

34

35

36

*f* is the frequency in MHz; 0.3 *f* 40 37

38

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#### Return loss 1

2

Mixing segment return loss includes any TCI return loss. See [188.9.2](#_bookmark268) for specification of TCI return loss. 3

4

The mixing segment with DTEs attached shall meet the values determined using [Equation (188–4)](#_bookmark259) at the 5

edge terminations. The reference impedance is 100 If the mixing segment includes TCI connectors which 6

are specified to use a simulated DTE load, this requirement may be met with the simulated DTE load 7

attached. 8

9

  10

0.8 0.3 *f* 1.6  11

 

RL*f*



7.34*f* – 10.21



0.024

1.6 *f* 2.8

dB

2 

(188–4) 12

13

 + – 

----------

+ 47.5 *f* – 6.39*f* + 0.0259*f*

2.8 *f* 40 

– 42.5

– 20log10 *f*

---

*f*  

14

where

  15

16

17

*f* is the frequency in MHz; 0.3 *f* 40 18

19

#### Mode conversion loss 20

21

The mode conversion loss of the 10BASE-T1M mixing segment shall meet the values determined 22

using [Equation (188–5](#_bookmark261)). 23

24

  25

43 0.3 *f* 20  26

Mode conversion loss*f*





where

43 – 20 log

--*f*- 

20

10--- 

 dB 20 *f* 200 



(188–5) 27

28

29

30

*f* is the frequency in MHz; 0.3 *f* 200 31

32

## TCI specification 33

34

The interface of the [Clause 188](#_bookmark167) PHY to the mixing segment is called the Trunk Connection Interface (TCI). 35

The TCI is an MDI for the shared transmission medium (single balanced pair of conductors). While 36

technically the TCI aligns with the definition of an MDI in 1.4.395, the fact that the TCI has two connections 37

to the medium and plays a role in mixing segment specifications by connecting the upstream and 38

downstream sides of the linear mixing segment mandates it has a unique role beyond what is normally 39

considered in an MDI. 40

41

Each TCI has one connection facing each direction of the mixing segment (TC1 and TC2) and a two- 42

conductor connection facing the DTE (including any associated stub or service loop) as shown in 43

[Figure 188–18.](#_bookmark264) 44

45

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Upstream side mixing segment

1

2

3

4

TCI

DTE, including any stubs or service loop

TC1

TC2

(2 conductors)

Downstream side 5

mixing segment 6

100  100  7

8

9

10

11

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#### Figure 188–18—TCI ports and connections 19

20

A TCI may physically be implemented as a “T” type connection to provide a means of connecting the trunk 21

segments and attaching a DTE to the mixing segment. 22

23

The TCI is part of the mixing segment, and the requirements of [188.8](#_bookmark254) are met with TCIs in place with or 24

without attached DTEs as specified for the particular specification. TCIs with compensation are expected to 25

be matched to a particular DTE/PMA implementation, including any associated stub or service loop. 26

27

The TCI may physically be implemented as: 28

29

* + 1. a two-conductor connection to the DTE, or 30
    2. an adapter separate from the DTE’s PMA assembly, or 31
    3. integrated, where the TCI and the PMA of the DTE are located within a single assembly. 32

33

The second configuration presents a negligible stub length if no PMA is attached. The third configuration 34

must be replaced to allow connectivity when the DTE is not present. Any configuration may include 35

compensation engaged when a PMA or simulated DTE load is attached. [Figure 188–17](#_bookmark255) shows one example 36

of each configuration. 37

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#### TCI electrical specification 39

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All TCI electrical specifications are intended to apply in the mixing segment’s operational condition. 41

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#### 188.9.1.1 TCI insertion loss 1

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With a DTE or simulated DTE load present at the TCI, the differential insertion loss of the TCI between 3

TC1 and TC2 shall meet the values determined using [Equation (188–6)](#_bookmark267) in each direction, measured into 4

100 . 5

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  7

0.6 0.3 *f* 1  8

0.16 1 *f* 10  9

 

Insertion loss*f*  dB

(188–6) 10

– 0.454 + 0----.-2---2--+ 0.63 *f* – 0.18*f* + 0.004*f*2

10 *f* 24  11

 *f* 

 12

 

where

0.145*f* – 2.86

24 *f* 40  13

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*f* is the frequency in MHz; 0.3 *f* 40 16

#### TCI return loss 17

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With a DTE or simulated DTE load present at the TCI, the return loss of the TCI at TC1 and TC2 shall meet 19

the values determined using [Equation (188–7)](#_bookmark269) with the other trunk TC (i.e., TC2 or TC1, respectively) ter- 20

minated in 100 . 21

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– 0.3 + 13*f*

0.3 *f* 1.7  24

  25

Return loss*f*



– 38.55 – 50.28log10

*f*– 3.16+ 69.31 *f* – 10.19*f* + 0.0636*f*2

 dB

1.7 *f* 40  26

 *f* 

----------

where

 27

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(188–7) 29

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*f* is the frequency in MHz; 0.3 *f* 40 32

#### TCI line powering voltage tolerance 33

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The DTE shall withstand without damage the application of any voltages between 0 V dc and 60 V dc 35

applied across TC1 or TC2’s BI\_DA+ and BI\_DA– in either polarity, under all operating conditions 36

indefinitely. 37

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#### TCI fault tolerance 1

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Each balanced pair of the TCI shall withstand without damage the application of short circuits of any 3

conductor to the other conductor of the same pair or ground potential, as per [Table 188–3](#_bookmark273), under all 4

operating conditions indefinitely. Normal operation shall resume after all short circuits have been removed. 5

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#### Table 188–3—Fault conditions 8

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| **BI\_DA+** | **BI\_DA–** |
| BI\_DA**–** | BI\_DA+ |
| Ground | No fault |
| No fault | Ground |
| Ground | Ground |
| +60 V dc | No fault |
| No fault | +60 V dc |
| +60 V dc | +60 V dc |
| Ground | +60 V dc |
| +60 V dc | Ground |

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## Environmental specifications 27

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#### General safety 29

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All equipment subject to this clause is expected to conform to IEC 60950-1, IEC 62368-1, or IEC 61010-1. 31

All equipment subject to this clause is expected to conform to all applicable local, state, national, and 32

application-specific standards. 33

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#### Network safety 35

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All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a 37

professional manner. All 10BASE-T1M cabling is expected to be routed according to any applicable local, 38

state, or national standards considering all relevant safety requirements. In automotive applications, all 39

10BASE-T1M cabling is expected to be routed to provide maximum protection by the motor vehicle sheet 40

metal and structural components, following SAE J1292, ISO 14229, and ISO 15764. The designer is urged 41

to consult the relevant local, national, and international safety regulations to ensure compliance with the 42

appropriate requirements. 43

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#### Environmental safety 45

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This subclause sets forth a number of recommendations and guidelines related to safety concerns; this list is 47

neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant 48

local, national, and international safety regulations to ensure compliance with the appropriate requirements. 49

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Systems described in this subclause are subject to various environmental hazards during their installation 51

and use. In particular, equipment used in automotive and industrial environments can expect to meet the 52

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potential environmental stresses with respect to their mounting location defined for the application. Stresses 1

expected in these environments may include but are not limited to those found in the listed specifications. 2

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The following specifications describe potential environmental stresses in an automotive environment: 4

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* General loads: ISO 16750-1 6
* Electrical loads: ISO 16750-2, ISO 7637-2, and ISO 8820-1 7
* Mechanical loads: ISO 16750-3, ASTM D4728, and ISO 12103-1 8

— Climatic loads: ISO 16750-4, and IEC 60068-2-1, IEC 60068-2-27, IEC 60068-2-30, 9

IEC 60068-2-38, IEC 60068-2-52, IEC 60068-2-64, and IEC 60068-2-78 10

* Chemical loads: ISO 16750-5 and ISO 20653 11

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The following specifications define potential environmental stresses in an industrial environment: 13

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* Environmental loads: IEC 60529 and ISO 4892 15
* Mechanical loads: IEC 60068-2-6 and IEC 60068-2-31 16

— Climatic loads: IEC 60068-2-1, IEC 60068-2-2, IEC 60068-2-14, IEC 60068-2-27, 17

IEC 60068-2-30, IEC 60068-2-38, IEC 60068-2-52, and IEC 60068-2-78 18

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Additional environment(s) require careful analysis prior to implementation to determine appropriate 20

environmental safety requirements. 21

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#### Electromagnetic compatibility 23

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A system integrating the 10BASE-T1M PHY is expected to comply with all applicable local and national 25

codes for electromagnetic compatibility. In addition, the system may need to comply with more stringent 26

requirements for the limitation of electromagnetic interference. 27

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#### Telephony voltages 29

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The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages 31

to a DTE. Other than voice signals, the primary voltages that may be encountered are the “battery” and 32

ringing voltages. Although there is no universal standard, the following maximums generally apply: Battery 33

voltage to a telephone line is generally 56 V dc, applied to the line through a balanced 400 Ω source 34

impedance. Ringing voltage is a composite signal consisting of an ac component and a dc component. The 35

ac component is up to 175 Vp at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc component is 56 V 36

dc with 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start and end of each 37

ring interval. 38

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Application of any of the above voltages to the TCI of a DTE in non-automotive applications shall not 40

preclude conformance with [188.10.1](#_bookmark275) and [188.10.2.](#_bookmark276) 41

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## Delay constraints 43

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The PHY shall comply with the timing requirements specified in [Table 188–](#_bookmark281)4. 46

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#### Table 188–4—10BASE-T1M delay constraints 1

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| --- | --- | --- | --- | --- | --- |
| **Event** | **Minimum value** | **Maximum value** | **Unit of measure** | **Input timing reference** | **Output timing reference** |
| TX\_EN/TX\_ER  sampled to TCI output | 120 | 440 | ns | Rising edge of MII TX\_CLK | First DME clock transition at the TCI |
| TCI input to CRS asserted | 400 | 1040 | ns | First DME clock transition at the TCI | Rising edge of CRS |
| TCI input to CRS deasserted | 640 | 1120 | ns | Last DME encoded zero clock transition at the TCI | Falling edge of CRS |
| TCI input to COL asserted | 0 | 5 | s | Start of corrupted transmitted signal at the TCI | Rising edge of COL |
| TCI input to COL deasserted | 0 | 3.2 | s | End of transmission at the TCI | Falling edge of COL |
| TCI input to RX\_DV asserted | 2.4 | 4 | s | First DME clock transition at the TCI | Rising edge of RX\_DV |
| TCI input to RX\_ER asserted | 1.6 | 4 | s | First DME clock transition at the TCI | Rising edge of RX\_ER |

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## Protocol implementation conformance statement (PICS) proforma for 1

## [Clause 188](#_bookmark167), Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) 2

## sublayer and baseband medium, type 10BASE-T1M7 3

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#### Introduction 5

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The supplier of a protocol implementation that is claimed to conform to [Clause 188,](#_bookmark167) Physical Coding 7

Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1M, 8

shall complete the following protocol implementation conformance statement (PICS) proforma. 9

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A detailed description of the symbols used in the PICS proforma, along with instructions for completing the 11

PICS proforma, can be found in Clause 21. 12

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#### Identification 14

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#### Implementation identification 16

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|  |  |
| --- | --- |
| Supplier1 |  |
| Contact point for inquiries about the PICS1 |  |
| Implementation Name(s) and Version(s)1,3 |  |
| Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)2 |  |
| NOTE 1—Required for all implementations.  NOTE 2—May be completed as appropriate in meeting the requirements for the identification.  NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier’s terminology (e.g., Type, Series, Model). | |

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#### Protocol summary 32

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| --- | --- |
| Identification of protocol standard | IEEE Std 802.3da-[202x, Clause 18](#_bookmark167)8, Physical Coding Sublayer (PCS), Physical Medium Attachment (PMA) sublayer and baseband medium, type 10BASE-T1M |
| Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS |  |
| Have any Exception items been required? No [ ] Yes [ ]  (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3da-202x.) | |

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Date of Statement

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7*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can 53

be used for its intended purpose and may further publish the completed PICS. 54

#### Major capabilities/options 1

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| \*MDIO | MDIO Capability | 45.1 | Register and Interface supported | O | Yes [ ]  No [ ] |
| \*INS- MIX | Installation / Mixing segment | [188.8](#_bookmark254) | Items marked with \*INS-MIX include installation practices and cabling specifications for mixing segments and are not applicable to a PHY manufacturer | O | Yes [ ]  No [ ] |
| MII | PHY associated with MII | [188.1.2](#_bookmark171) |  | O | Yes [ ]  No [ ] |
| PCS | 10BASE-T1M PCS | [188.4](#_bookmark190) |  | M | Yes [ ]  No [ ] |
| PMA | 10BASE-T1M PMA | [188.5](#_bookmark223) |  | M | Yes [ ]  No [ ] |

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#### PICS proforma tables for Physical Medium Attachment (PMA) sublayer and 22

#### baseband medium, type 10BASE-T1M 23

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#### PCS Transmit 25

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| PCST1 | PCS Reset | [188.4.1](#_bookmark191) | See [188.4.1](#_bookmark191) | M | Yes [ ] |
| PCST2 | PCS Data Transmission Enable function | [188.4.2.1](#_bookmark193) | Conform to the PCS Transmit state diagram | M | Yes [ ] |
| PCST3 | Values of tx\_cmd variable | [188.4.2.2](#_bookmark195) | See [188.4.2.2](#_bookmark195) | M | Yes [ ] |
| PCST4 | PCS Transmit function scrambler polynomial | [188.4.2.8](#_bookmark204) | See [188.4.2.8](#_bookmark204) | M | Yes [ ] |
| PCST5 | PCS scrambler seed values | [188.4.2.8](#_bookmark204) | Never initialized to zeros | M | Yes [ ] |
| PCST6 | xmit\_max\_timer | [188.4.2.6](#_bookmark200) | Upon expiration, an even number of nibbles have been sent | M | Yes [ ] |

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#### PCS Receive 1

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| PCSR1 | PCS Receive function | [188.4.3.1](#_bookmark208) | Conform to the PCS Receive state diagram and associated variables | M | Yes [ ] |
| PCSR2 | Generation of RXD<3:0> to the MII | [188.4.3.8](#_bookmark217) | Descramble the 5B/4B decoded data stream and return the proper sequence of nibbles | M | Yes [ ] |
| PCSR3 | self-synchronizing descrambler | [188.4.3.8](#_bookmark217) | See [188.4.2.8](#_bookmark204) | M | Yes [ ] |
| PCSR4 | False Carrier supported | [188.4.3.7](#_bookmark214) | See [Figure 188–7](#_bookmark215) | O | Yes [ ] |

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#### PCS loopback 17

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| PCSL1 | PCS loopback | [188.4.4](#_bookmark220) | The PCS shall be placed in loopback mode when the loopback bit in MDIO register 3.0.14, defined  in 45.2.3.1.2, is set to one | MDIO: M | Yes [ ]  N/A[ ] |
| PCSL2 | PCS loopback function | [188.4.4](#_bookmark220) | The PCS shall accept data on the transmit path from the MII and return it on the receive path to the MII | M | Yes [ ] |
| PCSL3 | PHY receive circuitry isolation | [188.4.4](#_bookmark220) | The PHY receive circuitry shall be isolated from the network medium | M | Yes [ ] |
| PCSL4 | PHY transmit circuity isolation | [188.4.4](#_bookmark220) | The assertion of TX\_EN at the MII shall not result in the transmission of data on the network medium | M | Yes [ ] |

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#### Collision detection 1

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| CD1 | Detect collisions on the media during data transmission | [188.4.5](#_bookmark221) | When a transmission initiated locally results in a corrupted signal at the TCI, a collision is detected | M | Yes [ ]  N/A[ ] |
| CD2 | When collisions are detected | [188.4.5](#_bookmark221) | Assert the signal COL on the MII for the duration of the collision or until TX\_EN signal is FALSE | M | Yes [ ]  N/A[ ] |
| CD3 | CRS asserted during collision of two or more other stations | [188.4.5](#_bookmark221) | See [188.4.5](#_bookmark221) | M | Yes [ ]  N/A[ ] |
| CD4 | Sense when the media is busy | [188.4.6](#_bookmark222) | Assert the signal CRS on the MII as specified in 22.2.2.11 | M | Yes [ ]  N/A[ ] |

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#### Physical Medium Attachment (PMA) 20

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#### PMA function 22

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| PMA1 | PMA reset function | [188.5.1](#_bookmark225) | S[ee 188.5.1](#_bookmark225) | M | Yes [ ] |
| PMA2 | tx\_sym parameter value is the special 5B symbol 'I' | [188.5.2](#_bookmark226) | See [188.5.2](#_bookmark226) | M | Yes [ ] |
| PMA3 | receive SILENCE | [188.5.3](#_bookmark228) | PMA receive conveys symbol ‘I’ when no activity is detected on the line | M | Yes [ ] |

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#### PMA electrical specification 1

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| PMAE1 | Test modes | [188.6.2](#_bookmark234) | Implemented in PHY to allow testing transmitter electrical requirements | M | Yes [ ] |
| PMAE2 | Enable test modes | [188.6.2](#_bookmark234) | Enable by setting  bits 1.2299.15:13 as described in [45.2.1.236](#_bookmark96) when MDIO implemented; similar functionality provided otherwise | MDIO:M | Yes [ ]  N/A[ ] |
| PMAE3 | These test modes shall change only the data symbols provided to the transmitter circuitry and shall not alter the electrical and jitter characteristics of the transmitter and receiver from those of normal (non-test mode) operation | [188.6.2](#_bookmark234) |  | M | Yes [ ] |
| PMAE4 | Test mode 1 | [188.6.2](#_bookmark234) | When enabled, PHY repeatedly transmits DME encoded ones | M | Yes [ ] |
| PMAE5 | Test mode 2 | [188.6.2](#_bookmark234) | When enabled, PHY repeatedly transmits a positive differential voltage for 1.6 s followed by a negative differential voltage level for 1.6 s | M | Yes [ ] |
| PMAE6 | Test mode 3 | [188.6.2](#_bookmark234) | When test mode 3 is enabled, the PHY shall transmit continually a pseudo-random sequence of positive and negative voltage levels, generated by the scrambler defined in [188.4.2.8](#_bookmark204) and encoded using Differential Manchester Encoding (DME) as in [188.5.2](#_bookmark226) | M | Yes [ ] |
| PMAE7 | Test mode 4 | [188.6.2](#_bookmark234) | When enabled, PHY transmitter shall present a high impedance termination to the line as specified in [188.5.2](#_bookmark226) | M | Yes [ ]  N/A[ ] |
| PMAE8 | TX\_CLK | [188.6.3](#_bookmark235) | PHY to provide access to TX\_CLK | M | Yes [ ] |
| PMAE9 | AC coupling at TCI | [188.6.4](#_bookmark238) |  | M | Yes [ ] |
| PMAE10 | The transmitter shall meet the requirements of this subclause with a 50 ± 0.1% resistive differential load connected to the transmitter output | [188.6.4](#_bookmark238) | When both TC1 and TC2 are terminated, the 50 resistive differential load should be implemented as a 100  termination on each of TC1 and TC2. | M | Yes [ ]  N/A[ ] |
| PMAE11 | Transmitter electrical specifications shall be measured at both TC1 and TC2 | [188.6.4](#_bookmark238) |  | M | Yes [ ]  N/A[ ] |

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| PMAE12 | Transmitter output voltage | [188.6.4.1](#_bookmark239) | 1.0 V ± 20% peak-to-peak differential when measured on test mode 1 | M | Yes [ ] |
| PMAE13 | Transmitter output droop | [188.6.4.2](#_bookmark240) | Less than 30% when measured on test mode 2 | M | Yes [ ] |
| PMAE14 | Transmitter timing jitter | [188.6.4.3](#_bookmark242) | Less than 5 ns symbol-to- symbol jitter when measured on test mode 1 | M | Yes [ ] |
| PMAE15 | Transmit power spectral density | [188.6.4.4](#_bookmark243) | Between the upper and lower masks specified  in [Equation (188–1)](#_bookmark244) and [Equation (188–2)](#_bookmark245) when measured on test mode 3 | M | Yes [ ] |
| PMAE16 | A transmitter configured for test mode 4 | [188.6.4.5](#_bookmark247) | Presents at least the minimum parallel impedance across the PMA port of the TCI to meet the TCI specifications in [188.9.1](#_bookmark265) | M | Yes [ ] |
| PMAE17 | Receiver differential input signals | [188.6.5.1](#_bookmark249) | Can be verified with a frame error ratio less than 1 10–7 for 125 octet frames | M | Yes [ ] |
| PMAE18 | Alien crosstalk noise rejection | [188.6.5.2](#_bookmark250) | BER < 10–10 with an alien crosstalk noise of Gaussian distribution of magnitude  of –101 dBm/Hz and bandwidth of 40 MHz at the TCI | M | Yes [ ] |
| PMAE19 | PMA local loopback | [188.6.6](#_bookmark252) | The PMA shall be placed in loopback mode when the PMA local loopback bit in MDIO register 1.0.0, defined  in 45.2.1.1, or in MDIO register 1.2297.13, defined  in [45.2.1.234.5](#_bookmark87) is set to one | MDIO:O | Yes [ ]  No [ ]  N/A[ ] |
| PMAE20 | PMA local loopback | [188.6.6](#_bookmark252) | The PMA and PCS Receive functions pass the data decoded from the signal to the MII RX | MDIO:M | Yes [ ]  No [ ]  N/A[ ] |

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#### Mixing segment characteristics 1

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| MXS1 | Linear topology | [188.8](#_bookmark254) | with edge terminations and TCI’s where DTEs are attached | INS- MIX:M | Yes [ ] |
| MXS2 | Insertion loss | [188.8.1](#_bookmark256) | Measured between edge termination attachment points | INS- MIX:M | Yes [ ] |
| MXS3 | Return loss at each PMA port of each TCI | [188.8.2](#_bookmark258) | Measured with a reference impedance of 50  | INS- MIX:M | Yes [ ] |
| MXS4 | Return loss at edge termination attachments points | [188.8.2](#_bookmark258) | Measured with a reference impedance of 100  | INS- MIX:M | Yes [ ] |
| MXS5 | Mode conversion loss | [188.8.3](#_bookmark260) |  | INS- MIX:M | Yes [ ] |

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#### TCI specification 20

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| --- | --- | --- | --- | --- | --- |
| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| TCI1 | TCI insertion loss between TC1 and TC2 with simulated DTE loading | [188.9.1.1](#_bookmark266) | In each direction, measured with a reference impedance of 100  | M | Yes [ ] |
| TCI2 | TCI insertion loss at ports TC1 and TC2 with simulated DTE loading | [188.9.2](#_bookmark268) | In each direction, measured with a reference impedance of 100  | M | Yes [ ] |
| TCI3 | MDI line powering voltage tolerance | [188.9.3](#_bookmark271) | Up to 60 V dc with the source current limited to 2000 mA | M | Yes [ ] |
| TCI4 | MDI fault tolerance | [188.9.4](#_bookmark272) | Withstand without damage the application of a short circuit of any conductor to the other conductor of the same pair or ground potential. Normal operation resumes after all short circuits are removed. | M | Yes [ ] |

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#### Delay constraints 41

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| --- | --- | --- | --- | --- | --- |
| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| DC1 | Delay constraints | [188.11](#_bookmark280) | Comply with [Table 188–4](#_bookmark281) | M | Yes [ ] |

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1. **Multidrop Power over Ethernet (MPoE)** 1

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## Overview 4

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This clause defines the functional and electrical characteristics of two power entities, an MPoE Powered 6

Device (MPD) and an MPoE Power Sourcing Equipment (MPSE), for use with the 10BASE-T1M Physical 7

Layer. These entities allow devices to supply/draw power using the same cabling that is used for data 8

transmission. MPoE can provide a multidrop single pair Ethernet Physical Layer device with an interface to 9

both the power and data over the mixing segment. Alternatively, MPoE can be used to provide power over a 10

single pair multidrop wiring configuration. 11

12

This clause specifies the following: 13

1. The characteristics of an MPSE to add power to the cabling system. 14
2. The characteristics of an MPD's load on the power source and the cabling. 15
3. A method for determining the presence of one or more MPDs prior to applying power. 16

17

1. A method for applying and removing power from the mixing segment in a controlled manner. 18
2. A method for scaling supplied power back to the idle level when power is no longer requested or 19

required. 20

1. A method for MPDs and MPSEs to negotiate and allocate power. 21
2. Power fault sensing and recovery. 22

23

1. Requirements for adding an MPD to an already powered mixing segment. 24

25

#### Compatibility considerations 26

27

Compliant implementations of MPD and MPSE systems are defined as compatible at their respective 28

Multidrop Power Interfaces (MPIs) when used in accordance with the restrictions of this clause. Designers 29

are free to implement circuitry within the MPD and MPSE in an application-dependent manner provided 30

that the respective MPI specifications are satisfied. DTEs that incorporate compliant MPoE TCIs are 31

compatible with their respective Physical Layer standards. Such compatibility may require additional 32

specifications found within this clause (see [189.6.2).](#_bookmark375) 33

34

#### Relationship of MPoE to the IEEE 802.3 architecture 35

36

MPoE is an optional power entity to be used in conjunction with supported multidrop single pair Ethernet 37

Physical Layers. [Figure 189–1](#_bookmark308) depicts the positioning of MPoE. The MPSE and MPD are positioned within 38

separate DTEs. The power is applied to the Multidrop Power Interface (MPI) (see [1.4.427b).](#_bookmark2) Compliance is 39

specified at the MPI (see [Figure 189–1](#_bookmark308)). An MPSE or MPD may or may not be co-located with a DTE, and 40

the power may be provided over the same pairs as the data or over dedicated pairs with power only. The 41

interface of the power entity to the medium is the MPI, with connection points MP1 and MP2 to the power 42

trunk. When the power is provided over the same pairs as data, the MPI and the TCI are the same connection 43

to the medium and the MPI must also meet the requirements for the TCI needed for the PHY (see, e.g., 44

[188.9).](#_bookmark262) However, when data and power are carried on separate conductors, the MPI may be separate from 45

the TCI and the related TCI requirements do not apply. 46

47

#### Conventions in this clause 48

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The body of this clause contains state diagrams including definitions of variables, constants, and functions. 50

Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails. 51

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#### State diagram notation 1

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The conventions of 21.5 are adopted with the extension that some states in the state diagrams use an 3

IF-THEN-ELSE-END construct to condition which actions are taken within the state. If the logical 4

expression associated with the IF evaluates TRUE, then all the actions listed between THEN and ELSE will 5

be executed. In the case where ELSE is omitted, the actions listed between THEN and END will be 6

executed. If the logical expression associated with the IF evaluates FALSE, then the actions listed between 7

ELSE and END will be executed. After executing the actions listed between THEN and ELSE, between 8

THEN and END, or between ELSE and END, the actions following the END, if any, will be executed. 9

10

#### State diagram timer specifications 11

12

All timers operate in the manner described in 40.4.5.2. 13

14

#### Service specifications 15

16

The method and notation used in the service specification follows the conventions of 1.2.2. 17

18

100 

MP1

node 1

MPI

MPSE

or MPD

MP2

MPI

MP1

node 2

MPI

MPSE

or MPD

MP2

MPI

MP1

node x

MPI

MPSE

or MPD

MP2

MPI

19

20

21

22

100  23

24

25

26

27

28

29

NOTE – The MPI may not be exposed. If it is not 30

exposed, specified values are calculated from 31

values observed at MP1 and MP2. 32

#### Figure 189–1—Mixing segment and reference points for power 33

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## Mixing segment 37

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The mixing segment consists of cable, nodes, and terminations (see [Figure 189–1](#_bookmark308)). 100 Ω terminations are 39

connected at the ends of the mixing segment and must be AC coupled. The dc loop resistance of the cable 40

(excluding connectors and attached DTEs) shall be less than or equal to 4 Ω. 41

42

This resistance budget is based on supporting up to 17 in-line nodes (1 MPSE and 16 MPDs). Each DTE, 43

including mated connectors and compensation components, adds up to 100 m Ω to the loop resistance. 44

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## System type power requirements 1

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MPSEs and MPDs are categorized by their system type. These system types and the relevant electrical 3

specifications are shown in [Table 189–1](#_bookmark312). An MPSE may transition between types during IDLE (see 4

[Figure 189–3](#_bookmark327) and [Figure 189–4](#_bookmark329)). 5

6

MPDs consume integer units of power called “unit loads”. 7

8

For Type 0 MPDs, one unit load represents 1W. For Type 1 MPDs, one unit load represents 9

2W. An MPD compatible with both Type 0 and Type 1 is designated Type 0/1 . For Type 0/1 MPDs, one unit load represents 1 W. See 189.5.1 for further discussion on MPD types. 10

11

A mixing segment can support up to 16 unit loads. Each MPD is allocated a minimum of 1 unit load and 12

may consume no more than 16 unit loads. The MPD system type and unit load level should be clearly 13

indicated so users can track loading on a mixing segment. The sum of unit load levels on a mixing segment 14

shall not exceed 16. 15

16

17

#### Table 189–1—System power types 18

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|  |  |  |  |
| --- | --- | --- | --- |
|  | **30V Max MPSE** | **50V Max MPSE** | **Units** |
| System type | 0 | 1 |  |
| VMPSE max | 30 | 50 | V |
| VMPSE min | 26 | 45 | V |
| VMPD min | 16 | 34 | V |
| IMPSE min | 1000 | 1000 | mA |
| PMPSE min | 26 | 45 | W |
| PMPD\_1U max | 1 | 2 | W |

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## Multidrop Power Sourcing Equipment (MPSE) 35

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The MPSE provides power to MPDs. The MPSE's main functions are as follows: 37

* + 1. To search the mixing segment for at least one available MPD. 38

39

* + 1. To supply power to one or more MPDs connected to the mixing segment. 40
    2. To monitor the power applied to a mixing segment. 41
    3. To apply and remove power from the mixing segment in a controlled manner. 42
    4. To sense, react to, and recover from system faults. 43

44

* + 1. To remove power when no longer required, returning to the idle state. 45

46

An MPSE is specified by its electrical and logical behavior as seen at the MPSE MPI. 47

48

* + 1. **MPSE types** 49

50

An MPSE shall comply with the voltage and power requirements listed in [Table 189–1](#_bookmark312) for the relevant type. 51

52

53

54

#### MPSE pin assignments 1

2

An MPSE provides power via a single two-conductor connection. [Table 189–2](#_bookmark316) in conjunction with 3

[Figure 189–1](#_bookmark308) illustrates the MPSE pinout. An MPSE shall conform to the pinout of [Table 189–2](#_bookmark316) and 4

provide a single polarity. 5

6

7

#### Table 189–2—MPSE pinout 8

9

|  |  |  |
| --- | --- | --- |
| **Conductor** | **MPSE** | **PMA signal** |
| 1 | Positive VMPSE | BI\_DA+ |
| 2 | Negative VMPSE | BI\_DA- |

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16

* + 1. **MPSE MPI** 17

18

MPSEs supply power to the mixing segment through the MPI. See [Figure 189–](#_bookmark318)2. This standard assumes one 19

MPSE per mixing segment. More than one MPSE per mixing segment is beyond the scope of this standard. 20

21

Current at an MPSE MPI is defined as positive when current flows out of the higher voltage pin of the MP1 22

or MP2 connection and flows into the lower voltage pin of the same MP1 or MP2 connection, respectively. 23

24

Current at an MPSE MPI is defined as negative when current flows into the higher voltage pin of the MP1 or 25

MP2 connection and flows out of the lower voltage pin of the same MP1 or MP2 connection, respectively. 26

27

For compliance, MPSE current is measured as the sum of MPI currents, MP1+MP2. Current is measured as 28

the sum of both higher voltage pins on MP1 and MP2 or both lower voltage pins on MP1 and MP2. 29

30

For compliance, voltage specifications shall be met at both MP1 and MP2 independently. When the MPI is 31

not accessible, compliance to voltage specifications is met at MP1 and MP2. If the specification calls for the 32

voltage to be above a value, or below a value, both MP1 and MP2 must meet the criteria. Current is 33

measured as the sum of both higher voltage pins on MP1 and MP2 or both lower voltage pins on MP1 and 34

MP2. 35

36

V(A,B) > 0 V(C,D) > 0 37

NEGATIVE CURRENT A

NEGATIVE B

MPI

POSITIVE 38

1. CURRENT 39

40

41

1. POSITIVE 42

CURRENT

MP1 MP2

MPI

CURRENT 43

44

45

MPSE DTE

NOTE – MPSE MPI may not be 46

exposed. If it is not exposed, 47

limits are calculated from values 48

at MP1 and MP2. 49

50

#### Figure 189–2—Current at the MPSE MPI 51

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#### MPSE state diagram 1

2

The MPSE shall implement the behavior of the state diagram shown in [Figure 189–3](#_bookmark327) and [Figure 189–4.](#_bookmark329) 3

Prior to application of full operating voltage, the MPSE determines the presence of at least one valid MPD 4

(see [Table 189–](#_bookmark331)3). An MPSE may apply full operating voltage if it is able to successfully discover a voltage- 5

compatible MPD and does not apply full operating voltage if an invalid discovery signature is measured (see 6

[Table 189](#_bookmark332)–4). 7

8

After full operating voltage has been applied, the MPSE removes full operating voltage in response to a 9

command from the management entity that results in mpse\_enable being set to disable. For example, the 10

management entity could monitor the link to determine if at least one MPD remains attached, and there have 11

been no changes in the network topology. 12

13

Additionally, while voltage is applied the MPSE monitors the current drawn and removes power if it detects 14

an overload (see [189.4.8](#_bookmark337)), short-circuit or other fault (see [189.4.9](#_bookmark338)), or for the absence of TPS (see [189.4.10](#_bookmark341)). 15

16

* + - 1. **Conventions** 17

18

The notation used in the state diagram follows the conventions of state diagrams as described in 145.2.5.2. 19

20

* + - 1. **Variables** 21

22

The MPSE state diagram uses the following variables: 23

discover\_fault 24

25

A variable indicating if IDiscovery measured by the MPSE during the most recent discover\_high 26

or discover\_low state is equal to or greater than IDiscovery\_LIM as defined in [Table 189–3](#_bookmark331). This 27

variable is set per this description. 28

Values: FALSE: Measured IDiscovery was less than IDiscovery\_LIM during 29

most recent discover\_high or discover\_low state. 30

TRUE: Measured IDiscovery was equal to or greater than IDiscovery\_LIM during 31

most recent discover\_high or discover\_low state. 32

discover\_low\_tare\_var 33

A variable that stores the baseline IDiscovery when MPDs are receiving power from the discov- 34

ery algorithm, but not issuing a discovery response. This baseline IDiscovery will be compared 35

against later discovery\_low IDiscovery measurements to determine which types of MPDs are 36

connected to the mixing segment. 37

mark\_number 38

39

A variable that counts the mark events in a single discovery cycle. This variable is reset in the 40

IDLE state, and incremented at each high mark event. 41

mpd\_type0\_discovered 42

A variable that indicates at least one valid Type 0 MPD is connected to the 43

mixing segment. 44

Values: FALSE: No valid Type 0 MPDs are connected to the mixing 45

segment. 46

TRUE: At least one valid Type 0 MPD is connected to the 47

mixing segment. 48

49

mpd\_type1\_discovered 50

A variable that indicates at least one valid Type 1 MPD is connected to the 51

mixing segment. 52

Values: FALSE: No valid Type 1 MPDs are connected to the mixing 53

segment. 54

TRUE: At least one valid Type 1 MPDs is connected to the 1

mixing segment. 2

mpd\_types01\_discovered 3

A variable that indicates at least one valid Type 0/1 MPD is con- 4

nected to the mixing segment. 5

Values: FALSE: No Type 0/1 MPDs are connected to the 6

mixing segment. 7

TRUE: At least one valid Type 0/1 MPD is connected 8

to the mixing segment. 9

10

mpi\_powered 11

A variable that controls the circuitry that the MPSE uses to power the MPI. 12

Values: FALSE: The circuitry that applies operating power to the MPI is disabled. 13

TRUE: The circuitry that applies operating power to the MPI is enabled. 14

mpse\_enable 15

A variable that selects MPSE operation. This variable may be set by the MPSE at any time. 16

Values: FALSE: All MPSE functions disabled (behavior is as if there was no MPSE 17

functionality). 18

TRUE: Normal MPSE operation. 19

20

mpse\_ready 21

A variable that is asserted in an implementation-dependent manner. This variable may be set 22

by the MPSE at any time. 23

Values: FALSE: The MPSE is not ready to discover the mixing segment. 24

TRUE: The MPSE is ready to discover the mixing segment. 25

overload\_detected 26

A variable indicating if the MPSE output current has been in an overload condition; see 27

[189.4.8](#_bookmark337). 28

Values: FALSE: The MPSE has not detected an overload condition. 29

TRUE: The MPSE has detected an overload condition. 30

31

power\_available 32

A variable that is set in an implementation-dependent manner when the MPSE is no longer 33

capable of sourcing sufficient power to support the attached MPD load. 34

Values: FALSE: MPSE is no longer capable of sourcing power to the MPD load. 35

TRUE: MPSE is capable of continuing to source power to the MPD load. 36

power\_stable 37

A variable that is asserted when the MPSE completes inrush and is ready to source full operat- 38

ing power to MPD loads. 39

Values: FALSE: The MPSE is either not applying full operating voltage or has begun 40

applying full operating voltage but is still in the INRUSH state. 41

TRUE: The MPSE has begun steady-state operation and is ready to enter the 42

POWER\_ON state. 43

44

short\_circuit\_detected 45

A variable indicating if the MPSE output has been in a short circuit condition; see [189.4](#_bookmark338).9. 46

This variable is set per this description. 47

Values: FALSE: The MPSE has not detected a short circuit condition. 48

TRUE: The MPSE has detected a short circuit condition. 49

50

* + - 1. **Timers** 51

52

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops 53

counting upon entering a state where "stop\_x\_timer" is asserted. 54

discovery\_backoff\_timer 1

A timer used to enforce the time between discovery cycles. See [Table 189–3](#_bookmark331). 2

3

mark\_timer 4

A timer used to delay measurement of the mark current after applying a high mark voltage. See 5

[Table 189–3.](#_bookmark331) 6

7

measure\_timer 8

A timer used to delay measurement of the discovery low event current after applying a low 9

event voltage. See [Table 189–3](#_bookmark331). 10

11

mpse\_inrush\_timer 12

A timer used to limit the duration of the inrush event. See [Table 189–5.](#_bookmark335) 13

tdiscover\_high\_timer 14

A timer used to limit the discovery\_high event time. See [Table 189–3.](#_bookmark331) 15

16

tdiscover\_low\_timer 17

A timer used to limit the discovery\_low event time. See [Table 189–](#_bookmark331)3. 18

ted\_timer 19

A timer used to regulate a subsequent attempt to power a MPD after an error condition causes 20

power removal. See [Table 189–5](#_bookmark335). 21

22

ttpsdo\_timer 23

A timer used to monitor the dropout of the TPS. See [189.4.10.1](#_bookmark342) and [Table 189–5](#_bookmark335). 24

25

* + - 1. **Functions** 26

27

The variable formed by the function name appended with "\_done" is used to indicate when the function has 28

completed. This variable is set to FALSE when the function is called and is set to TRUE once the function is 29

complete and its output variables are valid. 30

check\_discovery\_all 31

This function evaluates the results of the most recent discovery mark event. The measured 32

33

IDiscovery is compared against IMark from the previous discovery\_high\_mark event to 34

determine if MPDs are present (see [Table 189](#_bookmark331)–3). This function returns the following variable: 35

mpd\_discovered: This variable indicates the presence or absence of a valid MPD on the 36

mixing segment. 37

Values: open\_circuit: The MPSE has detected an open circuit. 38

valid: The MPSE has discovered at least one MPD is connected to the mixing 39

segment. 40

check\_discovery\_type 41

This function determines if MPDs are responding to the slot by subtracting the variable 42

discover\_low\_tare\_var from the measured IDiscovery to determine if an MPD is responding to 43

this discovery\_low event. This function returns the following variable: 44

45

mpd\_type\_discovered: This variable indicates the presence or absence of a valid MPD corre- 46

sponding to the discovery slot being probed. 47

Values: TRUE: At least one MPD responded to the most recent discovery event. 48

FALSE: No MPDs responded to the most recent discovery event. 49

do\_discovery\_eval 50

This function evaluates the results from the previous discovery states to determine if at least 51

one MPD is requesting power that is compatible with the MPSE's system type. 52

53

This function returns the following variable: 54

discover\_compatible\_mpd: 1

Values: TRUE: At least one MPD is requesting power that is compatible with the MPSE 2

system type. 3

FALSE: No MPDs are requesting power that is compatible with the MPSE 4

system type. 5

do\_discovery\_high 6

This function returns the following variables: 7

8

discover\_short: A variable indicating if IMark measured by the MPSE during do\_discov- 9

ery\_high is greater than IMark\_short as defined in [Table 189–3](#_bookmark331). This vari- 10

able is set per this description. 11

Values: FALSE: Measured IMark is less than IMark\_short during do\_discovery\_high. 12

TRUE: Measured IMark is equal to or greater than IMark\_short during 13

do\_discovery\_high. 14

15

discover\_high\_var: Measured IMark during the most recent discovery\_high\_mark event. 16

do\_discovery\_low 17

This function measures IDiscovery. This function returns the following variable: 18

19

discover\_low\_val: Measured IDiscovery during the most recent discovery\_low event. 20

do\_MPSE\_reset 21

This function produces the reset event voltage (VMPSE\_reset) at the MPI. 22

present\_low 23

24

This function produces the discovery low voltage, VDiscovery, as defined in [Table 189–](#_bookmark331)3. 25

present\_mark 26

This function produces the discovery mark voltage, VMark, as defined in [Table 189–3.](#_bookmark331) 27

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#### State diagrams

!mpse\_enable

D

|  |  |
| --- | --- |
| DISABLED | |
| mpi\_powered FALSE discover\_fault FALSE | |
|  | mpse\_enable |

mpse

|  |  |
| --- | --- |
| IDLE | |
| discover\_short FALSE discover\_compatible\_mpd FALSE mpd\_type0\_discovered FALSE mpd\_type1\_discovered FALSE mpd\_types01\_discovered FALSE mark\_number 0 | |
| \_ready | B |

|  |  |
| --- | --- |
| HIGH\_MARK | |
| present\_mark  start tdiscover\_high\_timer start mark\_timer mark\_number++ | |
| \_timer\_done |  |

mark

DISCOVERY\_HIGH\_MARK

do\_discovery\_high

1

discover\_fault \* 2

A

mpse\_enable 3

4

5

|  |  |  |
| --- | --- | --- |
|  | BACKOFF | |
| start discovery\_backoff\_timer do\_MPSE\_reset | |
| discovery\_backoff\_timer\_done | |  |
|  | | |

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22

|  |  |
| --- | --- |
| DISCOVERY\_LOW\_PRESENT | |
| present\_low  start tdiscover\_low\_timer start measure\_timer | |
|  | measure\_timer\_don |

23

24

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e 27

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29

DISCOVERY\_LOW 30

do\_discovery\_low 31

32

33

tdiscover\_high\_timer\_done \* discover\_short

A

mpd\_discovered = open\_circuit

|  |  |  |
| --- | --- | --- |
| DISCOVERY\_LOW\_ALL | | |
| check\_discovery\_all | | |
|  |  |  |
| A | |

tdiscover\_high\_timer\_done \* (!discover\_short)

tdiscover\_low\_timer\_done \* (mark\_number = 1)

tdiscover\_low\_timer\_done \* (mark\_number = 2)

|  |  |
| --- | --- |
| DISCOVERY\_LOW\_TARE | |
| discover\_low\_tare\_var discover\_low\_val | |
| id | UCT |

mpd\_discovered = val

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35

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C 37

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tdiscover\_low\_timer\_done \* (mark\_number > 2)

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B

#### Figure 189–3—Top level MPSE state diagram, part a 54

mark\_nu

A

mpse\_inrush\_timer\_done \*

1

2

C

3

4

5

|  |  |  |
| --- | --- | --- |
| DISCOVERY\_LOW\_TYPE | | |
| check\_discovery\_type  IF (mark\_number = 3) THEN  mpd\_type0\_discovered mpd\_type\_discovered ELSE IF (mark\_number = 4) THEN  mpd\_type1\_discovered mpd\_type\_discovered ELSE IF (mark\_number = 5) THEN  mpd\_types01\_discovered mpd\_type\_discovered  END END END | | |
| mber < 5 |  |  |
| B | |

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mark\_number = 5 15

16

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|  |  |  |  |
| --- | --- | --- | --- |
|  | DISCOVERY\_LOW\_EVAL | | |
| do\_discovery\_eval | | |
| !discover\_compatible\_mpd | |  |  |
|  | | |

25

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28

discover\_compatible\_mpd 29

30

31

32

|  |  |  |  |
| --- | --- | --- | --- |
|  | INRUSH | | |
| start mpse\_inrush\_timer mpi\_powered TRUE | | |
|  | |  | mpse\_inrush\_ti |
| power\_stable  POWER\_ON  ttpsdo  overload\_detected + A short\_circuit\_detected +  !power\_available | | | |

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mer\_done \* 36

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\_timer\_done 42

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|  |  |
| --- | --- |
| ERROR\_DELAY | |
| start ted\_timer mpi\_powered FALSE | |
| ted\_timer\_done |  |

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#### Figure 189–4—Top level MPSE state diagram, part b 54

#### Discovering the presence of an MPD before powering 1

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The ability for the MPSE to query all attached MPDs to determine the assortment of system types present on 3

the link is called discovery. Discovery also serves the function of checking that the link is clear of faults 4

before applying power. 5

6

Discovery consists of a series of discover high and discover low events as defined in the state diagram in 7

[Figure 189–3](#_bookmark327) and [Figure 189–4](#_bookmark329). 8

9

When the MPSE is in a HIGH\_MARK or DISCOVERY\_HIGH\_MARK state, as shown in the state diagram 10

of [Figure 189–3](#_bookmark327) and [Figure 189–4,](#_bookmark329) the MPSE supplies VMark voltage to the TCI subject to the 11

TDiscovery\_high timing specification. The MPSE waits TMark\_measure between applying the mark event 12

voltage at the entrance of HIGH\_MARK before measuring the mark event current IDiscovery in 13

DISCOVERY\_HIGH\_MARK. TMark\_measure and TDiscovery\_high are referenced from the application of 14

VMark min to ignore initial transients. If the current IDiscovery measured in a DISCOVERY\_HIGH\_MARK 15

state exceeds IMark\_short the MPSE returns to the BACKOFF state. 16

17

When the MPSE is presenting a discover low event voltage in any of the DISCOVERY\_LOWx states (i.e., 18

DISCOVERY\_LOW\_PRESENT, DISCOVERY\_LOW, DISCOVERY\_LOW\_ALL, DISCOVERY- 19

\_LOW\_TARE, DISCOVERY\_LOW\_TYPE, or DISCOVERY\_LOW\_EVAL), as shown in the state dia- 20

gram of [Figure 189–3](#_bookmark327) and [Figure 189–](#_bookmark329)4, the MPSE supplies VDiscovery voltage to the TCI subject to the 21

TDiscovery\_low timing specification. The MPSE waits TDiscover\_measure between the entrance of a DISCOV- 22

ERY\_LOW\_PRESENT state and measurement of the discovery event current, IDiscovery in the DISCOV- 23

ERY\_LOW state. TDiscover\_measure is referenced from the application of VDiscovery max to ignore initial 24

transients. 25

26

The MPSE shall limit current to IDiscovery\_LIM during all discovery events, DISCOVERY\_LOWx and 27

DISCOVER\_HIGH\_MARKx. 28

29

If the MPSE returns to BACKOFF, it maintains the MPI voltage at VMPSE\_reset for TDiscovery\_backoff before 30

starting a new discovery cycle. 31

32

The MPSE waits at least TBackoff before reattempting discovery. An MPSE may successfully complete 33

discovery, but then opt not to power the link. 34

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Unless acting as an MPD, an MPSE shall present an invalid MPD discovery signature with one of the 36

attributes as defined in [Table 189–4](#_bookmark332). 37

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#### Table 189–3—MPSE discovery parameters 1

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| --- | --- | --- | --- | --- | --- | --- |
| **Item** | **Parameter** | **Symbol** | **Min** | **Max** | **Units** | **Additional Information** |
| 1 | Discovery high mark voltage | VMark | 16.1 | 19.1 | V |  |
| 2 | Discovery low voltage | VDiscovery | 7.4 | 11.9 | V |  |
| 3 | Discovery current limit | IDiscovery\_LIM | 50 | 100 | mA |  |
| 4 | Discovery high event time | TDiscovery\_high | 7 | 44 | ms |  |
| 5 | Discovery low event time | TDiscovery\_low | 20 | 44 | ms |  |
| 6 | Discovery backoff time | TBackoff | 150 | - | ms |  |
| 7 | Mark short circuit threshold | IMark\_short | 3 | 4 | mA |  |
| 8 | Discovery\_all MPD present range | IMPD\_present | 0.8 | 40 | mA | IDiscovery - IMark |
| 9 | MPD type present | IType\_presen | 0.8 | 40 | mA | IDiscovery - ITare |
| 10 | Mark measurement delay | TMark\_measure | 5 | - | ms |  |
| 11 | Discovery measure- ment delay | TDiscover\_mea- sure | 6.5 | - | ms | Based on Mark- Discover fall time (10nF Cpd) |
| 12 | Discovery reset | VMPSE\_reset | 0 | 2.8 | V |  |

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#### Table 189–4—Discovery rejection criteria 35

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| --- | --- | --- | --- | --- | --- |
| **Item** | **Parameter** | **Symbol** | **Min** | **Max** | **Units** |
| 1 | Reject discovery - short circuit | Ibad | 30 | - | mA |
| 2 | Reject discovery - open circuit | Iopen | - | 75 | A |

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#### MPSE output requirements 1

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When the MPSE provides power to the MPSE MPI, it shall conform to the electrical limits in [Table 189–5.](#_bookmark335) 3

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#### Table 189–5—PSE output requirements 6

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Item** | **Parameter** | **Symbol** | **Unit** | **Min** | **Max** | **Type** | **Additional Information** |
| 1 | DC output voltage during POW- ER\_ON state | VMPSE | V | 26 | 30 | 0 |  |
|  | 45 | 50 | 1 |  |
| 2 | Continuous output capability in POWER\_ON state | PMPSE | W | 26 | 100 | 0 |  |
| 45 | 100 | 1 |  |
| 3 | Output slew rate  dV/dt |  | V/ms | - | 9.5 | ALL |  |
| 4 | Output current - at short circuit condi- tion | ILIM | A | 1.1 | 1.4 | ALL |  |
| 5 | Short-circuit time limit | TLIM | ms | 50 | 75 | ALL |  |
| 6 | Inrush time | TInrush | ms | 10 | 20 | ALL |  |
| 7 | MPD maintain power signature dropout time limit | TTPSDO | ms | 320 | 400 | ALL |  |
| 8 | PD TPS time for validity | TTPS | ms | 6 | - | ALL |  |
| 9 | DC TPS current | IHOLD | mA | 4 | 9 | ALL |  |
| 10 | Error delay timing | TED | ms | 750 | - | ALL |  |
| 11 | Overload current | ICUT | A | PMPSE/ VMPSE | - | ALL |  |
| 12 | Overload time limit | TCUT | ms | 50 | 70 | ALL |  |

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#### Continuous output power in POWER\_ON state 42

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PMPSE min is the minimum continuous power that the MPSE is capable of supplying as defined in 44

[Table 189–5.](#_bookmark335) External safety requirements limit the power an MPSE can supply. Often this value is 45

100 W max, but an MPSE designer is encouraged to refer to the safety standards that will govern the desired 46

installation (i.e., the target market for a given MPSE). 47

48

#### Overload current 49

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If the current exceeds ICUT for longer than TCUT, the MPSE may remove power. The cumulative duration of 51

TCUT is measured using a sliding window of 1 second width. 52

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#### Short circuit current 1

2

During operation in the INRUSH and POWER\_ON states, the MPSE shall limit the current to ILIM for a 3

duration of up to TLIM in order to account for MPSE dV/dt transients at the MPI as defined in [Table 189–5.](#_bookmark335) 4

If IMPSE exceeds ILIM min during the POWER\_ON state, the MPSE output voltage may drop below 5

VMPSE min. 6

7

#### MPSE power removal 8

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While the MPSE is operating in POWER\_ON, full operating voltage shall be removed from the MPI for any 10

of the following reasons: 11

* in the absence of the MPD TPS, 12
* if overload\_detected is TRUE, 13

14

* if short\_circuit\_detected is TRUE, 15
* if commanded to do so by a management entity. 16

17

#### 189.4.10.1 MPSE detection of MPD Transmit Power Signature (TPS) 18

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TPS allows MPDs to minimize power consumption, for example, in sleep states. By sensing the presence of 20

TPS, an MPSE can tell that there are active MPDs on the mixing segment, even if they are consuming 21

minimal power. TPS is defined as being present in the POWER\_ON state when IMPSE is greater than or 22

equal to IHold max for a minimum of TTPS as defined in [Table 189–5.](#_bookmark335) TPS may be defined as present or 23

absent in the POWER\_ON state if IMPSE is in the range of IHold. TPS shall be defined as absent in the 24

POWER\_ON state if IMPSE is less than or equal to IHold min. Power is removed from the MPI when TPS has 25

been absent for a duration greater than TTPSDO. 26

27

The MPSE shall not consider TPS absent and should not remove power when IMPSE is greater than or equal 28

to IHold max continuously for at least TTPS every TTPS + TTPSDO, as defined in [Table 189–](#_bookmark335)5, except as 29

defined for entry to the ERROR\_DELAY state in [Table 189–4](#_bookmark329). This allows an MPD to minimize its power 30

consumption. 31

32

## Multidrop Powered Device (MPD) 33

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An MPD is the portion of a device that is either drawing power or requesting power by participating in the 36

MPD discovery algorithms. A device that is capable of becoming an MPD may have the ability to draw 37

power from an alternate power source. An MPD requiring power from the MPI may simultaneously draw 38

power from an alternate power source. 39

40

An MPD is specified at the point of physical connection to the trunk. Limits defined for an MPD are 41

specified at the MPD MPI. If the MPD MPI is not exposed, values are calculated from observable voltages 42

and currents at MP1 and MP2. 43

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#### MPD system types 45

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MPDs can be characterized as Type 0, Type 1, or Type 0/1. 47

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Type 0 MPDs receive power from Type 0 MPSEs only. Type 1 MPDs receive power from Type 1 MPSEs 49

only. Type 0/1 MPDs receive power from either Type 0 MPSEs or Type 1 MPSEs. 50

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* + 1. **MPD MPI** 1

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An MPD may receive power in two polarities, Polarity A and Polarity B. MPDs are insensitive to the 3

polarity of the power supply and shall be able to operate per the Polarity A column and the Polarity B 4

column in [Table 189–](#_bookmark346)6. 5

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#### Table 189–6—MPD pinout 8

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| --- | --- | --- |
| **Conductor** | **Polarity A** | **Polarity B** |
| 1 | Positive VMPD | Negative VMPD |
| 2 | Negative VMPD | Positive VMPD |

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MPDs are current sinks. See [Figure 189–5.](#_bookmark347) Current at an MPD MPI is defined as positive when current 17

flows into the higher voltage pin of an MPI connection and flows out of the lower voltage pin of the same 18

connection. 19

20

Current at an MPD MPI is defined as negative when current flows out of the higher voltage pin of an MPI 21

connection and flows into the lower voltage pin of the same connection. 22

23

For compliance, MPD current is measured as the sum of MPI currents, MP1+MP2. Current is measured as 24

the sum of both higher voltage pins on MP1 and MP2, or both lower voltage pins on MP1 and MP2. 25

NOTE - One of the currents on MP1 or MP2 will be positive and the other will be negative; making this "sum" a 26

difference. The current used by the MPD lowers the current supplied to the output MP feeding the rest of the MPDs that 27

follow in the mixing segment. 28

29

V(A,B) > 0 V(C,D) > 0 30

POSITIVE CURRENT A

POSITIVE B CURRENT

MPI

NEGATIVE 31

1. CURRENT 32

33

1. NEGATIVE 34

CURRENT 35

MP1 MP2

MPI

MPSD DTE

36

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NOTE – MPD MPI may not be 39

exposed. If it is not exposed, 40

limits are calculated from values

at MP1 and MP2. 41

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#### Figure 189–5—Current at an MPD MPI 44

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#### MPD state diagram 46

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The MPD shall implement the behavior of the state diagram shown in [Figure 189–](#_bookmark356)6, [Figure 189–7](#_bookmark357), and 48

[Figure 189–](#_bookmark359)8. 49

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* + - 1. **Conventions** 51

52

The notation used in the state diagram follows the conventions of state diagrams as described in 145.2.5.2. 53

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#### Constants 1

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IInrush\_MPD\_max 3

The maximum MPD inrush current IInrush\_MPD max (see [Table 189–9).](#_bookmark364) 4

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VDiscovery\_th 6

Mark discovery threshold voltage (see [Table 189–7](#_bookmark361)) 7

8

VReset\_MPD\_max 9

The maximum MPD reset voltage VReset\_MPD max (see [Table 189–7](#_bookmark361)). 10

VReset\_th 11

Reset voltage threshold (see [Table 189–7](#_bookmark361)). 12

13

Vtype0\_th 14

Threshold between discovery and type 0 operating region. 15

Vtype1\_th 16

Threshold between Type 0 operating region and Type 1 operating region. 17

18

* + - 1. **Variables** 19

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The MPD state diagram uses the following variables: 21

dte\_power\_required 22

A variable indicating that the MPD is enabled and should request power from the MPSE by 23

participating in the discovery protocol, and when the MPSE sources power to apply the TPS to 24

keep the MPSE sourcing power. This variable may be set by the MPD at any time. 25

Values: FALSE: MPD functionality is disabled. 26

TRUE: MPD functionality is enabled. 27

28

mpd\_reset 29

An implementation-specific variable that unconditionally resets the MPD state diagram to 30

OFFLINE. This variable may be set by the MPD at any time. 31

Values: FALSE: The device has not been reset. 32

TRUE: The device has been reset. 33

mpd\_type 34

A variable indicating the MPD type. 35

Values: type0: The MPD supports only Type 0. 36

type1: The MPD supports only Type 1. 37

types01: The MPD supports both Type 0 and Type 1. 38

39

present\_sig 40

Controls presenting the current presented (see [Table 189–7](#_bookmark361) and [Table 189](#_bookmark364)–9) by the MPD. 41

Values: IDLE: The MPD presents IMPD\_idle at the MPI. 42

MARK: The MPD presents IMPD\_mark at the MPI. 43

DISCOVERY:The MPD presents IMPD\_discover at the MPI. 44

INRUSH: The MPD presents IInrush\_MPD at the MPI. 45

PON: The MPD current at the MPI is limited by PMPD. 46

DISABLED:The MPD presents IMPD\_Disabled at the MPI. 47

present\_mismatch\_indication 48

Controls presenting an indication that an MPD type is mismatched to the MPSE type on the 49

mixing segment 50

Values: 51

FALSE: The MPD does not indicate a type mismatch 52

TRUE: The MPD indicates a type mismatch 53

54

present\_mpi\_power 1

Values: FALSE: The MPD is disabled or not ready to consume full power from the MPI 2

TRUE: The MPD is enabled and ready to consume full power from the MPI 3

present\_tps 4

Controls applying the Transmit Power Signature TPS (see [Table 189–1](#_bookmark368)0) to the MPI. 5

Values: FALSE: The TPS is not to be applied to the MPI. 6

TRUE: The TPS is to be applied to the MPI. 7

8

VMPD 9

Voltage at the MPD MPI (see [Table 189–9](#_bookmark364)). 10

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* + - 1. **Timers** 12

13

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops 14

counting upon entering a state where "stop\_x\_timer" is asserted. 15

inrush\_timer 16

A timer used to prevent full load power draw while the MPD is in the inrush state. 17

18

See TInrush in [Table 189–9](#_bookmark364) for duration. 19

mark\_timer 20

A timer used to hold off inrush of an MPD during the mark state. See TMark in [Table 189–9](#_bookmark364) for 21

duration. 22

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#### State diagrams

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mpd\_reset + !dte\_power\_required 3

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(VMPD < VReset\_MPD\_max) \*

!mpd\_reset \* dte\_power\_required

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|  |  |
| --- | --- |
| OFFLINE | |
| present\_sig IDLE present\_tps FALSE present\_mpi\_power FALSE  present\_mismatch\_indication FALSE | |
|  | !mpd\_reset \* dte\_power (VMPD > VDiscovery\_th) |

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\_required \* 15

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DO\_MARK2

present\_sig MARK start mark\_timer

DO\_MARK3

present\_sig MARK start mark\_timer

DO\_MARK1

present\_sig MARK start mark\_timer

DO\_DISCOVERY1

present\_sig DISCOVERY

mark\_timer\_done \* (VMPD ≥ VDiscovery\_th)

VMPD < VDiscovery\_th

VMPD > VDiscovery\_th

VMPD < VReset\_th

VMPD < VDiscovery\_th

mark\_timer\_done \* (VMPD ≥ VDiscovery\_th)

VMPD < VDiscovery\_th

mark\_timer\_done \* (VMPD ≥ VDiscovery\_th)

C

A

B

**Figure 189–6—Top level MPD state diagram, part a**

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| --- | --- | --- | --- | --- |
|  | DO\_DISCOVERY2 | | |  |
| present\_sig MARK | | |
| VMPD > VDiscovery\_th | |  | VMPD < VReset\_th | |
|  | | |
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VMPD < VDiscovery\_th

VMPD < VDiscovery\_th

DO\_DISCOVERY6

present\_sig MARK

DISCOVERY\_LOW\_TYPE\_0

IF (mpd\_type = 0) THEN present\_sig DISCOVERY

ELSE

present\_sig MARK END

DO\_MARK4

present\_mark\_sig MARK start mark\_timer

DO\_MARK5

present\_mark\_sig MARK start mark\_timer

C

VMPD > VDiscovery\_th

VMPD < VReset\_th

mark\_timer\_done \* (VMPD ≥ VDiscovery\_th)

mark\_timer\_done \* (VMPD ≥ VDiscovery\_th)

VMPD >

VMPD < VDiscovery\_th

mark\_timer\_done \* (VMPD ≥ VDiscovery\_th)

A

VMPD > VDiscovery\_th

VMPD < VReset\_th

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| --- | --- | --- | --- | --- |
|  | DISCOVERY\_LOW\_TYPE\_1 | | |  |
| IF (mpd\_type = 1) THEN present\_sig DISCOVERY  ELSE  present\_sig MARK END | | |
| VMPD > VDiscovery\_th | |  | VMPD < VReset\_th | |
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| --- | --- | --- | --- | --- |
|  | DISCOVERY\_LOW\_TYPE\_0/1 | | |  |
| IF (mpd\_type = 01) THEN present\_sig DISCOVERY  ELSE  present\_sig MARK END | | |
| VDiscovery\_th | |  | VMPD < VReset\_th | |
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| --- | --- | --- | --- |
|  | DO\_MARK6 | | |
| present\_sig MARK start mark\_timer | | |
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#### Figure 189–7—Top level MPD state diagram continued, part b 53

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PON\_EVAL 6

present\_mismatch\_indication ((mpd\_type = 1) \* (VMPD < Vtype1\_th)) + 7

((mpd\_type = 0) \* (VMPD > Vtype1\_th)) + 8

(VMPD < Vtype0\_th) 9

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!present\_mismatch\_indication

|  |  |
| --- | --- |
| INRUSH | |
| present\_sig INRUSH start inrush\_timer | |
| mer\_done |  |

inrush\_ti

|  |  |
| --- | --- |
| PON\_LOAD\_ON | |
| present\_sig PON present\_mpi\_power TRUE present\_tps TRUE | |
| pe = 1) \* (VMPD < Vtype1\_th)) + pe = 0) \* (VMPD > Vtype1\_th)) + Vtype0\_th) |  |

((mpd\_ty ((mpd\_ty (VMPD <

|  |  |  |
| --- | --- | --- |
| PON\_NO\_POWER | | |
| present\_sig DISABLED present\_mpi\_power FALSE present\_tps FALSE | | |
| < VReset\_th |  | VMPD > V |

VMPD

B

present\_mismatch\_indication 12

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type0\_th 36

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#### Figure 189–8—Top level MPD state diagram continued, part c 40

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#### MPD discovery 43

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When the MPD is presenting a mark event signature in a DO\_MARKx state, as shown in the state diagram 45

of [Figure 189–6,](#_bookmark356) [Figure 189–7](#_bookmark357), and [Figure 189–](#_bookmark359)8, the MPD shall draw IMPD\_mark as defined in [Table 189–7](#_bookmark361) 46

within TMPD\_mark after entering the state. 47

48

The MPD shall not exceed the IMPD\_mark current limits when voltage at the MPI enters the VMPD\_mark 49

specification as defined in [Table 189–](#_bookmark361)7. 50

51

The MPD enters a DO\_DISCOVERYx state, as shown in the state diagram of [Figure 189–6,](#_bookmark356) [Figure 189–7,](#_bookmark357) 52

and [Figure 189–8,](#_bookmark359) when the MPI voltage transitions from VMPD\_mark to VMPD\_discover, crossing the 53

threshold VDiscovery\_th. 54

When the MPD enters a DO\_DISCOVERYx state and present\_sig is DISCOVERY, the MPD shall draw 1

IMPD\_discover within TMPD\_discover after entering the state. 2

3

When the MPD enters a DO\_DISCOVERYx state and present\_sig is MARK, the MPD shall draw 4

IMPD\_mark within TMPD\_discover after entering the state. 5

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#### Table 189–7—MPD discovery parameters 8

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|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Item** | **Parameter** | **Symbol** | **Min** | **Max** | **Units** | **Additional Information** |
| 1 | Mark event voltage | VMPD\_mark | 16 | 19.1 | V |  |
| 2 | Mark discovery threshold | VDiscovery\_th | 11.9 | 16 | V |  |
| 3 | Discovery event voltage | VMPD\_discover | 6.9 | 11.9 | V |  |
| 4 | Mark event current | IMPD\_mark | 100 | 200 | A |  |
| 5 | Discovery event cur- rent | IMPD\_discover | 1 | 2 | mA |  |
| 6 | Discovery reset threshold | VMPD\_reset | 2.8 | 6.9 | V |  |
| 7 | MPD discovery sta- bility time | TMPD\_discover | - | 6 | ms |  |
| 8 | MPD mark stability time | TMPD\_mark | - | 3 | ms |  |
| 9 | Input capacitance outside of PON\_- LOAD-ON state | CMPD\_discover | 5 | 12 | nF | 2.7V to 19.1V |
| 10 | IDLE and OFFLINE  event current | IMPD\_idle | - | 200 | A |  |

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The MPD’s response to the DISCOVERx events informs the MPSE of the MPD Type. The first two 37

DISCOVERx events allow the MPSE to calibrate. During event 1, all MPDs respond by drawing 38

IMPD\_discover. During event 2, all MPDs do not respond (i.e. continue to draw IMPD\_mark). During 39

event 3, only Type 0 MPDs respond. During event 4, only Type 1 MPDs 40

respond. During event 5, only Type 0/1 MPDs respond. An MPD responds only once during events 3, 4,

and 5. [Table 189–8](#_bookmark363) shows MPD responses to each DISCOVER\_LOWx event. 43

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#### MPD power

**Table 189–8—MPD response to DISCOVERx events** 1

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|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| DISCOVERx Event 1 | DO\_DISCOVERY1 | | | | |
| DISCOVERx Event 2 | DO\_DISCOVERY2 | | | | |
| DISCOVERx Event 3 | DISCOVERY\_LOW\_TYPE\_0 | | | | |
| DISCOVERx Event 4 | DISCOVERY\_LOW\_TYPE\_1 | | | | |
| DISCOVERx Event 5 | DISCOVERY\_LOW\_TYPE\_0/1 | | | | |
|  | | | | | |
| **Discovery event:** | **1** | **2** | **3** | **4** | **5** |
| Type 0 | 1 | 0 | 1 | 0 | 0 |
| Type 1 | 1 | 0 | 0 | 1 | 0 |
| Type 0/1 | 1 | 0 | 0 | 0 | 1 |

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The power supply of the MPD shall operate within the characteristics in [Table 189–9](#_bookmark364). The MPD may be 22

capable of drawing power from a local power source. When a local power source is provided, the MPD may 23

draw some, none, or all of its power from the MPI. 24

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#### Table 189–9—MPD power supply limits 27

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|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Item** | **Parameter** | **Symbol** | **Unit** | **Min** | **Max** | **Type** | **Additional Information** |
| 1 | Input voltage | VPort\_MPD | V | 16 | 30 | 0 |  |
| 34 | 50 | 1 |  |
| 2 | Unit power | PMPD\_1U | W |  | 1 | 0 and 0/1 | 1 unit load |
|  | 2 | 1 | 1 unit load |
| 3 | Unit loading | Nunit | - | 1 | 16 | ALL | Must be an inte- ger |
| 4 | Input power | PMPD | W | 1 | 16 | 0 and 0/1 | Nunit \* PMP- D\_1U |
| 2 | 32 | 1 |
| 5 | Inrush current | IInrush\_MPD | A | - | .01 | ALL |  |
| 6 | MPD Type 0 Voltage threshold | Vtype0\_th | V | 11.9 | 16 | ALL |  |
| 7 | MPD Type 1 Voltage threshold | Vtype1\_th | V | 30.1 | 34 | ALL |  |

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**Table 189–9—MPD power supply limits *(continued)*** 1

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| **Item** | **Parameter** | **Symbol** | **Unit** | **Min** | **Max** | **Type** | **Additional Information** |
| 8 | Mark Timer dura- tion | TMark | ms | 50 | 75 | ALL |  |
| 9 | Inrush to operating state delay | TInrush | ms | 50 | 75 | ALL |  |
| 10 | MPD MPI capaci- tance during POW- ER\_ON | CPort | F | - | 180 | ALL |  |
| 11 | MPD current when connected to in- compatible MPSE type | IMPD\_Dis- abled | mA | - | 5 | ALL |  |
| 12 | MPD current slew rate  dI/dt |  | mA/ms | - | 190 | ALL |  |

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#### MPD inrush and Power On 24

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An MPD evaluates the MPSE system type when VMPD is greater than Vtype0\_th and TMark time has elapsed. 26

If VMPD is greater than Vtype0\_th, the TMark time has elapsed, and the voltages at both MP1 and MP2 are in a 27

range that is compatible with the MPD type, the MPD proceeds to the INRUSH state. 28

29

The inrush current is the initial current drawn by the MPD, which is used to charge CPort. An MPD limits the 30

inrush current below IInrush\_MPD to allow for large values of CPort. MPDs remain in inrush for TInrush time. 31

After TInrush has elapsed the MPD may draw full operating power. 32

33

When it is connected to an incompatible system type, an MPD draws no more than IMPD\_Disabled and does 34

not enter the INRUSH state. If VMPD is greater than Vtype0\_th, the TMark time has elapsed, and VMPD is not 35

in a voltage range that is compatible with the MPD type, the MPD shall provide an active indication to the 36

user that the MPD is connected to an incompatible MPSE. The method of active indication is left to the 37

MPD implementor. Two examples would be a flashing LED or a message from a console port. 38

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#### MPD unit load 40

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MPDs consume integer units of load, known as “unit loads”. 42

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For Type 0 and Type 0/1 MPDs, one unit load represents 1W. For Type 1 MPDs, one unit load represents 44

2W. 45

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A mixing segment can support up to 16 unit loads. Each MPD is allocated a minimum of 1 unit load and 47

may consume no more than 16 unit loads. The MPD system type and unit load level should be clearly 48

indicated so users can track loading on a mixing segment. 49

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MPD unit load level shall be an integer indicating the maximum power required by the MPD, where 51

Nunit \* PMPD\_1U is greater than the MPD’s power requirements for the MPD system type. 52

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MPDs may draw power less than or equal to PMPD, based on the unit load level indicated, after entering the 1

PON\_LOAD\_ON state. 2

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#### MPD Transmit Power Signature (TPS) 4

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The Transmit Power Signature (TPS) is a minimum current waveform reported by an MPD which allows an 6

MPD to minimize its power consumption while signaling the MPSE to continue transmitting power. 7

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An MPD that requires power from the MPI shall report a valid TPS at the MPI. An MPD that does not report 9

TPS may have its power removed within the limits of TTPSDO as defined in [Table 189–5.](#_bookmark335) IMPI\_TPS, TTPS\_MPD, 10

and TTPSDO\_MPD, are defined in [Table 189–1](#_bookmark368)0. 11

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TPS shall consist of current draw equal to or above IMPI\_TPS for a minimum duration of TTPS\_MPD followed 13

by an optional TPS dropout for no longer than TTPS\_MPD. 14

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#### Table 189–10—MPD Transmit Power Signature (TPS) parameters 17

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| --- | --- | --- | --- | --- | --- | --- |
| **Item** | **Parameter** | **Symbol** | **Min** | **Max** | **Units** | **Additional Information** |
| 1 | MPD MPI current | IMPI\_TPS | 10 | - | mA |  |
| 2 | MPD TPS time | TTPS\_MPD | 7 | - | ms |  |
| 3 | MPD TPS dropout period | TTPSDO\_MPD | - | 310 | ms |  |

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## Additional electrical specifications 29

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This clause defines additional electrical specifications for a fully connected MPoE system (that is, MPSE, 31

cabling, one or more MPDs, and related PHYs) and therefore to each element of such a system. 32

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#### Electrical Isolation 34

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MPDs and MPSEs shall provide isolation between all accessible external conductors, including frame 36

ground (if any), and all MPI leads, including those not used by the MPD or MPSE. Any equipment that can 37

be connected to an MPSE or MPD through a non-MPI connector that is not isolated from the MPI leads 38

needs to provide isolation between all accessible external conductors, including frame ground (if any), and 39

the non-MPI connector. External accessibility to conductors is specified in Section 5.4.10.1 b) of 40

IEC 62368-1:2023. 41

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#### Electrical isolation environments 43

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There are three electrical power distribution environments to be considered that require different electrical 45

isolation properties. They are as follows: 46

* **MPoE Environment A:** When a LAN or LAN segment, with all its associated interconnected 47

equipment, is entirely contained within a single low-voltage power distribution system and within a 48

single building. 49

* **MPoE Environment B:** When a LAN crosses the boundary between separate power distribution 50

systems or the boundaries of a single building. 51

52

* **MPoE Environment C:** When a LAN or LAN segment, with all its associated interconnected 53

equipment, is entirely contained within a single low-voltage power distribution system contained 54

within a single cabinet, vehicle, machine, or other power domain where ground loops are unlikely to 1

occur. 2

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#### MPoE Environment A requirements 4

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Attachment of a network segment via a Network Interface Device (NID) that has multiple instances of a 6

balanced twisted-pair MPI requires electrical isolation between each segment and the protective ground of 7

the NID. 8

9

This electrical isolation shall meet the isolation requirements as specified in [Annex J.1](#_bookmark398) with electrical 10

strength test c) details being replaced by: “An impulse test consisting of a 1500 V, 10/700 waveform, 11

applied 10 times, with a 60 s interval between pulses. The shape of the impulses is 10/700 (10 μs virtual 12

front time, 700 μs virtual time to half value)”, as defined in ITU-T Recommendation K.44. 13

14

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or 15

PHY (see, e.g., 14.3.1.1, 25.4.6, or 40.6.1.1). Equipment with multiple instances of MPSE, MPD, or both 16

shall meet or exceed the isolation requirement of the MAU/PHY with which they are associated. 17

18

An Environment A multiport NID does not require electrical power isolation between mixing segments. 19

20

An Environment A MPSE shall switch the more negative conductor. It is allowed to switch both conductors. 21

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#### MPoE Environment B requirements 23

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The attachment of network segments that cross Environment A boundaries requires electrical isolation 25

between each segment and all other attached segments as well as to the protective ground of the NID. 26

27

This electrical isolation shall meet the isolation requirements as specified in [Annex J.1](#_bookmark398) with electrical 28

strength test c) details being replaced by: “An impulse test consisting of a 1500 V, 10/700 waveform, 29

applied 10 times, with a 60 s interval between pulses. The shape of the impulses is 10/700 (10 μs virtual 30

front time, 700 μs virtual time to half value)”, as defined in ITU-T Recommendation K.44. 31

32

For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or 33

PHY (see, e.g., 14.3.1.1, 25.4.6, or 40.6.1.1). Equipment with multiple instances of MPSE, MPD, or both 34

shall meet or exceed the isolation requirement of the MAU/PHY with which each is associated. 35

36

An environment B MPSE shall switch the more negative conductor. It is allowed to switch both conductors. 37

The requirements for interconnected electrically conducting link segments that are partially or fully external 38

to a single building environment may require additional protection against lightning strikes or other hazards. 39

Protection requirements for such hazards are beyond the scope of this standard. Guidance on these 40

requirements may be found in Section 6 of IEC 60950-1:2001 and throughout IEC 62368-1:2023, as well as 41

many local and national codes related to safety. 42

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#### MPoE Environment C requirements 44

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Attachment of network segments via NIDs that have multiple instances of a balanced twisted-pair MPI 46

requires electrical isolation between each segment and the protective ground of the NID. 47

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This electrical isolation shall provide at least 1 MΩ dc isolation between all accessible external conductors, 49

including frame ground (if any), and all MPI leads, when measured using a 5 V ± 20% source voltage. 50

Environment C MPSEs shall not be required to comply with the isolation requirements as specified in 51

[Annex J.1.](#_bookmark398) 52

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For NIDs, the requirement for isolation is encompassed within the isolation requirements of the MAU or 1

PHY (see, e.g., 14.3.1.1, 25.4.6, or 40.6.1.1). Equipment with multiple instances of MPSE, MPD, or both 2

shall meet or exceed the isolation requirement of the MAU/PHY with which they are associated. 3

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An Environment C multiport NID does not require electrical power isolation between link segments. 5

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An Environment C MPSE shall switch the more negative conductor. It is allowed to switch both conductors. 7

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#### 189.6.2 Fault tolerance 9

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MPDs tolerate 60 V in either polarity (see [188.9.3).](#_bookmark270) 11

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MPSEs tolerate 60 V applied with specified polarity in [189.4.2.](#_bookmark315) MPSEs tolerate ILIM for TLIM when 13

connected to the mixing segment in reverse polarity and the power source is another MPSE. 14

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## Environmental 16

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#### General safety 19

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Equipment subject to this clause shall conform to the general safety requirements in Annex J.2. In particular, 21

the MPSE shall be classified as a Limited Power Source in accordance with Annex Q of IEC 62368-1:2023, 22

as applicable. For automotive applications, systems described in this clause may be subject to additional 23

requirements; refer to ISO 26262. All equipment subject to this clause additionally may be required to 24

conform to any applicable local, state, or national standards related to safety, including national motor 25

vehicle standards related to safety. 26

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#### Network safety 28

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This subclause sets forth a number of recommendations and guidelines related to safety concerns. The list is 30

neither complete nor does it address all possible safety issues. The designer is urged to consult the relevant 31

local, national, and international safety regulations to verify compliance with the appropriate requirements. 32

LAN cabling systems described in this clause are subject to at least four direct electrical safety hazards 33

during their installation and use. These hazards are as follows: 34

* a) Direct contact between LAN components and power, lighting, or communications circuits. 35
* b) Static charge buildup on LAN cabling and components. 36
* c) High-energy transients coupled onto the LAN cabling system. 37
* d) Voltage potential differences between safety grounds to which various LAN components are con- 38

nected. 39

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Such electrical safety hazards should be avoided or appropriately protected against for proper network 41

installati, special measures should be taken to verify that the intended safety features are not negated during 42

installation on and performance. In addition to provisions for proper handling of these conditions in an 43

operational systemof a new network or during modification of an existing network. 44

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#### Installation and maintenance guidelines 46

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It is a mandatory requirement that sound installation practice, as defined by applicable local codes and 48

regulations, be followed in every instance in which such practice is applicable. In particular, users are 49

cautioned to be aware of the ampacity of cabling, as installed, and local codes and regulations, e.g., NFPA70 50

– the National Electrical Code® (NEC®) relevant to the maximum class supported. 51

52

It is a mandatory requirement that, during installation of the cabling plant, care be taken to verify that non- 53

insulated network cabling conductors do not make electrical contact with unintended conductors or ground. 54

All cabling and equipment subject to this clause is expected to be mechanically and electrically secure in a 1

professional manner. In automotive applications, all MPoE cabling should be routed in way to provide 2

maximum protection by the motor vehicle sheet metal and structural components, following SAE J1292, 3

ISO 14229, and ISO 15764. 4

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Automotive environmental conditions are generally more severe than those found in many commercial and 6

industrial environments. 7

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#### Patch panel considerations 9

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It is possible that the current carrying capability of a cabling cross-connect may be exceeded by the current 11

capacity of the MPSE. The designer should consult the manufacturers’ specifications to verify compliance 12

with the appropriate requirements. 13

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#### Telephony voltages 15

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The use of building wiring brings with it the possibility of wiring errors that may connect telephony voltages 17

to an MPSE or MPD. Other than voice signals, the primary voltages that may be encountered are the 18

“battery” and ringing voltages. Although there is no universal standard, the following maximums generally 19

apply: Battery voltage to a telephone line is generally 56 V dc, applied to the line through a balanced 400 Ω 20

source impedance. Ringing voltage is a composite signal consisting of an ac component and a dc 21

component. The ac component is up to 175 Vp at 20 Hz to 60 Hz with a 100 Ω source resistance. The dc 22

component is 56 V dc with 300 Ω to 600 Ω source resistance. Large reactive transients can occur at the start 23

and end of each ring interval. 24

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Application of any of the above voltages to the MPI of an MPSE or an MPD in non-automotive applications 26

shall not preclude conformance with [189.7.1](#_bookmark377) and [189.7.2](#_bookmark378). 27

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#### Electromagnetic emissions 29

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The MPD and MPSE powered cabling link shall comply with applicable local and national codes for the 31

limitation of electromagnetic interference. 32

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In automotive applications, when tested according to CISPR 25 test methods, an MPoE system shall meet 34

the following motor vehicle EMC requirements: 35

* + - 1. Radiated/Conducted Emissions: CISPR 25, IEC 61967-1/4, and IEC 61000-4-21 36
      2. Radiated/Conducted Immunity: ISO 11452, IEC 62132-1/4, and IEC 61000-4-21 37

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* + - 1. Electrostatic Discharge: ISO 10605 and IEC 61000-4-2/3 39
      2. Electrical Disturbances: IEC 62215-3 and ISO 7637-2/3 40

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Exact test setup and test limit values may be adapted to each specific application. 42

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#### Temperature and humidity 44

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The MPD and MPSE powered cabling link segment is expected to operate over a reasonable range of 46

environmental conditions related to temperature, humidity, and physical handling. Specific requirements 47

and values for these parameters are beyond the scope of this standard. 48

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#### Labeling 1

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It is recommended that the MPSE or MPD (and supporting documentation) be labeled in a manner visible to 3

the user with at least the following parameters: 4

* + - 1. Power classification and power level in terms of maximum current drain over each compatible 5

operating voltage range both in terms of Watts, Amps, and Unit Loads, applies for MPD only 6

* + - 1. Port type (e.g., 10BASE-T1M, TIA Category, or ISO Class) 7

8

* + - 1. Any applicable safety warnings 9
      2. “MPSE” or “MPD” as appropriate 10
      3. Indicate any non-MPI connectors which are not isolated from the MPI leads 11
      4. System type (i.e., “Type 0”, “Type 1” or “Type 0/1”) 12

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* + - 1. MPoE Environment type (e.g., Environment A, B, or C) 14

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## Protocol implementation conformance statement (PICS) proforma for 1

## [Clause 189](#_bookmark300), [Multidrop Power over Ethernet (MPoE)](#_bookmark300)8 2

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#### Introduction 4

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The supplier of a protocol implementation that is claimed to conform to [Clause 189,](#_bookmark300) [Multidrop Power over](#_bookmark300) 6

[Ethernet (MPoE](#_bookmark300)), shall complete the following protocol implementation conformance statement (PICS) 7

proforma. 8

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A detailed description of the symbols used in the PICS proforma, along with instructions for completing the 10

PICS proforma, can be found in Clause 21. 11

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#### Identification 13

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#### Implementation identification 15

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|  |  |
| --- | --- |
| Supplier1 |  |
| Contact point for inquiries about the PICS1 |  |
| Implementation Name(s) and Version(s)1,3 |  |
| Other information necessary for full identification—e.g., name(s) and version(s) for machines and/or operating systems; System Name(s)2 |  |
| NOTE 1—Required for all implementations.  NOTE 2—May be completed as appropriate in meeting the requirements for the identification.  NOTE 3—The terms Name and Version should be interpreted appropriately to correspond with a supplier’s terminology (e.g., Type, Series, Model). | |

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#### Protocol summary 32

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| --- | --- |
| Identification of protocol standard | IEEE Std 802.3da-202x, [Clause 189,](#_bookmark300) [Multidrop Power over](#_bookmark300) [Ethernet (MPoE)](#_bookmark300) |
| Identification of amendments and corrigenda to this PICS proforma that have been completed as part of this PICS |  |
| Have any Exception items been required? No [ ] Yes [ ]  (See Clause 21; the answer Yes means that the implementation does not conform to IEEE Std 802.3da-202x.) | |

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Date of Statement

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8*Copyright release for PICS proformas:* Users of this standard may freely reproduce the PICS proforma in this subclause so that it can 53

be used for its intended purpose and may further publish the completed PICS. 54

#### Major capabilities/options 1

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| \*MPSE | Implements MPSE behavior |  | Provides power to the mixing segment | O | Yes [ ]  No [ ] |
| \*MPD | Implements MPD behavior |  | Sources power from the mixing segment | O | Yes [ ]  No [ ] |

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#### PICS proforma tables for [Multidrop Power over Ethernet (MPoE)](#_bookmark300) 12

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#### Power and Mixing segment requirements 14

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| MS1 | DC loop resistance | [189.2](#_bookmark309) | Less than or equal to 4 Ω | M | Yes [ ] |
| MS2 | Sum of unit loads on a mixing segment | [189.3](#_bookmark310) | Shall not exceed 16 | M | Yes [ ] |

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#### Multidrop Power Sourcing Equipment (MPSE) 25

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| MPSE1 | MPSE voltage and power types | [189.4.1](#_bookmark314) | Complies with voltage and power requirements in  [Table 189–1](#_bookmark312) for the relevant type | MPSE:M | Yes [ ]  N/A [ ] |
| MPSE2 | Pinout and Polarity | [189.4.2](#_bookmark315) | Conforms to the pinout of [Table 189–2](#_bookmark316) and provide a single polarity | MPSE:M | Yes [ ]  N/A [ ] |
| MPSE3 | Voltage specifications met at both MP1 and MP2 independently | [189.4.3](#_bookmark317) |  | MPSE:M | Yes [ ]  N/A [ ] |
| MPSE4 | MPSE state diagram behavior | [189.4.4](#_bookmark319) | Implements behavior of [Figure 189–3](#_bookmark327) and  [Figure 189–4](#_bookmark329) | MPSE:M | Yes [ ]  N/A [ ] |
| MPSE5 | Discovery current limit | [189.4.5](#_bookmark330) | Limits current to IDiscovery\_LIM during all discovery events, DISCOVERY\_LOWx and DISCOVERY\_HIGH\_MARK  x | MPSE:M | Yes [ ] N/A [ ] ] |
| MPSE6 | Presents an invalid MPD discovery signature | [189.4.5](#_bookmark330) | Unless acting as an MPD, presents with one of the attributes defined in  [Table 189–4](#_bookmark332) | MPSE:M | Yes [ ] N/A [ ]] |

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| MPSE7 | Output requirements | [189.4.6](#_bookmark333) | Conforms to limits in [Table 189–5](#_bookmark335) | MPSE:M | Yes [ ]  N/A [ ] |
| MPSE8 | Short circuit current | [189.4.9](#_bookmark338) | Limits current to ILIM for a duration up to TLIM | MPSE:M | Yes [ ]  N/A [ ] |
| MPSE9 | Power removal | [189.4.10](#_bookmark341) | Removes power from the MPI in the absence of MPD TPS, if an overload is detected, if a short circuit is detected, or if commanded by management. | MPSE:M | Yes [ ]  N/A [ ] |
| MPSE10 | Transmit Power Signature (TPS) absent | [189.4.10.1](#_bookmark342) | TPS defined as absent in the POWER\_ON state if IMPSE is less than or equal to IHold min. | MPSE:M | Yes [ ]  N/A [ ] |
| MPSE1 | TPS not absent | [189.4.10.1](#_bookmark342) | TPS not absent when IMPSE is greater than or equal to IHold max continuously for at least  TTPS every TTPS + TTPSDO  (except for in  ERROR\_DELAY state) | MPSE:M | Yes [ ]  N/A [ ] |

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#### Multidrop Powered Device (MPD) 23

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| MPD1 | MPD polarity insensitive | [189.5.2](#_bookmark345) | Able to operate in polarity A or polarity B per [Table 189–6](#_bookmark346) | MPD:M | Yes [ ]  N/A [ ] |
| MPD2 | MPD state diagram | [189.5.3](#_bookmark348) | Implements behavior of [Figure 189–6,](#_bookmark356) [Figure 189–7](#_bookmark357)  and [Figure 189–8](#_bookmark359) | MPD:M | Yes [ ]  N/A [ ] |
| MPD3 | MPD Mark current in MARK state | [189.5.4](#_bookmark360) | Draws IMPD\_mark within TMPD\_mark after entering a DO\_MARKx state | MPD:M | Yes [ ]  N/A [ ] |
| MPD4 | MPD Mark current limits | [189.5.4](#_bookmark360) | Does not exceed IMPD\_mark current limits when voltage is  within the VMPD\_mark specification of [Table 189–7](#_bookmark361) | MPD:M | Yes [ ] N/A [ ] ] |
| MPD5 | MPD Discovery signature current | [189.5.4](#_bookmark360) | Draws IMPD\_discover within TMPD\_discover after entering a DO\_DISCOVERYx state | MPD:M | Yes [ ] N/A [ ]] |
| MPD6 | MPD Mark signature current in DISCOVERY state | [189.5.4](#_bookmark360) | Draws IMPD\_mark within TMPD\_discover after entering a DO\_DISCOVERYx state | MPD:M | Yes [ ]  N/A [ ] |

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| MPD7 | MPD power draw | [189.5.5](#_bookmark362) | Conforms to limits in [Table 189–9](#_bookmark364) | MPD:M | Yes [ ]  N/A [ ] |
| MPD8 | Mismatch indication | [189.5.5.1](#_bookmark365) | Provides an active indication to the user that the MPD is connected to an incompatible MPSE | MPD:M | Yes [ ]  N/A [ ] |
| MPD9 | MPD unit load | [189.5.5.2](#_bookmark366) | An integer indicating the maximum power required by the MPD | MPD:M | Yes [ ]  N/A [ ] |
| MPD10 | MPS reporting TPS | [189.5.5.3](#_bookmark367) | An MPD that requires power reports a valid TPS at the MPI | MPD:M | Yes [ ]  N/A [ ] |
| MPD11 | TPS current | [189.5.5.3](#_bookmark367) | Current draw equal to or above IMPI\_TPS for at least TTPS\_MPD, wiht an optional dropout no longer than TTPS\_MPD | MPD:M | Yes [ ]  N/A [ ] |

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#### Additional electrical specifications 21

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| AES1 | Electrical isolation | [189.6.1](#_bookmark370) | Isolation between all accessible external conductors, including frame ground, and all MPI leads | M | Yes [ ]  N/A [ ] |
| AES2 | Environment A Electrical isolation | [189.6.1.1.1](#_bookmark372) | Meet requirements of [Annex J.1](#_bookmark398) with electrical strength test c) modified as in [189.6.1.1.1](#_bookmark372) | M | Yes [ ]  N/A [ ] |
| AES3 | Environment A multi-port equipment | [189.6.1.1.1](#_bookmark372) | Meet requirements of the associated PHY or MAU | M | Yes [ ]  N/A [ ] |
| AES4 | Environment A MPSE switched conductor | [189.6.1.1.1](#_bookmark372) | Switch the more negative conductor | M:MPSE | Yes [ ] N/A [ ] ] |
| AES5 | Environment B Electrical isolation | [189.6.1.1.2](#_bookmark373) | Meet requirements of [Annex J.1](#_bookmark398) with electrical strength test c) modified as in [189.6.1.1.2](#_bookmark373) | M | Yes [ ] N/A [ ]] |
| AES6 | Environment B multi-port equipment | [189.6.1.1.3](#_bookmark374) | Meet requirements of the associated PHY or MAU | M | Yes [ ]  N/A [ ] |

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| AES7 | Environment B MPSE switched conductor | [189.6.1.1.1](#_bookmark372) | Switch the more negative conductor | M:MPSE | Yes [ ]  N/A [ ] |
| AES8 | Environment C accessible conductors isolation | [189.6.1.1.3](#_bookmark374) | provide at least 1 MΩ dc isolation between all accessible external conductors, including frame ground (if any), and all MPI leads, | M | Yes [ ]  N/A [ ] |
| AES9 | Environment C exception to [Annex J.1](#_bookmark398) | [189.6.1.1.3](#_bookmark374) | Not required to comply with [Annex J.1](#_bookmark398) | M | Yes [ ]  N/A [ ] |
| AES10 | Environment C multi-port equipment | [189.6.1.1.3](#_bookmark374) | Meet requirements of the associated PHY or MAU | M | Yes [ ]  N/A [ ] |
| AES11 | Environment B MPSE switched conductor | [189.6.1.1.3](#_bookmark374) | Switch the more negative conductor | M:MPSE | Yes [ ]  N/A [ ] |

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#### Environmental specifications 19

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| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| ES1 | General safety for MPoE equipment | [189.7.1](#_bookmark377) | Conforms to Annex J.2 | M | Yes [ ]  N/A [ ] |
| ES2 | Limited Power Source | [189.7.1](#_bookmark377) | MPSE classified as a Limited Power Source per Annex Q of IEC 62368-1:2023 | MPSE:M | Yes [ ]  N/A [ ] |
| ES3 | Telephony voltages for non- automotive applications | [189.7.5](#_bookmark381) | Application of telephony voltages does not preclude conforman[ce with 189.7.1](#_bookmark377) and [189.7.2](#_bookmark378) | M | Yes [ ]  N/A [ ] |
| ES4 | Electromagnetic emissions | [189.7.6](#_bookmark382) | Shall comply with applicable local and national codes for limitation of electromagnetic interference | M | Yes [ ]  N/A [ ] |
| ES5 | Automotive electromagnetic requirements | [189.7.6](#_bookmark382) | Meet the following motor vehicle EMC requirements:   1. Radiated/Conducted Emissions: CISPR 25, IEC 61967-1/4, and IEC 61000-4-21 2. Radiated/Conducted Immunity: ISO 11452, IEC 62132-1/4, and IEC 61000-4-21 3. Electrostatic Discharge: ISO 10605 and IEC 61000-4-2/3 4. Electrical Disturbances: IEC 62215-3 and ISO 7637-2/3 | M | Yes [ ] N/A [ ] ] |

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**Annex J** 1

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(normative) 3

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**Electrical isolation and general safety** 6

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**J.1 Electrical isolation** 9

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##### Change the NOTE in J.1 as follows: 12

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NOTE 1—If the MDI is a PI or MPI, then see the relevant "Electrical isolation" subclause~~also a Clause 33 or Clause 145~~

PI then see 33.4.1 or 145.4.1 for specific requirements associated with option c). 14

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