**79. IEEE 802.3 Organizationally Specific Link Layer Discovery Protocol**

**(LLDP) type, length, and value (TLV) information elements**

**79.1.1.1 Destination Address field**

The Destination Address field of an IEEE 802.3 LLDP frame contains a MAC address specified by 7.1 of

IEEE Std 802.1AB-2009 (see 79.2).

For nodes operating on a 10BASE-T1S or 10BASE-T1M mixing segment, the Destination Address field of an IEEE 802.3 LLDP frame shall contain the “Nearest bridge” group MAC address value as specified in Table 7-1 of IEEE Std 802.1AB-2009.

## 79.3 IEEE 802.3 Organizationally Specific TLVs

#### Table 79–1—IEEE 802.3 Organizationally Specific TLVs

|  |  |  |
| --- | --- | --- |
| **IEEE 802.3 subtype** | **TLV name** | **Subclause reference** |
| … |
| 9 | PLCA | [79.3.9](#_bookmark119) |
| 10 | Topology Discovery | 79.3.10 |
| 11 | Hibernation Control | 79.3.11 |
| 12 | Power Bus Management | 79.3.12 |
| ~~9~~ 13 to 255 | Reserved | — |

## Power Via MDI TLV

Clause 33 and Clause 145 define two optional power entities: a Powered Device (PD) and Power Sourcing Equipment (PSE). These entities allow devices to draw/supply power over the sample generic cabling as used for data transmission. The Power Via MDI TLV allows network management to advertise and discover the Power over Ethernet capabilities of the sending IEEE 802.3 LAN station. This TLV is also required to perform Data Link Layer classification as defined in 33.6 and 145.5. Figure 79–3 shows the format of this TLV.

Clause 189 defines Multidrop Power over Ethernet (MPoE) which allows a PSE to power multiple PDs. For maximum compatibility this TLV may also be utilized to communicate information about powering state. The following terms shall be considered equivalent for the purposes of this TLV unless otherwise noted: MPSE and PSE, MPD and PD, MDI and MPI.

The Power via MDI TLV shown in Figure 79–3 was originally defined in IEEE Std 802.1AB-2005 Annex G.3. This original TLV supported only the first three fields of Figure 79–3, labeled basic fields, enabling discovery and advertisement of Power via MDI capabilities. The Power via MDI TLV was revised by IEEE Std 802.3at-2009 to add a further three fields, labeled DLL classification extension, to provide Data Link Layer (DLL) classification capabilities. The Power via MDI TLV was revised again by IEEE Std 802.3bt-2018 to add a further nine fields, labeled Type 3 and Type 4 extension, to support additional capabilities offered by Type 3 and Type 4 PSEs and PDs.

Power entities may continue to use the Power Via MDI TLV basic fields shown in Figure 79–3 prior to supplying/drawing power to/from the Power Interface (PI), as defined in 1.4.484. The DLL classification extension fields and Type 3 and Type 4 extension fields shown in Figure 79–3 shall not be sent by the PSE unless it is supplying power to a PI encompassed within an MDI and by the PD unless it is drawing power from the PI.

**...**

TLV header

TLV information string

Basic fields

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| TLVtype=127 | TLV information string length | IEEE 802.3 OUI00-12-0F | IEEE 802.3subtype=2 | MDIpower support | PSEpower pair | Power class |
| 7 bits | 9 bits | 3 octets | 1 octet | 1 octet | 1 octet | 1 octet |

**... ...**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Type/ source/ priority | PDrequested power value | PSEallocated power value | PD requested power value Mode A | PD requested power value Mode B | PSE allocated power value Alternative A |

1 octet

2 octets

2 octets

2 octets

2 octets

2 octets

TLV information string *(continued)*

DLL classification extension

Type 3 and Type 4 extension

**...**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| PSE allocated power value Alternative B | Power status | System setup | PSEmaximum available power | Autoclass | Power down |

2 octets

2 octet 1 octet

2 octets

1 octet 3 octets

TLV information string *(continued)*

Type 3 and Type 4 extension *(continued)*

The TLV information string length is

* Basic fields: 7 octets
* Basic fields and DLL classification extension: 12 octets
* Basic fields, DLL classification extension, and Type 3 and Type 4 extension: 29 octets

## Figure 79–3—Power Via MDI TLV format

Power entities that implement Data Link Layer classification shall support the Power via MDI TLV DLL classification extension fields shown in Figure 79–3 after the PI has been powered. Type 3 or Type 4 power entities that implement Data Link Layer classification and are connected to another Type 3 or Type 4 power entity shall support the Type 3 and Type 4 extension fields shown in Figure 79–3 after the PI has been powered. Such entities, when connected to a Type 1 or Type 2 power entity, may support the Type 3 and Type 4 extension fields shown in Figure 79–3 after the PI has been powered. Type 1 and Type 2 devices shall not include the Type 3 and Type 4 extension fields in the transmitted Power via MDI TLV.

NOTE—Some implementations of the Power via MDI TLV in Type 1 and Type 2 power entities ignore TLVs that are longer than 12 octets. In order to be interoperable with these implementations, Type 3 and Type 4 power entities are permitted to transmit 12-octet TLVs (without the Type 3 and Type 4 extension) after first transmitting at least one valid 29-octet TLV (including the Type 3 and Type 4 extension). Table 79–3 lists the recommended Power via MDI TLV formats for each combination of power entity Types.

Type 3 and Type 4 PD power entities can determine the PSE Type based on the duration of the first classification event (see 145.3.7) or based on the length of a received Power via MDI TLV (see Figure 79–3). Type 3 and Type 4 PSEs can determine the PD Type based on the PDs Physical Layer requested Class (see 145.2.8 and 145.3.6.1) or based on the length of a received Power via MDI TLV (see Figure 79–3).

## MDI power support

The MDI power support field shall contain a bitmap of the MDI power capabilities and status as defined in Table 79–4.

**Table 79–3—Recommended TLV format**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Power entity A** | **Power entity B** | **Power entity A sends** | **Power entity B sends** | **Recommended TLV format** |
| Type 1, Type 2 | Type 1, Type 2 | 12-octet TLV | 12-octet TLV | 12-octet TLV |
| Type 3, Type 4 | Type 1, Type 2 | 29-octet TLV | 12-octet TLV | 12-octet TLV |
| Type 1, Type 2 | Type 3, Type 4 | 12-octet TLV | 29-octet TLV | 12-octet TLV |
| Type 3, Type 4 | Type 3, Type 4 | 29-octet TLV | 29-octet TLV | 29-octet TLV |

**Table 79–4—MDI power support field**

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 7:4 | Reserved for future standardization | — |
| 3 | PSE pairs control ability | 1 = pair selection can be controlled0 = pair selection can not be controlled |
| 2 | PSE MDI power state | 1 = enabled0 = disabled |
| 1 | PSE MDI power support | 1 = supported0 = not supported |
| 0 | Port class | 1 = PSE0 = PD |

* + - * 1. **Port class**

The ‘Port class’ field transmitted shall indicate if the port is a PSE or a PD.

## PSE MDI power support

The ‘PSE MDI power support’ field transmitted by a PSE shall indicate if MDI power is supported. The value of the ‘PSE MDI power support’ field transmitted by a PD is undefined.

## PSE MDI power state

The ‘PSE MDI power state’ field transmitted by a PSE shall indicate if the PSE function is enabled or disabled. When disabled all PSE functions are disabled and behavior is as if there was no PSE functionality. The value of the ‘PSE MDI power state’ field transmitted by a PD is undefined.

## PSE pairs control ability

The ‘PSE pairs control ability’ field transmitted by a PSE shall indicate if the PSE has the capability to control which PSE Pinout Alternative (see 33.2.3 and 145.2.4) is used for PD detection and power. The value of the ‘PSE pairs control ability’ field transmitted by a PD is undefined.

## PSE power pair

The ‘PSE power pair’ field transmitted by a PSE shall contain an integer value as defined in Table 79–5 based on aPSEPowerPairs (see 30.9.1.1.4). A Type 3 or Type 4 PSE that is supplying power on a single pairset shall use the value that defines that pairset. Either pairset may be indicated when a PSE is detecting or supplying power on both pairsets. The ‘PSE power status value’ field defined in 79.3.2.9 indicates when a PSE is supplying power on both pairsets. The value of the ‘PSE power pair’ field transmitted by a PD is undefined.

For MPoE systems, the value of 1 shall indicate that power is provided on the data pair. A value of 2 shall indicate that the power is provided on conductors other than the data pair carrying the LLDPDU.

## Table 79–5—PSE power pair field

|  |  |  |
| --- | --- | --- |
| **Value** | **Meaning** | **Alternative** |
| 1 | signal | Alternative A |
| 2 | spare | Alternative B |

* + - 1. **Power class**

The ‘Power class’ field transmitted by a PSE shall contain an integer value as defined in Table 79–6 based on aPSEPowerClassification (see 30.9.1.1.8). Class 4 and above is indicated with the same value in this field. Class 5 and above is communicated by the ‘Power Class ext’ field defined in 79.3.2.9.6. The ‘Power class’ field transmitted by a PD is undefined.

## Table 79–6—Power class field

|  |  |
| --- | --- |
| **Value** | **Meaning** |
| 1 | Class 0 PD |
| 2 | Class 1 PD |
| 3 | Class 2 PD |
| 4 | Class 3 PD |
| 5 | Class 4 and above PD |

For MPoE systems, this field shall contain the integer value of Unit Loads supported by an MPSE or required by an MPD.

* + - 1. **Power type/source/priority**

The ‘Power type/source/priority’ field shall contain a bit-map of the power type, source, and priority defined in Table 79–7 and is reported for the device generating the TLV.

## Power type

This field shall be set according to Table 79–7. Type 3 or Type 4 PSEs shall set this field to the value corresponding with Type 2 PSEs. Type 3 or Type 4 PDs shall set this field to the value corresponding with Type 2 PDs.

For MPOE systems, bit 6 shall be set for devices that support Type 0 and bit 7 shall be set for devices that support Type 1 operation.

## Table 79–7—Power type/source/priority field

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 7:6 | Power type | 71100 | 61010 | = Type 1 PD or Type 0 and 1 MPSE/MPD= Type 1 PSE or Type 1 MPSE/MPD= Type 2 PD or Type 0 MPSE/MPD= Type 2 PSE or MPoE Inactive |
| 5:4 | Power source | Where Power type = PD |
|  |  | 5 4 |
|  |  | 1 1 = PSE and local |
|  |  | 1 0 = Reserved |
|  |  | 0 1 = PSE |
|  |  | 0 0 = Unknown |
|  |  | Where Power type = PSE |
|  |  | 5 4 |
|  |  | 1 1 = Reserved |
|  |  | 1 0 = Backup source |
|  |  | 0 1 = Primary power source |
|  |  | 0 0 = Unknown |
| 3 | Reserved | Transmit as zero, ignore on receive |
| 2 | PD 4PID | 1 = PD supports powering of both Modes simultaneously0 = PD does not support powering of both Modes simultaneously |
| 1:0 | Power priority | 11100 | 01010 | = low= high= critical= unknown (default) |

* + - * 1. **Power source**

When the power type is PD, this field shall be set to 01 when the PD is being powered only through the PI; to 11 when the PD is being powered from both; and to 00 when this information is not available.

When the power type is PSE, this field shall be set to 01 when the PSE is sourcing its power through the PI from its primary supply; to 10 when the PSE is sourcing its power through the PI from a backup source; and to 00 when this information is not available.

## PD 4PID

This field shall be set according to Table 79–7 when the Power type is PD to indicate whether the PD supports powering of both Modes simultaneously. This field shall be set to ‘0’ when the Power type is PSE.

## Power priority

When the power type is PD, this field shall be set to the power priority configured for the device. If a PD is unable to determine its power priority or it has not been configured, then this field shall be set to 00.

When the power type is PSE, this field reflects the PD priority that the PSE advertises to assign to the PD.

## PD requested power value

The ‘PD requested power value’ field shall contain the PD’s requested power value defined in Table 79–8. See 33.6.3.3 and Table 145–42 for permitted value ranges.

## Table 79–8—PD requested power value field

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 15:0 | PD requested power value | Power expressed in units of 0.1 WValid values for these bits are decimal 0 through 999. |

## “PD requested power value” is the maximum input average power (see 33.3.7.2 and 145.3.8.2) the PD is requesting. “PD requested power value” is the power value at the PD PI. A value higher than 713 requires the PSE to support a power level higher than PClass\_PD at the PD PI. See 145.2.8 and 145.3.8.2.PSE allocated power value

The ‘PSE allocated power value’ field shall contain the PSE allocated power value defined in Table 79–9. See 33.6.3.3 and Table 145–41 for permitted value ranges.

## Table 79–9—PSE allocated power value field

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 15:0 | PSE allocated power value | Power expressed in units of 0.1 WValid values for these bits are decimal 0 through 999. |

“PSE allocated power value” is the maximum input average power (see 33.3.7.2 and 145.3.8.2) the PSE expects the PD to draw. “PSE allocated power value” is the power at the PD PI. The PSE uses this value to compute PClass as defined in 33.2.6 and 145.2.8. A value higher than 713 indicates that the PSE is capable of supporting a power level beyond PClass\_PD at the PD PI. This may require an output power level higher than PType min. See 145.2.8.

MPoE systems shall indicate the sum of all power allocations currently known.

## Dual-signature PD requested power value for Mode A and Mode B

The ‘PD requested power value Mode A’ field and ‘PD requested power value Mode B’ field shall contain the PD requested power value defined in Table 79–10 for Mode A and in Table 79–11 for Mode B of a dual- signature PD.

## Table 79–10—PD requested power value Mode A field

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 15:0 | Dual-signature PD requested power value for Mode A | Power expressed in units of 0.1 W.Valid values for these bits are decimal 0 through 499. |

**Table 79–11—PD requested power value Mode B field**

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 15:0 | Dual-signature PD requested power value for Mode B | Power expressed in units of 0.1 W.Valid values for these bits are decimal 0 through 499. |

The ‘PD requested power value Mode A’ field and ‘PD requested power value Mode B’ field are the maximum input average power levels (see 145.3.8.2) the PD is requesting for the respective Mode.

MPoE systems shall ignore this field.

## PSE allocated power value Alternative A and Alternative B

The ‘PSE allocated power value Alternative A’ field and the ‘PSE allocated power value Alternative B’ field shall contain the values in Table 79–12 and Table 79–13 for Type 3 and Type 4 PSEs operating over both pairsets when connected to a dual-signature PD.

## Table 79–12—PSE allocated power value Alternative A field

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 15:0 | PSE allocated power value for Alternative A | Power expressed in units of 0.1 W.Valid values for these bits are decimal 0 through 499. |

**Table 79–13—PSE allocated power value Alternative B field**

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 15:0 | PSE allocated power value for Alternative B | Power expressed in units of 0.1 W.Valid values for these bits are decimal 0 through 499. |

The ‘PSE allocated power value Alternative A’ and ‘PSE allocated power value Alternative B’ fields are the maximum input average power levels (see 145.3.8.2) the PSE expects the dual-signature PD to draw on the respective Alternatives when the PSE provides power over 4-pair. These fields are the power levels at the dual-signature PD PI. The PSE uses these values to compute PClass-2P as defined in 145.2.8.

For MPoE systems, the value for Alternative A shall indicate that power allocated on the data pair. The value for Alternative B shall indicate that the power is provided on conductors other than the data pair carrying the LLDPDU.

## Power status

The ‘Power status’ field contains the PSE's bit-map of the PSE power pair and PSE or PD power class, defined in Table 79–14, and is reported for the device generating the TLV.

Editors Note: this field still needs to be addressed if re-use of this TLV is accepted.

## Table 79–14—Power status field

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 15:14 | PSE powering status | 151 | 141 | = 4-pair powering dual-signature PD |
|  |  | 1 | 0 | = 4-pair powering single-signature PD |
|  |  | 0 | 1 | = 2-pair powering |
|  |  | 0 | 0 | = Reserved/Ignore |
| 13:12 | PD powered status | 131 | 121 | = 4-pair powered dual-signature PD |
|  |  | 1 | 0 | = 2-pair powered dual-signature PD |
|  |  | 0 | 1 | = Powered single-signature PD |
|  |  | 0 | 0 | = Reserved/Ignore |
| 11:10 | PSE power pairs ext | 111 | 101 | = Both Alternatives |
|  |  | 1 | 0 | = Alternative B |
|  |  | 0 | 1 | = Alternative A |
|  |  | 0 | 0 | = Reserved/Ignore |

**Table 79–14—Power status field *(continued)***

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 9:7 | Dual-signature | 9 | 8 | 7 |  |  |
|  | power Class ext Mode A | 1 | 1 | 1 | = Single-signature PD or 2-pair only PSE |
|  |  | 1 | 1 | 0 | = Reserved/Ignore |
|  |  | 1 | 0 | 1 | = Class 5 |
|  |  | 1 | 0 | 0 | = Class 4 |
|  |  | 0 | 1 | 1 | = Class 3 |
|  |  | 0 | 1 | 0 | = Class 2 |
|  |  | 0 | 0 | 1 | = Class 1 |
|  |  | 0 | 0 | 0 | = Reserved/Ignore |
| 6:4 | Dual-signature | 6 | 5 | 4 |  |  |
| power Class ext Mode B | 1 | 1 | 1 | = Single-signature PD or 2-pair only PSE |
|  |  | 1 | 1 | 0 | = Reserved/Ignore |
|  |  | 1 | 0 | 1 | = Class 5 |
|  |  | 1 | 0 | 0 | = Class 4 |
|  |  | 0 | 1 | 1 | = Class 3 |
|  |  | 0 | 1 | 0 | = Class 2 |
|  |  | 0 | 0 | 1 | = Class 1 |
|  |  | 0 | 0 | 0 | = Reserved/Ignore |
| 3:0 | Power Class ext | 31 | 21 | 11 | 01 | = Dual-signature PD |
|  |  | 1 | 1 | 1 | 0 | = Reserved/Ignore |
|  |  | 1 | 1 | 0 | 1 | = Reserved/Ignore |
|  |  | 1 | 1 | 0 | 0 | = Reserved/Ignore |
|  |  | 1 | 0 | 1 | 1 | = Reserved/Ignore |
|  |  | 1 | 0 | 1 | 0 | = Reserved/Ignore |
|  |  | 1 | 0 | 0 | 1 | = Reserved/Ignore |
|  |  | 1 | 0 | 0 | 0 | = Class 8 |
|  |  | 0 | 1 | 1 | 1 | = Class 7 |
|  |  | 0 | 1 | 1 | 0 | = Class 6 |
|  |  | 0 | 1 | 0 | 1 | = Class 5 |
|  |  | 0 | 1 | 0 | 0 | = Class 4 |
|  |  | 0 | 0 | 1 | 1 | = Class 3 |
|  |  | 0 | 0 | 1 | 0 | = Class 2 |
|  |  | 0 | 0 | 0 | 1 | = Class 1 |
|  |  | 0 | 0 | 0 | 0 | = Reserved/Ignore |

## PSE powering status

The ‘PSE powering status’ field is used to indicate the existing powering configuration as shown in Table 145–41 and thus to indicate that the PSE is using the ‘PSE allocated power value’ field or is using the ‘PSE allocated power value Alternative A’ field and ‘PSE allocated power value Alternative B’ field as specified in Table 79–12 and Table 79–13. A PSE shall set this field according the current powering status as defined in Table 79–14. A PD shall set the field to 0.

## PD powered status

The ‘PD powered status’ field is used to indicate the existing powered configuration of the PD as shown in Table 145–42 and thus to indicate that the PD is using the ‘PD requested power value’ field or is using the ‘PD requested power value Mode A’ field and the ‘PD requested power value Mode B’ field as specified in Table 79–10 and Table 79–11. A PD shall set this field according to its signature configuration and the current powering status as defined in Table 79–14. A PSE shall set the field to 0.

## PSE power pairs ext

The ‘PSE power pairs ext’ field shall contain the powering status of the PSE, as defined in Table 79–14. A PD shall set the field to 0.

## Dual-signature power Class ext Mode A

A single-signature PD shall set this field to value 7. A dual-signature PD shall set this field per its requested Class on Mode A defined in 145.3.6. A 2-pair only PSE or a PSE connected to a single-signature PD shall set this field to value 7. A PSE connected to a dual-signature PD shall set this field to the PSEs assigned Class for Alternative A as defined in 145.2.8.

## Dual-signature power Class ext Mode B

A single-signature PD shall set this field to value 7. A dual-signature PD shall set this field per its requested Class on Mode B defined in 145.3.6. A 2-pair only PSE or a PSE connected to a single-signature PD shall set this field to value 7. A PSE connected to a dual-signature PD shall set this field to the PSEs assigned Class for Alternative B as defined in 145.2.8.

## Power Class ext

A single-signature PD shall set this field per its requested Class as defined in 145.3.6. A dual-signature PD shall set this field to value 15. A 2-pair only PSE or a PSE connected to a single-signature PD shall set this field to the PSEs assigned Class as defined in 145.2.8. A PSE connected to a dual-signature PD shall set this field to value 15.

## System setup

The ‘System setup’ field shall contain the device bit-map of the Power Type ext and PD Load defined in Table 79–15 and is reported for the device generating the TLV.

## Table 79–15—System setup field

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 7:4 | Reserved | Transmit as zero. Ignore on receive. |
| 3:1 | Power Type ext | 3 2 11 1 1 = Reserved / ignore1 1 0 = Reserved / ignore1 0 1 = Type 4 dual-signature PD1 0 0 = Type 4 single-signature PD0 1 1 = Type 3 dual-signature PD0 1 0 = Type 3 single-signature PD0 0 1 = Type 4 PSE0 0 0 = Type 3 PSE |
| 0 | PD Load | 1 = PD is dual-signature and power demand on Mode A and Mode B are electrically isolated.0 = PD is single-signature or dual-signature and power demand on Mode A and Mode B are not electrically isolated. |

* + - * 1. **Power Type ext**

This field shall be set according to Table 79–15.

## PD Load

This field shall be set according to Table 79–15 when the Power type is PD. This field shall be set to 0 when the Power type is PSE. See 145.4.1 for details.

## PSE maximum available power value

The ‘PSE maximum available power value’ field shall contain the highest power the PSE can grant as defined in Table 79–16. The PSE sets the value of this field taking available power budget and hardware capabilities into account. When connected to a dual-signature PD this value refers to the total amount of power available at the PI, even though power is allocated separately on a per pairset basis. A PD shall set this field to 0.

## Table 79–16—PSE maximum available power value field

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 15:0 | PSE maximum available power value | Power expressed in units of 0.1 W.Valid values for these bits are 1 through 999. |

* + - 1. **Autoclass**

The ‘Autoclass’ field shall contain the bits defined in Table 79–17 to control Autoclass. See 145.2.8.2 and

145.3.6.2 for details on Autoclass. Using the ‘Autoclass’ field to trigger a new Autoclass measurement allows a PD to change maximum power consumption.

## Table 79–17—Autoclass field

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 7:3 | Reserved | Transmit as zero. Ignore on receive. |
| 2 | PSE Autoclass support | 1 = PSE supports Autoclass0 = PSE does not support Autoclass |
| 1 | Autoclass completed | 1 = Autoclass measurement completed 0 = Autoclass idle |
| 0 | Autoclass request | 1 = PD requests Autoclass measurement 0 = Autoclass idle |

* + - * 1. **PSE Autoclass support**

When the Power type is PSE, this field shall be set to indicate if the PSE supports Autoclass over DLL according to Table 79–17. When the Power type is PD, this field shall be set to 0.

## Autoclass completed

When the Power type is PSE, this field shall be set to indicate that the PSE has concluded the Autoclass measurement. This happens after a request for Autoclass is made by the PD using the ‘Autoclass request’ field defined in Table 79–17. When the Power type is PD, this field shall be set to 0.

## Autoclass request

When the Power type is PD, this field may be set to 1 to request a Autoclass measurement by the PSE. The PD sets this field when it is in a state where it consumes its maximum amount of power. In all other cases, the PD sets this field to 0. When the Power type is PSE, this field shall be set to 0.

## Power down

The ‘Power down’ field shall contain the bits defined in Table 79–18. The ‘Power down’ field allows the PD to request power delivery to be terminated, either indefinitely or for a certain period of time.

## Table 79–18—Power down field

|  |  |  |
| --- | --- | --- |
| **Bit** | **Function** | **Value/meaning** |
| 23:18 | Power down request | Value = 0x1D requests a power down. Any other value is ignored. |
| 17:0 | Power down time | The amount of time in seconds the PD requests to be unpowered. A value of zero means to remain unpowered indefinitely.Valid values are 0 through 262 143. |

* + - * 1. **Power down request**

When the Power type is PD, this field may be set to 0x1D to indicate a request for power down. If power is to be maintained, the field shall be set to 0. When the Power type is PSE, this field shall be set to 0.

## Power down time

This field controls the amount of time in seconds the PD is requesting to be unpowered. When the Power type is PD, this field shall be set per the description in Table 79–18. When the Power type is PSE, this field shall be set to 0.

## Power Via MDI TLV usage rules

An LLDPDU should contain no more than one Power Via MDI TLV.

#### 79.3.9 PLCA TLV

The PLCA TLV is an optional TLV that indicates capabilities and status of [Clause 148](#_bookmark134) PLCA. [Figure 79–10](#_bookmark120)

shows the format of this TLV.

**

Figure 79–10—PLCA TLV format

#### PLCA support/status

The PLCA support/status field shall contain a bitmap that identifies the PLCA and D-PLCA support and

status of the local IEEE 802.3 LAN station as defined in [Table 79–21.](#_bookmark124)

* + - 1. **PLCA nodeID**

The PLCA nodeId field contains an integer value indicating the PLCA nodeId of the local IEEE 802.3 LAN

station.

#### PLCA TLV usage rules

An LLDPDU should contain no more than one PLCA TLV. Since this TLV is intended to inform a link

partner of capabilities, the PLCA TLV should be sent in an LLDPDU addressed to the Nearest Bridge group

address (see IEEE 802.1Q). If PLCA is not enabled, this field reports 255.

#### Table 79–21—PLCA support/status

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Field** | **Length (Octets)** | **Format** | **Field definitions** | **Value/Values** | **Notes** |
| PLCA support/status | 2 | Bitmap | Bit 0 – PLCA supported | 1 = supported0 = not supported | [30.16.1.1.13](#_bookmark38) |
| Bit 1 – PLCA status | 1 = TRUE0 = FALSE | 30.16.1.1.2 |
| Bit 2 – PLCA admin state | 1 = enabled0 = disabled | 30.16.1.1.1 |
| Bit 3 – D-PLCA sup- ported | 1 = supported0 = not supported | [30.16.1.1.14](#_bookmark40) |
| Bit 4 – D-PLCA admin state | 1 = enabled0 = disabled | [30.16.1.1.11](#_bookmark35) |
| Bits 5 to 15 | Reserved |  |
| PLCA nodeID | 1 | Unsigned Integer | 0 to 255 | 0 to 255 | 30.16.1.1.4 |

#### Topology Discovery TLV

The Topology Discovery TLV is a mandatory TLV that coordinates indicates capabilities and status of 10BASE-T1S and 10BASET-1M mixing segment discovery agents. Figure 79-xx shows the format of this TLV.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| TLV type = | TLV information | 802.3 OUI | 802.3 | Topology discovery support/ | Topology discovery target node | Topology Discovery Internal Delay Measurement Results |
| 127 | string length = 9 | 00-12-0F | subtype = 10 | status | targetNode | internalDelay |
| 7 bits | 9 bits | 3 octets | 1 octet | 2 octets | 6 octects | 4 octets |
| TLV Header | TLV Header | TLV Info Str | TLV Info Str | TLV Info Str | TLV Info Str | TLV Info Str |

Figure 79–xx—Topology Discovery TLV format

#### Topology discovery support/status

The topology discovery support/status field shall contain a bitmap that identifies the topology discovery support and

status of the local IEEE 802.3 LAN station as defined in [Table 79–xx.](#_bookmark124)

* + - 1. Topology discovery targetNode

The topology discovery targetNode field contains the MAC address of the station that is permitted to perform a internal delay measurement or is required to respond to a measurement process.

* + - 1. Topology discovery **internalDelay**

The topology discovery internalDelay field contains an unsigned integer value indicating the results of the local IEEE 802.3 LAN station’s most recent internal delay measurement.

#### Topology discovery TLV usage rules

An LLDPDU shall contain no more than one topology discovery TLV.

#### Table 79–xx— Topology discovery support/status

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Field** | **Length (Octets)** | **Format** | **Field definitions** | **Value/Values** | **Notes** |
| Topology discovery support/status | 2 | Bitmap | Bit 0 –topology discovery mute supported | 1 = supported0 = not supported |  |
| Bit 1 – topology discovery measurement supported | 1 = supported0 = not supported |  |
| Bit 2 – topology discovery target mode supported | 1 = supported0 = not supported |  |
| Bit 3 – topology discovery internal delay measurement supported | 1 = supported0 = not supported |  |
| Bit 4 – topology discovery internal delay measurement valid | 1 = internalDelay field is valid0 = internalDelay field is invalid |  |
| Bit 5 – topology discovery target node internal delay measurement requested | 1 = targetNode requested to perform internal delay measurement0 = targetNode not currently allowed to perform internal delay measurements |  |
| Bit 6 – topology discovery target node measurement response requested | 1 = targetNode requested to respond to measurement process0 = targetNode not permitted to respond to measurement process |  |
| Bits 7 to 15 | Reserved |  |

#### 79.3.11 Hibernation Control TLV

The Hibernation Control TLV is an optional TLV that indicates capabilities and status of 10BASE-T1S and 10BASET-1M mixing segment nodes capable of power modes so low that they no longer respond to Ethernet frames while hibernating. Figure 79-xx shows the format of this TLV.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| TLV type = | TLV information | 802.3 OUI | 802.3 | Hibernation Control support/ | Hibernation Control target node count | Hibernation Control target nodes |
| 127 | string length = 9 | 00-12-0F | subtype = 11 | status | targetNodeCount | targetNodes |
| 7 bits | 9 bits | 3 octets | 1 octet | 2 octets | 2 octets | 6 octets \* NumNodes |
| TLV Header | TLV Header | TLV Info Str | TLV Info Str | TLV Info Str | TLV Info Str | TLV Info Str |

Figure 79–xx—Hibernation Control TLV format

#### Hibernation Control support/status

The Hibernation Control support/status field shall contain a bitmap that identifies the Hibernation Control support and

status of the local IEEE 802.3 LAN station as defined in [Table 79–xx.](#_bookmark124)

* + - 1. Hibernation Control targetNodeCount

The Hibernation Control targetNodes field contains the 16-bit unsigned integer representing the number of MAC addresses present in the targetNodes list.

* + - 1. Hibernation Control targetNodes

The Hibernation Control targetNodes field contains the MAC addresses of the stations that are permitted to return to a hibernating state following an out-of-band wake up event. The length of this field is 6 octets \* targetNodeCount.

#### Hibernation Control TLV usage rules

An LLDPDU shall contain no more than one Hibernation Control TLV.

#### Table 79–xx— Hibernation Control support/status

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Field** | **Length (Octets)** | **Format** | **Field definitions** | **Value/Values** | **Notes** |
| Hibernation Control support/status | 2 | Bitmap | Bit 0 –Hibernation Coordinator Role supported | 1 = supported0 = not supported |  |
| Bit 1 – Hibernation wake event reception supported | 1 = supported0 = not supported |  |
| Bit 2 – Hibernation Coordinator Role active | 1 = sender is acting as a hibernation coordinator0 = sender is not acting as a hibernation coordinator |  |
| Bit 3 – Hibernation Control internal delay measurement supported | 1 = supported0 = not supported |  |
| Bits 4 to 7 | Reserved |  |

#### 79.3.12 Dynamic Power Allocation TLV

The Dynamic Power Allocation TLV is an optional TLV that negotiates a time limited dynamic power grant.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| TLV type = | TLV information | 802.3 OUI | 802.3 | Dynamic Power Allocation support/ | Dynamic Power Allocation entry count | Dynamic Power Allocation entry list |
| 127 | string length = 9 | 00-12-0F | subtype = 12 | status | entryCount | requestEntries |
| 7 bits | 9 bits | 3 octets | 1 octet | 2 octets | 2 octets | xx octets \* entryCount |
| TLV Header | TLV Header | TLV Info Str | TLV Info Str | TLV Info Str | TLV Info Str | TLV Info Str |

Figure 79–xx—Dynamic Power Allocation TLV format

#### Dynamic Power Allocation support/status

The Dynamic Power Allocation support/status field shall contain a bitmap that identifies the Dynamic Power Allocation support and status of the local IEEE 802.3 LAN station as defined in [Table 79–xx.](#_bookmark124)

* + - 1. Dynamic Power Allocation entryCount

The Dynamic Power Allocation entryCount field contains the number of requestEntries in the grantEntries field.

* + - 1. Dynamic Power Allocation requestEntries

The Dynamic Power Allocation requestEntries field contains a packed list of Dynamic Power Allocation Entries as defined in Table 79-xx. Both power supplies and powered devices utilize the same entry structure. In the case of a multi-device powering system, more than one entry may be present.

#### Dynamic Power Allocation TLV usage rules

An LLDPDU shall contain no more than one Dynamic Power Allocation TLV.

#### Table 79–xx— Dynamic Power Allocation support/status

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Field** | **Length (Octets)** | **Format** | **Field definitions** | **Value/Values** | **Notes** |
| Dynamic Power Allocation support/status | 2 | Bitmap | Bit 0 –Dynamic power allocation supported | 1 = supported0 = not supported |  |
| Bit 1 –Dynamic power allocation role | 1 = power supply0 = powered device |  |
| Bits 2 to 7 | Reserved |  |

#### Table 79–xx— Dynamic Power Allocation Entry

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Field** | **Length (Octets)** | **Format** | **Field definitions** | **Value/Values** | **Notes** |
| MAC Address | **6** | MAC Address | MAC Address of the powered device affected by this grant entry | MAC Address |  |
| Requested Additional Power | **1** | Unsigned Integer | Number of additional unit loads requested by the powered device | Number of Unit Loads |  |
| Requested Additional Power Duration | **2** | Unsigned Integer | Duration in seconds requested for the additional power grant | Grant duration requested in seconds |  |
| Requested Additional Power Use Delay | **2** | Unsigned Integer | Time in seconds until the additional power will be used | Delay duration in seconds |  |
| Granted Additional Power | **1** | Unsigned Integer | Number of additional unit loads granted by the power supply | Number of Unit Loads |  |
| Granted Additional Power Duration | **2** | Unsigned Integer | Duration in seconds granted for the additional power grant | Grant duration requested in seconds |  |
| Granted Additional Power Use Delay | **2** | Unsigned Integer | Time in seconds until the additional power may be used | Delay duration in seconds |  |

## 79.5 Protocol implementation conformance statement (PICS) proforma for IEEE 802.3

## Organizationally Specific Link Layer Discovery Protocol (LLDP) type, length, and

## value (TLV) information elements

#### 79.5.3 Major capabilities/options

##### Insert new row to the end of the protocol implementation conformance statement (PICS) proforma as

##### follows (unchanged rows and unchanged footnote number 142 in subclause 79.5 not shown):

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| \*PL | PLCA TLV | [79.3.9](#_bookmark119) |  | O | Yes [ ]No [ ] |

*Insert new subclause 79.5.13 after 79.5.12 as follows:*

####

#### 79.5.13 PLCA TLV

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Item** | **Feature** | **Subclause** | **Value/Comment** | **Status** | **Support** |
| PLC1 | PLCA support/status field | [79.3.9.1](#_bookmark121) | Contains a bitmap identifying PLCA and D-PLCA support defined in [Table 79–21](#_bookmark124) | PL:M | Yes [ ]N/A [ ] |
| PLC2 | PLCA nodeID field | [79.3.9.2](#_bookmark122) | Contains an integer value indi- cating the PLCA nodeId | PL:M | Yes [ ]N/A [ ] |
| PLC3 | PLCA TLV usage rules | [79.3.9.3](#_bookmark123) | PLCA support/status TLV should contain no more than one PLCA TLV | PL:O | Yes [ ]No [ ]N/A [ ] |