# Type 0 Power Parameter Updates

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# Channel V / I / P / R Assumptions

Desire for industrial compatible supply voltages

- Type 0 MPSE:  24V +/- 20% => 21.6V to 26.4V

Desire to align power consumption with ODVA

- PMPD_TYPE0 = 1.1W

Requirement to reach 50m with 16 nodes

- Assume 50m 20AWG cable @ 65C =~ 4Ω
- Assume 20cm node separation
- 16 Nodes at end of mixing segment

Requirement to stay above 16V at last MPD

The last degree of freedom in solving the system is the resistance through each node

**Table 189–1—System power types**

| | 30V Max MPSE (Type 0) | 50V Max MPSE (Type 1) | Units |
|---|---|---|---|
| $V_{MPSE}$ max | 30 | 50 | V |
| $V_{MPSE}$ min | ~~26~~ 21.6 | 45 | V |
| $V_{MPD}$ min | 16 | 34 | V |
| $I_{MPSE}$ min | ~~1000~~ 1100 | 1000 | mA |
| $P_{MPSE}$ min | ~~26~~ 23.76 | 45 | W |
| $P_{MPD\_1U}$ max | ~~1~~ 1.1 | 2 | W |

# Existing Presentations on Connector Resistance

Resistance through a node is made up of resistance due to connectors and resistance due to compensation

Connection resistance references:

https://ieee802.org/3/da/public/0724/Voss_01_da_2024_07_10.pdf

https://ieee802.org/3/da/public/0124/boyer_3da_RevB_01_24_24.pdf

Bob Voss's data suggests we need ~ 75mΩ allocated to connection resistance per node

- 15mΩ max resistance per connection (4 connections per node)
- Add ~20% for temperature

Currently the specification allocates 100mΩ to loop resistance between TC1 and TC2

- 75mΩ allocated to connectors
- 25mΩ left to allocate to 2 compensation elements (input / output elements)
- 25mΩ may be too low…

# Compensation Elements

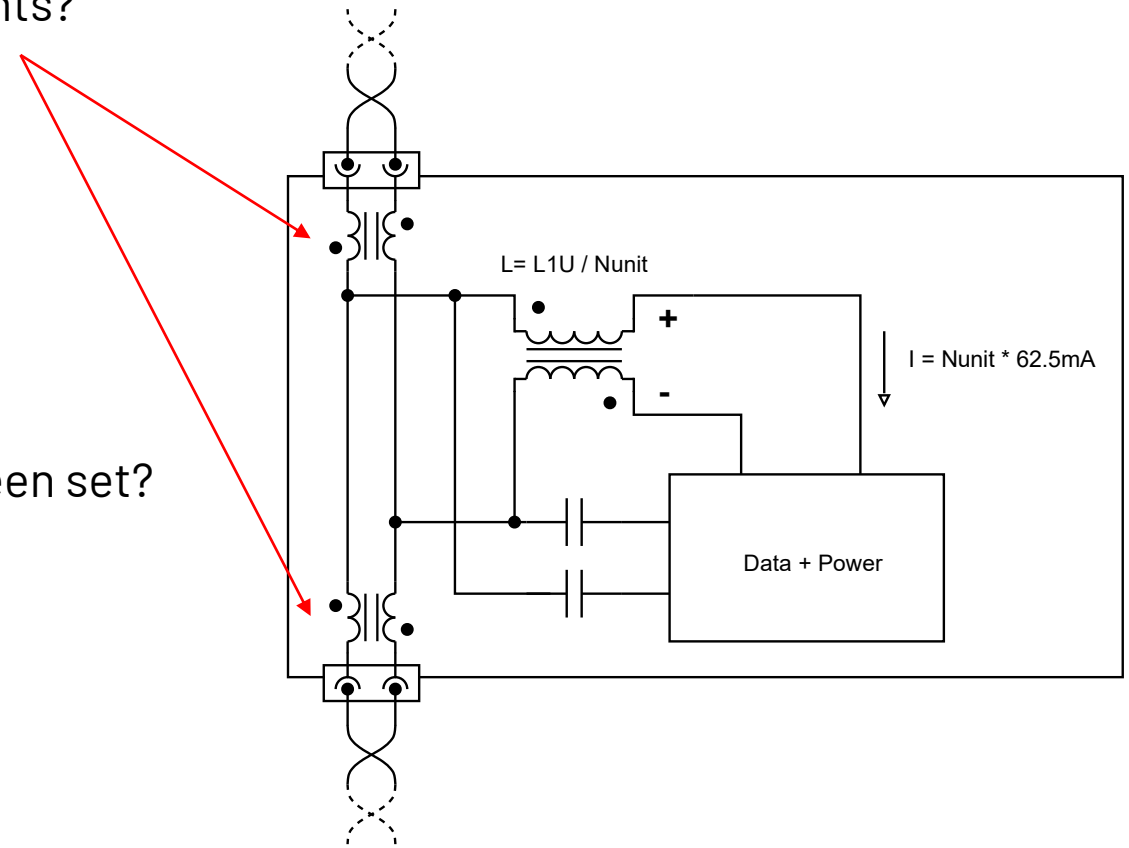
Low resistance / high current (>2A Isat) ~150nH coupled inductors are unique.

Not impossible to make, but not common yet

We need to set a target for vendors that pushes the limits, but does not push cost too hard

What is a good target resistance for these unique elements?

What is left in the budget after other parameters have been set?

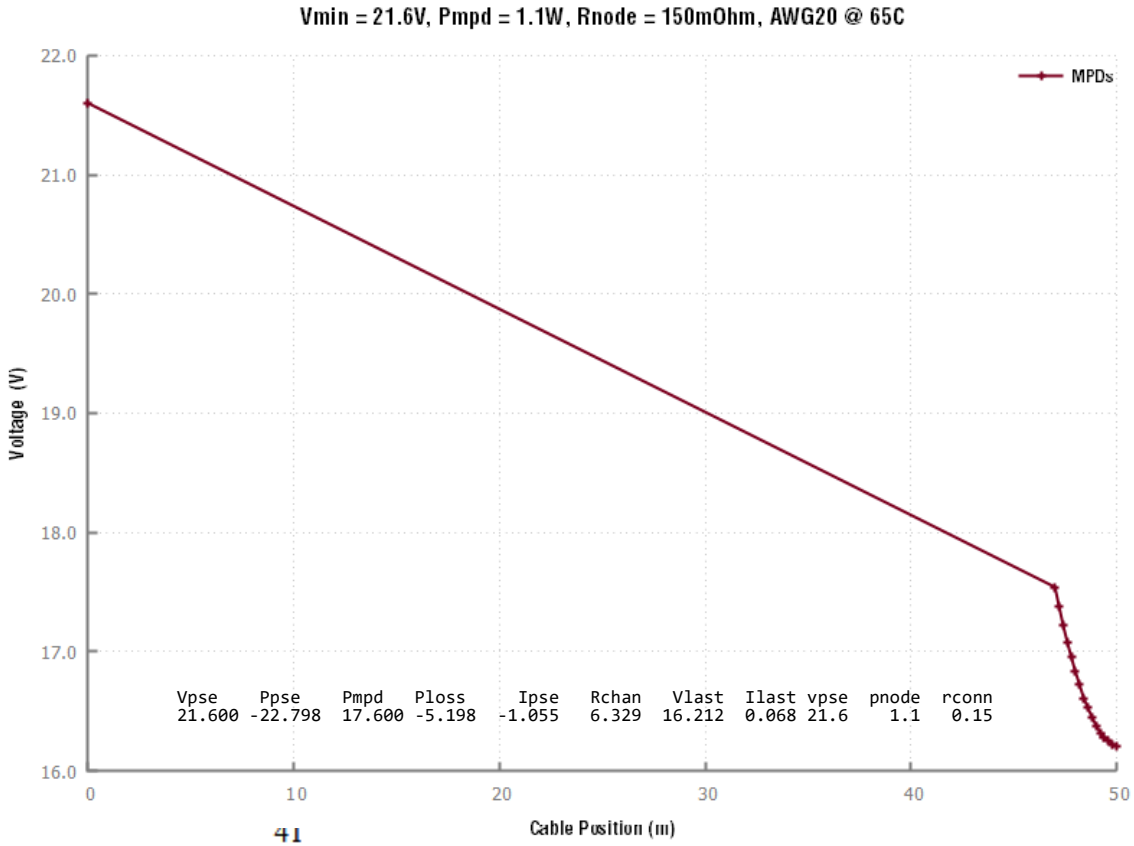


# Power Budgeting for Type 0

Set other desirable parameters, then adjust DTE loop resistance until last node is above 16V

**Table 189–1—System power types**

| | 30V Max MPSE (Type 0) | 50V Max MPSE (Type 1) | Units |
|---|---|---|---|
| $V_{MPSE}$ max | 30 | 50 | V |
| $V_{MPSE}$ min | ~~26~~ 21.6 | 45 | V |
| $V_{MPD}$ min | 16 | 34 | V |
| $I_{MPSE}$ min | ~~1000~~ 1100 | 1000 | mA |
| $P_{MPSE}$ min | ~~26~~ 23.76 | 45 | W |
| $P_{MPD\_1U}$ max | ~~1~~ 1.1 | 2 | W |




### 189.2 Mixing segment

The mixing segment consists of cable, nodes, and terminations (see Figure 189–1). 100 Ω terminations are connected at the ends of the mixing segment and must be AC coupled. The DC loop resistance of the cable (excluding connectors and attached DTEs) shall be less than or equal to 4 Ω.

This resistance budget is based on supporting up to 17 in-line nodes (1 MPSE and 16 MPDs). Each DTE, including mated connectors and compensation components, adds up to 100 mΩ to the loop resistance.

150

Edits Satisfy D2.1 Comments:
87, 88, 89, 90, 91

# Each DTE adds 150mΩ

Set resistance through each node to 150mΩ

Allocates ~75mΩ to connectors

Allocates ~75mΩ to compensators

Achieves other power deliver goals (Vmpse_type0_min, Pmpd_type0, #Nodes, 50m Reach)

**189.2 Mixing segment**

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This resistance budget is based on supporting up to 17 in-line nodes (1 MPSE and 16 MPDs). Each DTE, including mated connectors and compensation components, adds up to ~~100~~ 150 mΩ to the loop resistance.

# MPSE / MPD Table Changes

**Table 189–5—PSE output requirements**

Replace w/ emdash

| Item | Parameter | Symbol | Unit | Min | Max | Type | Additional Information |
|---|---|---|---|---|---|---|---|
| 1 | DC output voltage during POW-ER_ON state | $V_{MPSE}$ | V | ~~26~~ 21.6 | 30 | 0 | |
| | | | | 45 | 50 | 1 | |
| 2 | Continuous output capability in POWER_ON state | $P_{MPSE}$ | W | ~~26~~ 23.76 | ~~100~~ | 0 | See 189.4.7 |
| | | | | 45 | ~~100~~ | 1 | |
| 3 | Output slew rate dV/dt | | V/ms | - | 9.5 | ALL | |
| 4 | Output current - at short circuit condi-tion | $I_{LIM}$ | A | ~~1.1~~ 1.2 | ~~1.4~~ 2.3 | ALL | See 189.4.9 |
| 5 | Short-circuit time limit | $T_{LIM}$ | ms | 50 | 75 | ALL | See 189.4.9 |
| 6 | Inrush time | $T_{Inrush}$ | ms | 10 | 20 | ALL | |
| 7 | MPD maintain power signature dropout time limit | $T_{TPSDO}$ | ms | 320 | 400 | ALL | See 189.4.10.1 |
| 8 | PD TPS time for validity | $T_{TPS}$ | ms | 6 | - | ALL | See 189.4.10.1 |
| 9 | DC TPS current | $I_{HOLD}$ | mA | 4 | 9 | ALL | See 189.4.10.1 |
| 10 | Error delay timing | $T_{ED}$ | ms | 750 | - | ALL | |
| 11 | Overload current | $I_{CUT}$ | A | $P_{MPSE}$/ $V_{MPSE}$ | - | ALL | See 189.4.8 |
| 12 | Overload time limit | $T_{CUT}$ | ms | 50 | 70 | ALL | See 189.4.8 |

**Table 189–9—MPD power supply limits**

| Item | Parameter | Symbol | Unit | Min | Max | Type | Additional Information |
|---|---|---|---|---|---|---|---|
| 1 | Input voltage | $V_{Port\_MPD}$ | V | 16 | 30 | 0 | |
| | | | | 34 | 50 | 1 | |
| 2 | Unit power | $P_{MPD\_1U}$ | W | | ~~1~~ 1.1 | 0 and 0/1 | 1 unit load |
| | | | | | 2 | 1 | 1 unit load |
| 3 | Unit loading | $N_{unit}$ | - | 1 | 16 | ALL | See 189.5.5.3 |
| 4 | Input power | $P_{MPD}$ | W | ~~1~~ 1.1 | ~~16~~ 17.6 | 0 and 0/1 | $N_{unit}$ x $P_{MP-D\_1U}$ |
| | | | | 2 | 32 | 1 | |
| 5 | Inrush current | $I_{Inrush\_MPD}$ | mA | - | 10 | ALL | See 189.5.5.2 |
| 6 | MPD Type 0 Voltage threshold | $V_{type0\_th}$ | V | 11.9 | 16 | ALL | |
| 7 | MPD Type 1 Voltage threshold | $V_{type1\_th}$ | V | 30.1 | 34 | ALL | |

Edits Satisfy D2.1 Comments:
84, 93, 94, 95, 96, 97