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MPD Power On State Machine Edits

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MPD PON State Machine Issues

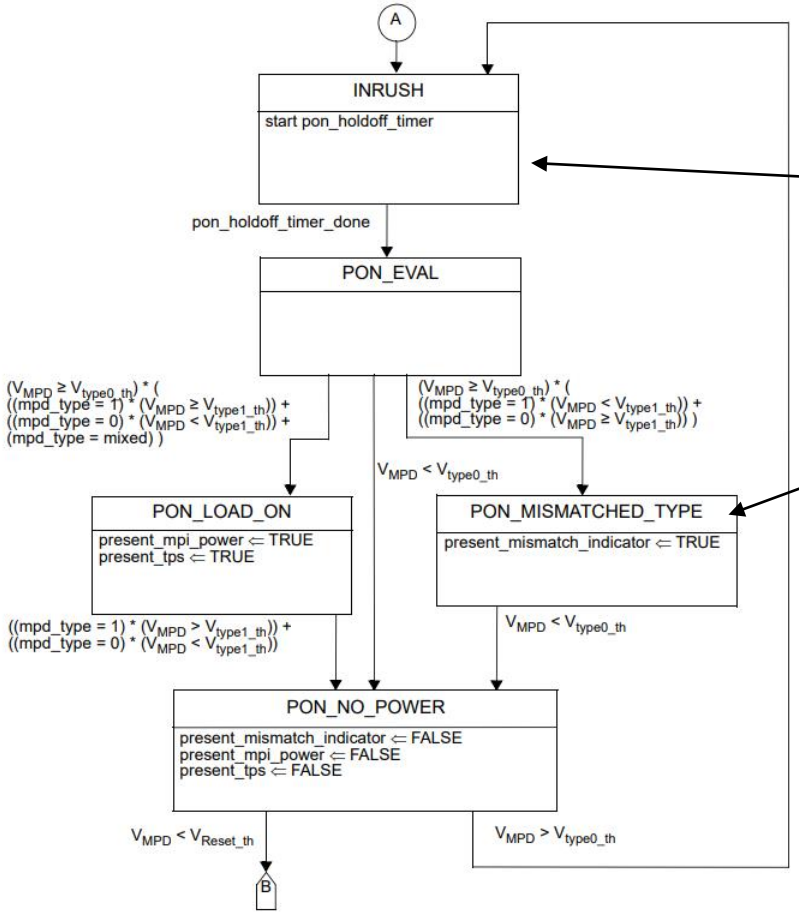

Figure 169–8—Top level MPD state diagram continued, part c

- INRUSH should only precede states where present_mpi_power <= True
- PON_MISMATCHED_TYPE state not needed
  - PON_MISMATCHED_TYPE and PON_NO_POWER are effectively the same states
  - Both are entered when MPD voltage is not in correct operating region
- Fix the arc logic

Discovery Issues

- V_{On_MPD} overlaps mark event voltage
- Mark and Power On must be differentiated with a timer
- Existing DO_MARKx exits do not make sense

Table 169–7—MPD discovery parameters

Item	Parameter	Symbol	Min	Max	Units	Additional Information
1	Mark event voltage	V_{MPD_mark}	16	19.1	V	

Table 169–8—MPD power supply limits

Item	Parameter	Symbol	Unit	Min	Max	Type	Additional Information
1	Input voltage	VPort_MPD	V	16	30	0	
				34	50	1	

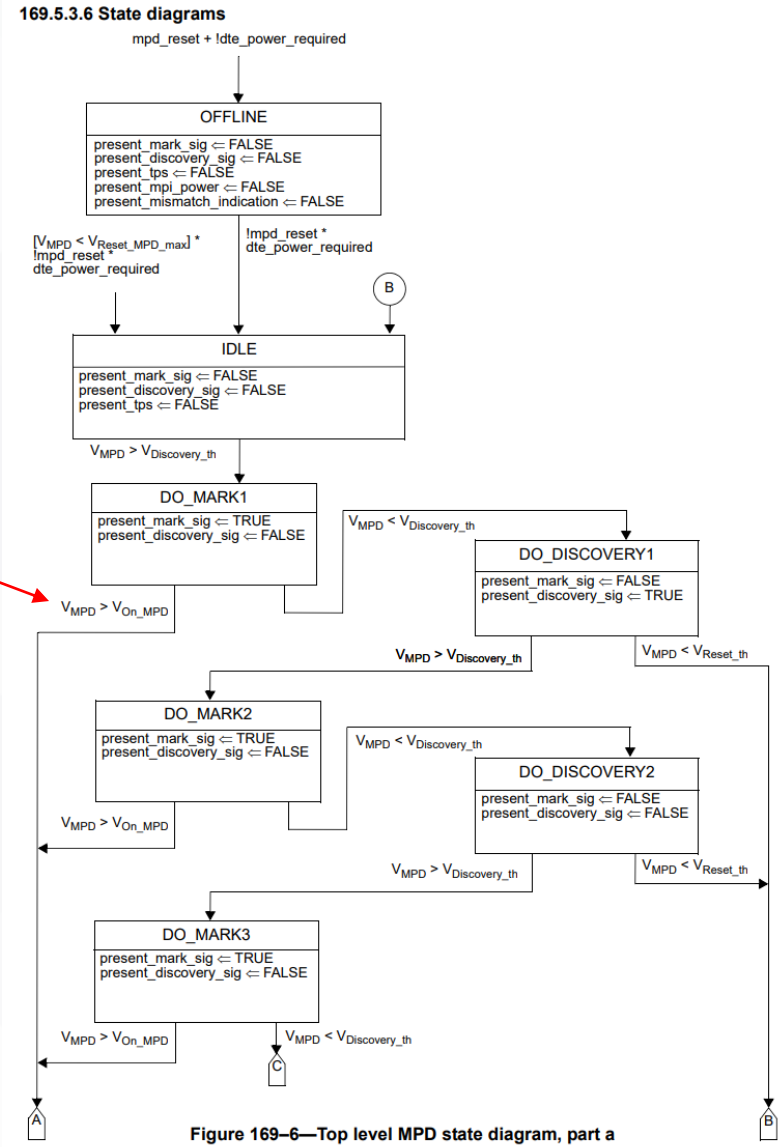

Figure 169–6—Top level MPD state diagram, part a

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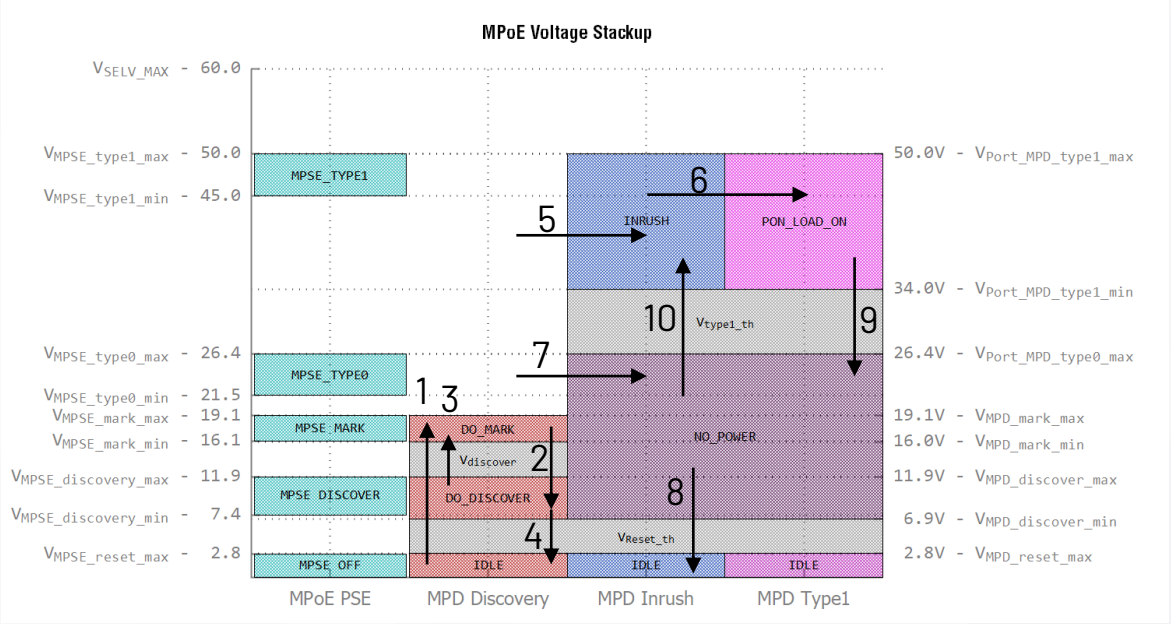
State Machine Analysis

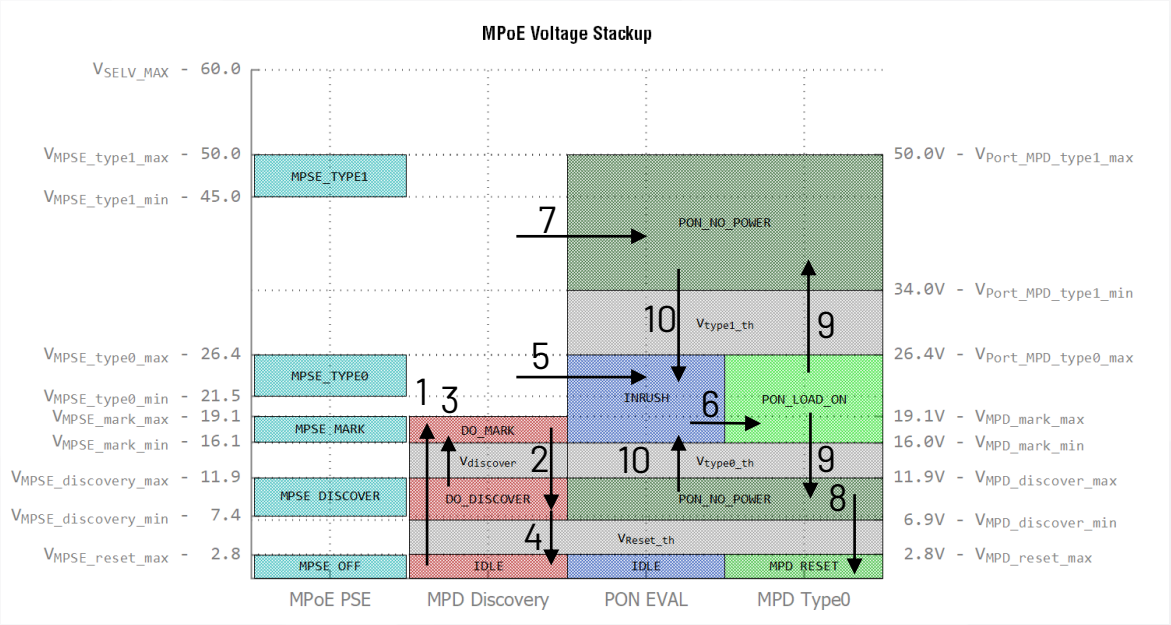
Type 1 MPD States

ARC	last state	next state	condition	note
1	IDLE	DO_MARK1	V_{MPD} > V_{Discovery_th}	start mark timer needs to be added to state machine
2	DO_MARKx	DO_DISCOVERYx	V_{MPD} < V_{Discovery_th}	
3	DO_DISCOVERYx	DO_MARK(x+1)	V_{MPD} > V_{Discovery_th}	start mark timer needs to be added to state machine
4	DO_DISCOVERYx	OFFLINE		discovery2 arcs go to IDLE instead of OFFLINE in current state machine? What is the difference between offline and idle
5	MPD_MARKx	INRUSH	mark_timer_done * V_{MPD} > V_{type1_th}	fix this in state machine, need to go to PON_EVAL 1st, then PON_INRUSH if we are arcing to POWER_ON
6	INRUSH	PON_LOAD_ON	INRUSH COMPLETE - Define Condition	
7	MPD_MARKx	PON_NO_POWER	mark_timer_done * V_{MPD} < V_{type1_th}	Move through "PON_EVAL" 1st.
8	PON_NO_POWER	IDLE	V_{MPD} < V_{Reset_th}	
9	PON_LOAD_ON	PON_NO_POWER	V_{MPD} < V_{type1_th}	Consider timing and what happens at PI vs. behind recitifer and bulk caps. PI voltage and internal voltage can get out of sync
10	PON_NO_POWER	PON_LOAD_ON	V_{MPD} > V_{type1_th}	Any timing or hysteresis requirements to stop a 10-6-9 loop?



Type 0 MPD States

ARC	last state	next state	condition	note
1	IDLE	DO_MARK1	V_{MPD} > V_{Discovery_th}	start mark timer needs to be added to state machine
2	DO_MARKx	DO_DISCOVERYx	V_{MPD} < V_{Discovery_th}	
3	DO_DISCOVERYx	DO_MARK(x+1)	V_{MPD} > V_{Discovery_th}	start mark timer needs to be added to state machine
4	DO_DISCOVERYx	IDLE		Discovery arcs go to IDLE instead of OFFLINE in current state machine? What is the difference between offline and idle
5	MPD_MARKx	INRUSH	mark_timer_done * V_{MPD} > V_{type0_th} * V_{MPD} < V_{type1_th}	fix this in state machine, need to go to PON_EVAL 1st, then PON_INRUSH if we are arcing to POWER_ON
6	INRUSH	PON_LOAD_ON	INRUSH COMPLETE - Define Condition	
7	MPD_MARKx	PON_NO_POWER	mark_timer_done * V_{MPD} < V_{type0_th} + V_{MPD} > V_{type1_th}	Move through "PON_EVAL" 1st
8	PON_NO_POWER	IDLE	V_{MPD} < V_{Reset_th}	
9	PON_LOAD_ON	PON_NO_POWER	V_{MPD} < V_{type0_th} + V_{MPD} > V_{type1_th}	Consider timing and what happens at PI vs. behind rectifier and bulk caps. PI voltage and internal voltage can get out of sync
10	PON_NO_POWER	PON_LOAD_ON	V_{MPD} > V_{type0_th} * V_{MPD} < V_{type0_th}	Any timing or hysteresis requirements to stop a 10-6-9 loop?



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Proposed Changes

MPD Change Summary

- Fix state machine diagrams
  - Edits on state machine parts A, B, and C
  - Figures 169-6, 169-7, 169-8
- Add a timer for inrush
  - Modify subclause 169.5.3.4
  - Modify table 169-8
- Add a function for inrush
  - Modify subclause 169.5.3.5
- Open-up Mark Event voltage limit
  - Modify table 169-7

- Add “THEN” to all IF statements
- Set present_discovery_sig <= TRUE on DO_MARK1
- Set present_discovery_sig <= FALSE at PON_EVAL or IDLE

MPD Discover State Machine Changes

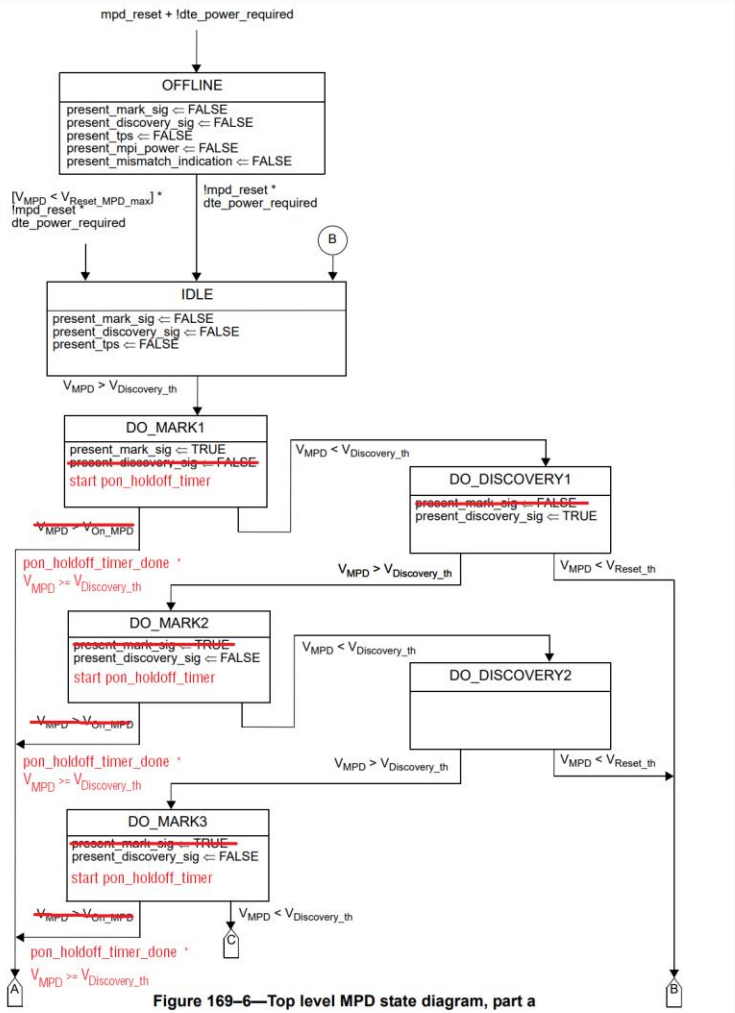

Figure 169–6—Top level MPD state diagram, part a

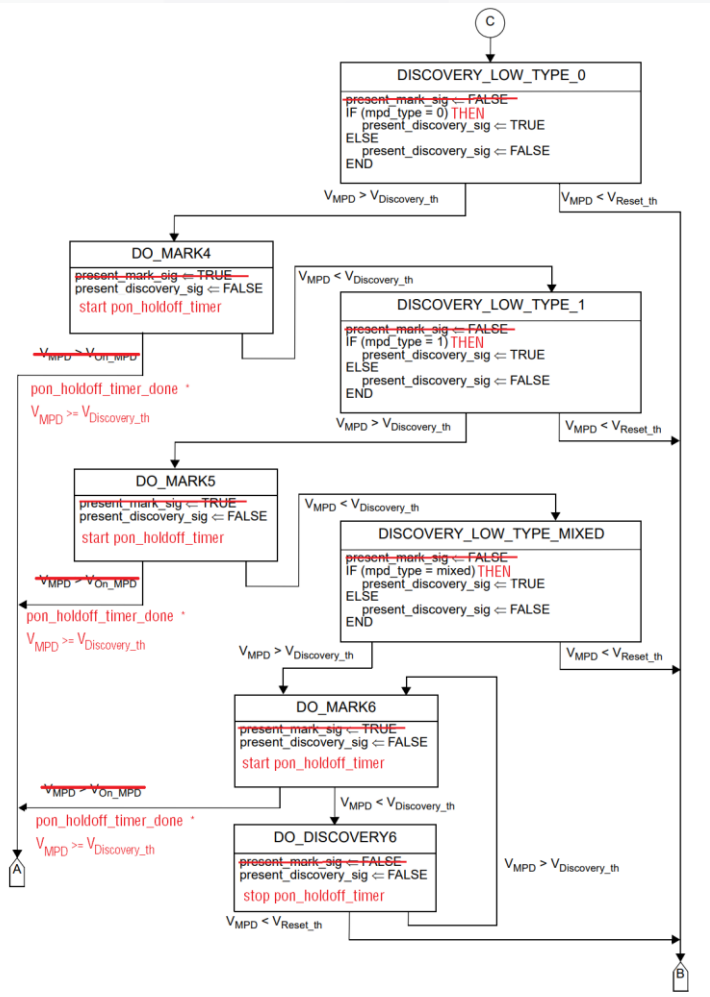

Figure 169–7—Top level MPD state diagram continued, part b

Updated PON State Machine

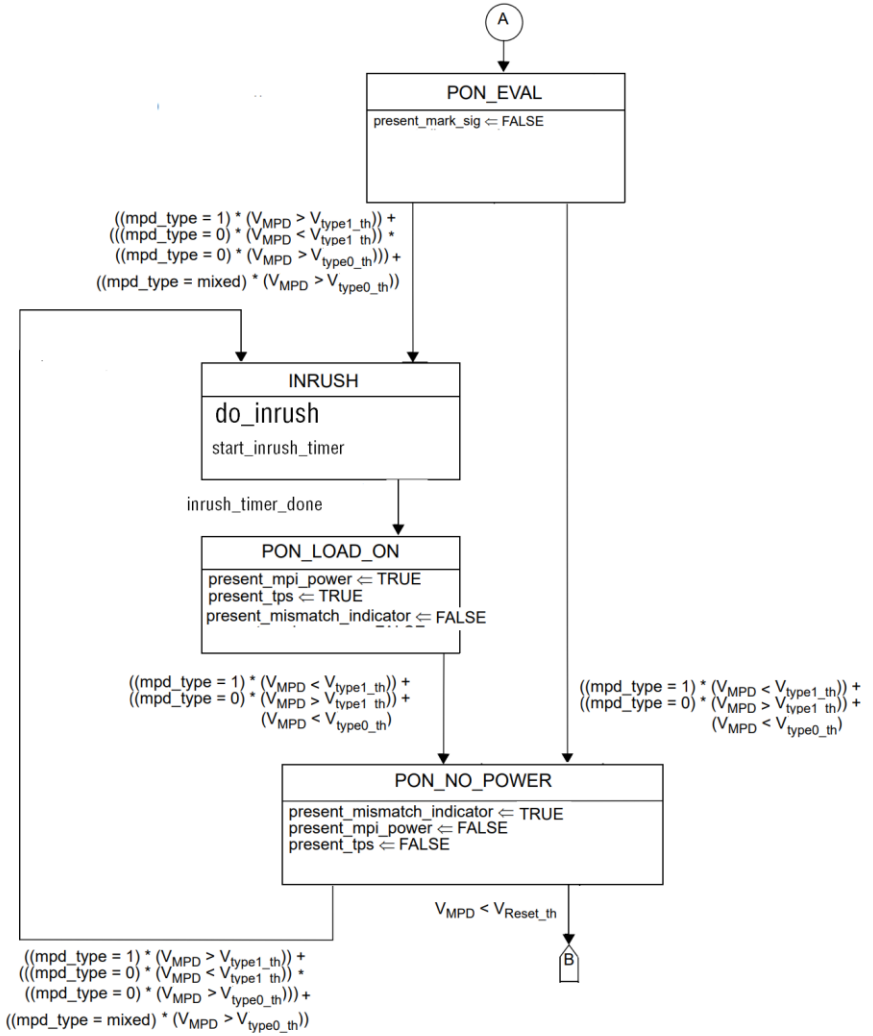

Figure 169–8—Top level MPD state diagram continued, part c

- PON_EVAL simplifies arc logic out of the discovery state machine
  - Set ‘present_mark_sig’ <= FALSE
- INRUSH only precedes PON_LOAD_ON
- PON_NO_POWER handles all conditions where MPD type and MPD voltage are mismatched

Timer Section

169.5.3.4 Timers

All timers operate in the manner described in 14.2.3.2 with the following addition: a timer is reset and stops counting upon entering a state where "stop_x_timer" is asserted.

pon_holdoff_timer

A timer used to hold off the inrush of an MPD after V_{MPD} crosses the V_{type0_th} threshold; see $T_{Inrush\_backoff}$ in Table 169–8 for duration.

pon_holdoff

inrush_timer

A timer used to prevent full load power draw while the MPD is in the inrush state. See T_{Inrush_backoff} in Table 169-8 for duration.

- Insert item in Table 169-8 for the pon_holdoff_timer

Item	Parameter	Symbol	Min	Max	Units	Additional Information
N	Power On Holdoff time	T_{pon_holdoff}	50	75	ms	

ADD to MPD Functions Section

169.5.3.5 Functions

do_inrush

This function transitions the MPD load from off to on (drawing power). During the INRUSH state the MPD charges bulk capacitors with a controlled current, I_{Inrush_MPD}. See Table 169-8.

Discovery Parameter Changes

- Change Mark event voltage Max to emdash '–'

Table 169–7—MPD discovery parameters

Item	Parameter	Symbol	Min	Max	Units	Additional Information
1	Mark event voltage	V_{MPD_mark}	16	~~19.1~~ '–'	V	