

# MPD State Machine Edits

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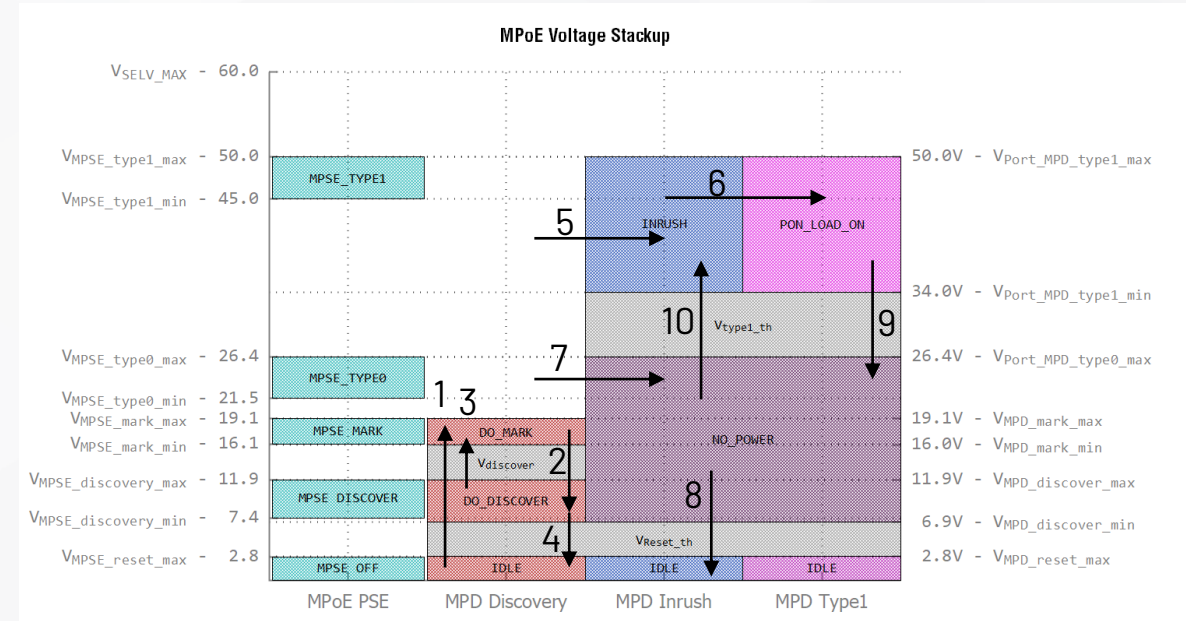
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- ▶ George Zimmerman and I tried to incorporate all comments on the MPD state machine into a single document and fix any other issues that arose as we integrated everybody's work
- ▶ See the attached document 8023-169t4.pdf for proposed text

# State Machine Analysis (reference)

# Type 1 MPD States

ARC	last state	next state	condition	note
1	IDLE	DO_MARK1	$V_{\{MPD\}} > V_{\{Discovery\_th\}}$	start mark timer needs to be added to state machine
2	DO_MARKx	DO_DISCOVERYx	$V_{\{MPD\}} < V_{\{Discovery\_th\}}$	
3	DO_DISCOVERYx	DO_MARK(x+1)	$V_{\{MPD\}} > V_{\{Discovery\_th\}}$	start mark timer needs to be added to state machine
4	DO_DISCOVERYx	OFFLINE		discovery2 arcs go to IDLE instead of OFFLINE in current state machine? What is the difference between offline and idle
5	MPD_MARKx	INRUSH	$mark\_timer\_done * V_{\{MPD\}} > V_{\{type1\_th\}}$	fix this in state machine, need to go to PON_EVAL 1st, then PON_INRUSH if we are arcing to POWER_ON
6	INRUSH	PON_LOAD_ON	INRUSH COMPLETE - Define Condition	
7	MPD_MARKx	PON_NO_POWER	$mark\_timer\_done * V_{\{MPD\}} < V_{\{type1\_th\}}$	Move through "PON_EVAL" 1st.
8	PON_NO_POWER	IDLE	$V_{\{MPD\}} < V_{\{Reset\_th\}}$	
9	PON_LOAD_ON	PON_NO_POWER	$V_{\{MPD\}} < V_{\{type1\_th\}}$	Consider timing and what happens at PI vs. behind recitifer and bulk caps. PI voltage and internal voltage can get out of sync
10	PON_NO_POWER	PON_LOAD_ON	$V_{\{MPD\}} > V_{\{type1\_th\}}$	Any timing or hysteresis requirements to stop a 10-6-9 loop?



# Type 0 MPD States

ARC	last state	next state	condition	note
1	IDLE	DO_MARK1	$V_{\{MPD\}} > V_{\{Discovery\_th\}}$	start mark timer needs to be added to state machine
2	DO_MARKx	DO_DISCOVERYx	$V_{\{MPD\}} < V_{\{Discovery\_th\}}$	
3	DO_DISCOVERYx	DO_MARK(x+1)	$V_{\{MPD\}} > V_{\{Discovery\_th\}}$	start mark timer needs to be added to state machine
4	DO_DISCOVERYx	IDLE		Discovery arcs go to IDLE instead of OFFLINE in current state machine? What is the difference between offline and idle
5	MPD_MARKx	INRUSH	mark_timer_done * $V_{\{MPD\}} > V_{\{type0\_th\}}$ * $V_{\{MPD\}} < V_{\{type1\_th\}}$	fix this in state machine, need to go to PON_EVAL 1st, then PON_INRUSH if we are arcing to POWER_ON
6	INRUSH	PON_LOAD_ON	INRUSH COMPLETE - Define Condition	
7	MPD_MARKx	PON_NO_POWER	mark_timer_done * $V_{\{MPD\}} < V_{\{type0\_th\}}$ + $V_{\{MPD\}} > V_{\{type1\_th\}}$	Move through "PON_EVAL" 1st
8	PON_NO_POWER	IDLE	$V_{\{MPD\}} < V_{\{Reset\_th\}}$	
9	PON_LOAD_ON	PON_NO_POWER	$V_{\{MPD\}} < V_{\{type0\_th\}}$ + $V_{\{MPD\}} > V_{\{type1\_th\}}$	Consider timing and what happens at PI vs. behind rectifier and bulk caps. PI voltage and internal voltage can get out of sync
10	PON_NO_POWER	PON_LOAD_ON	$V_{\{MPD\}} > V_{\{type0\_th\}}$ * $V_{\{MPD\}} < V_{\{type0\_th\}}$	Any timing or hysteresis requirements to stop a 10-6-9 loop?

