Clarifications related to Clause 119 PCS restart_lock

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Previous Work

- P802d3bs_D3p2_comments_final_Cl.pdf, changed (through comment resolution of Comment #r02-6) the Figure 119-12 – Alignment marker lock state diagram
  - But not the body of subclause text

Overview

- **Published 802.3-2018 and current P802.3/D2.0 draft lack consistency between state diagram and body of subclause**
  - The inconsistency was introduced when a state diagram change was made during the P802.3bs draft development
- **This presentation proposes to modify the body of subclause to return consistency to the standard**

P802.3/D2.0 (IEEE 802.3dc)
22nd July 2021

P802.3/D2.0 (IEEE 802.3dc) – State Diagrams Prevail

- **119.2.6.3 State diagrams**
  - Current P802.3/D2.0 draft contains same text as published in 802.3-2018 standard
- **State diagrams take precedence over body of subclause as stated in 119.2.6.1**

The PCS receive decodes blocks as specified in the receive state diagram shown in Figure 119–15.

119.2.6 Detailed functions and state diagrams

119.2.6.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, functions, and counters. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

P802.3/D2.0 119.2.6.3 State diagrams – Current Text

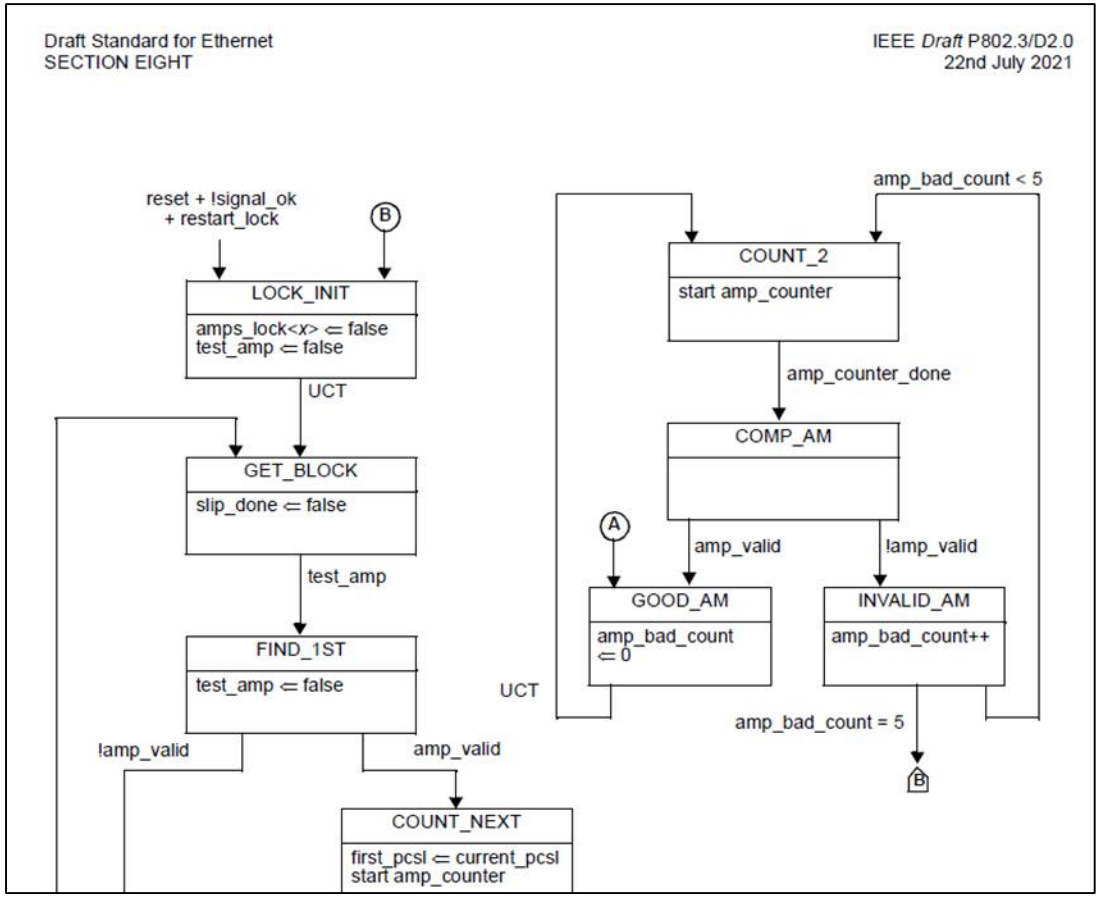
- **Text description (highlighted) of 119.2.6.3 states that restart_lock is signaled in either of following conditions:**
  - When the PCS synchronization process determines that three uncorrectable codewords in a row are seen
  - When the alignment marker lock process sees five alignment markers in a row that fail to match the expected pattern on a given lane
- **Based on state diagrams (next slide) only one of these conditions still impacts restart_lock**
  - The other condition is historical text that pre-dates the state diagram change that appeared in P802.3bs/D3.3 Figure 119-12 – Alignment marker lock state diagram

119.2.6.3 State diagrams

The 200GBASE-R PCS shall implement eight alignment marker lock processes and the 400GBASE-R PCS shall implement sixteen alignment marker lock processes as depicted in Figure 119-12. An alignment marker lock process operates independently on each lane. The alignment marker lock state diagram shown in Figure 119-12 determines when the PCS has obtained alignment marker lock to the received bit stream for a given lane of the service interface. Each alignment marker lock process looks for two valid alignment markers 278 528 × 10-bit Reed-Solomon symbols apart, on a per PCS lane basis, to gain alignment marker lock. When the alignment marker lock process achieves lock for a lane, and if a Clause 45 MDIO is implemented, the PCS shall record the PCS lane number received on that lane of the service interface in the appropriate lane mapping register (3.400 to 3.415). Once in lock, a lane goes out of alignment marker lock only when restart_lock is signaled. This occurs when the PCS synchronization process determines that three uncorrectable codewords in a row are seen, or when the alignment marker lock process sees five alignment markers in a row that fail to match the expected pattern on a given lane.

P802.3/D2.0 – Figure 119-12

- **From INVALID_AM state, if FSM sees amp_bad_count=5, it directly transitions to LOCK_INIT state**
  - Note that it does not modify restart_lock



Source: P802.3/D2.0 Figure 119-12 – Alignment marker lock state diagram

P802.3/D2.0 119.2.6.3 State diagrams – Proposed Text

- **Propose to modify portion of the text**
  - Encapsulate within parenthesis (see highlighted text) the single condition that affects restart_lock

119.2.6.3 State diagrams

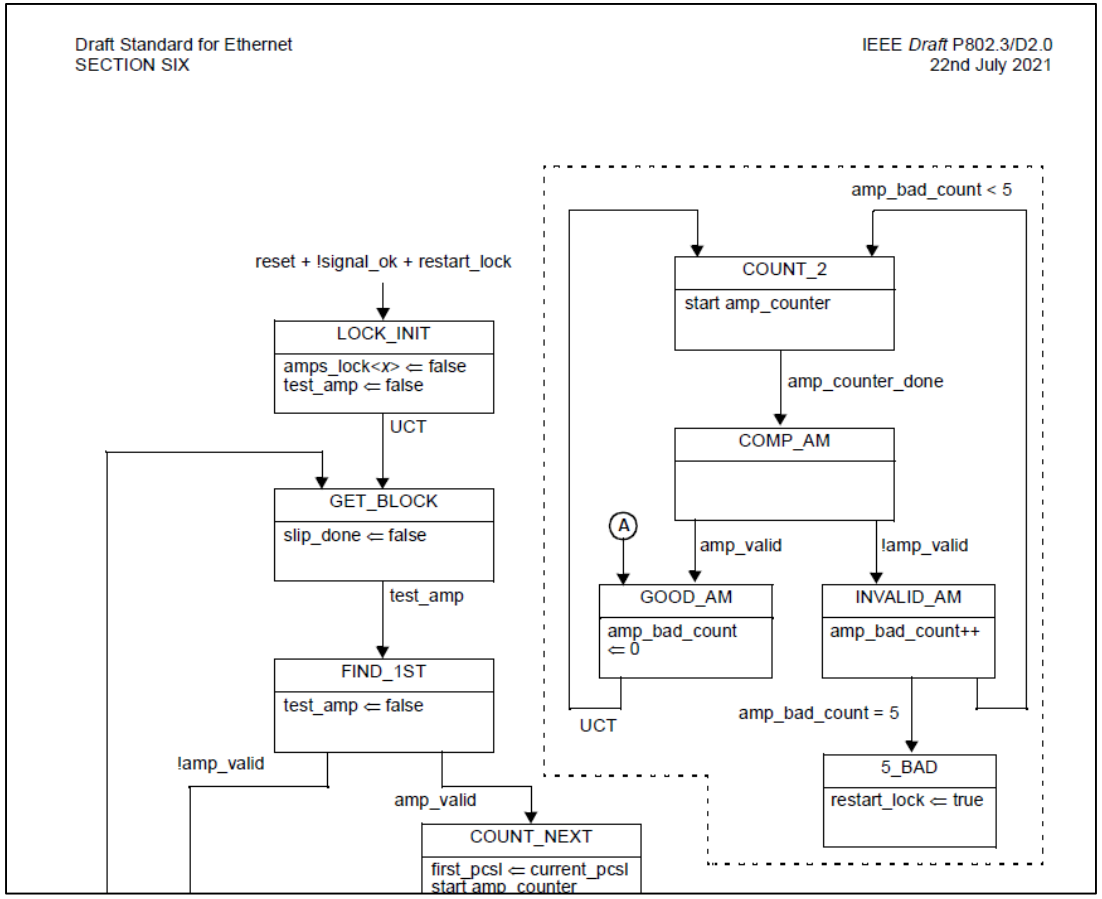
The 200GBASE-R PCS shall implement eight alignment marker lock processes and the 400GBASE-R PCS shall implement sixteen alignment marker lock processes as depicted in Figure 119-12. An alignment marker lock process operates independently on each lane. The alignment marker lock state diagram shown in Figure 119-12 determines when the PCS has obtained alignment marker lock to the received bit stream for a given lane of the service interface. Each alignment marker lock process looks for two valid alignment markers 278 528 × 10-bit Reed-Solomon symbols apart, on a per PCS lane basis, to gain alignment marker lock. When the alignment marker lock process achieves lock for a lane, and if a Clause 45 MDIO is implemented, the PCS shall record the PCS lane number received on that lane of the service interface in the appropriate lane mapping register (3.400 to 3.415). Once in lock, a lane goes out of alignment marker lock when restart_lock is signaled (this occurs when the PCS synchronization process determines that three uncorrectable codewords in a row are seen) or when the alignment marker lock process sees five alignment markers in a row that fail to match the expected pattern on a given lane.

Thank You!

Backups

P802.3/D2.0 (IEEE 802.3dc) – Figure 91-8

- **Contrast Clause 119 restart_lock with Clause 91 restart_lock**
- **In Clause 91, from the optional INVALID_AM state, if FSM sees amp_bad_count=5, it transitions to 5_BAD state**
  - This sets restart_lock to true

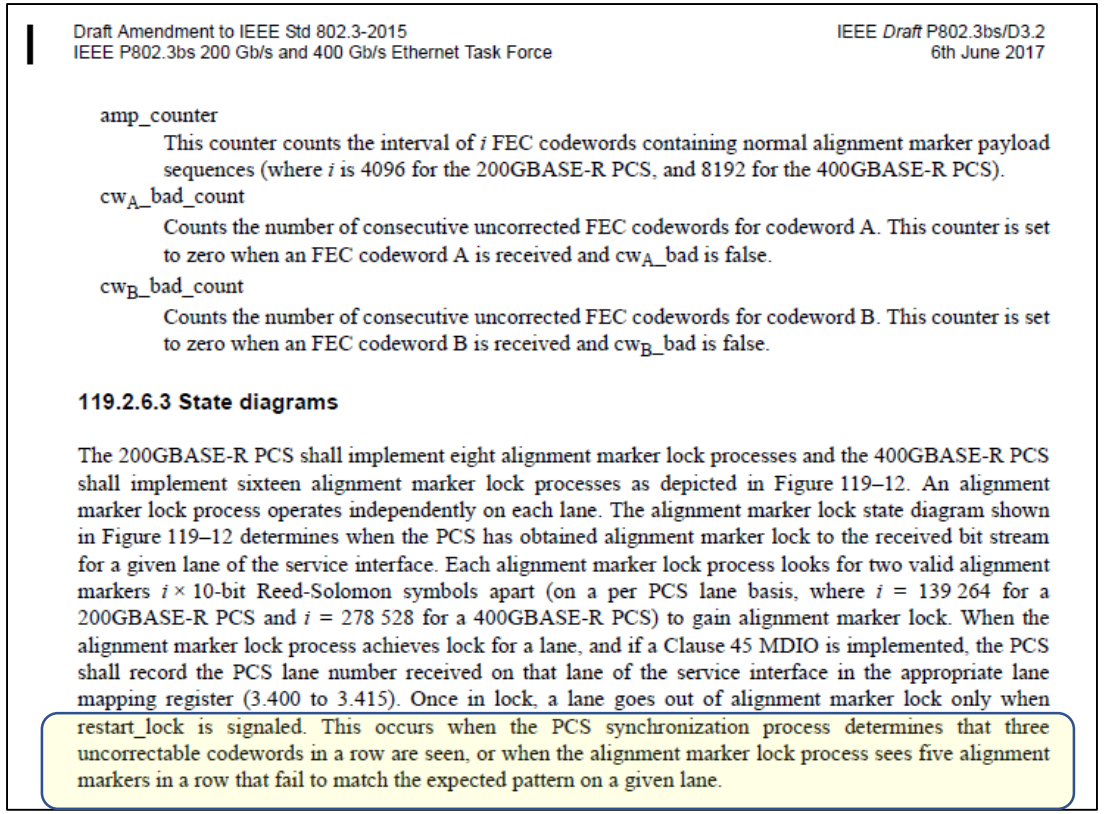


Source: P802.3/D2.0 Figure 91-8 – FEC synchronization state diagram

P802.3bs/D3.2
6th June 2017

P802.3bs/D3.2 119.2.6.3 State diagrams

- **Text description of 119.2.6.3 states that restart_lock is signal in either of following cases:**
  - When the PCS synchronization process determines that three uncorrectable codewords in a row are seen
  - When the alignment marker lock process sees five alignment markers in a row that fail to match the expected pattern on a given lane



amp_counter

This counter counts the interval of *i* FEC codewords containing normal alignment marker payload sequences (where *i* is 4096 for the 200GBASE-R PCS, and 8192 for the 400GBASE-R PCS).

cw_A_bad_count

Counts the number of consecutive uncorrected FEC codewords for codeword A. This counter is set to zero when an FEC codeword A is received and cw_A_bad is false.

cw_B_bad_count

Counts the number of consecutive uncorrected FEC codewords for codeword B. This counter is set to zero when an FEC codeword B is received and cw_B_bad is false.

119.2.6.3 State diagrams

The 200GBASE-R PCS shall implement eight alignment marker lock processes and the 400GBASE-R PCS shall implement sixteen alignment marker lock processes as depicted in Figure 119–12. An alignment marker lock process operates independently on each lane. The alignment marker lock state diagram shown in Figure 119–12 determines when the PCS has obtained alignment marker lock to the received bit stream for a given lane of the service interface. Each alignment marker lock process looks for two valid alignment markers $i \times$ 10-bit Reed-Solomon symbols apart (on a per PCS lane basis, where i = 139 264 for a 200GBASE-R PCS and i = 278 528 for a 400GBASE-R PCS) to gain alignment marker lock. When the alignment marker lock process achieves lock for a lane, and if a Clause 45 MDIO is implemented, the PCS shall record the PCS lane number received on that lane of the service interface in the appropriate lane mapping register (3.400 to 3.415). Once in lock, a lane goes out of alignment marker lock only when restart_lock is signaled. This occurs when the PCS synchronization process determines that three uncorrectable codewords in a row are seen, or when the alignment marker lock process sees five alignment markers in a row that fail to match the expected pattern on a given lane.

Source: P802.3bs/D3.2 119.2.6.3 State diagrams

P802.3bs/D3.2 119.2.6.2.2 Variables

- **Text description of 119.2.6.2.2 describes restart_lock signal**
  - It mentions two conditions that set it to true

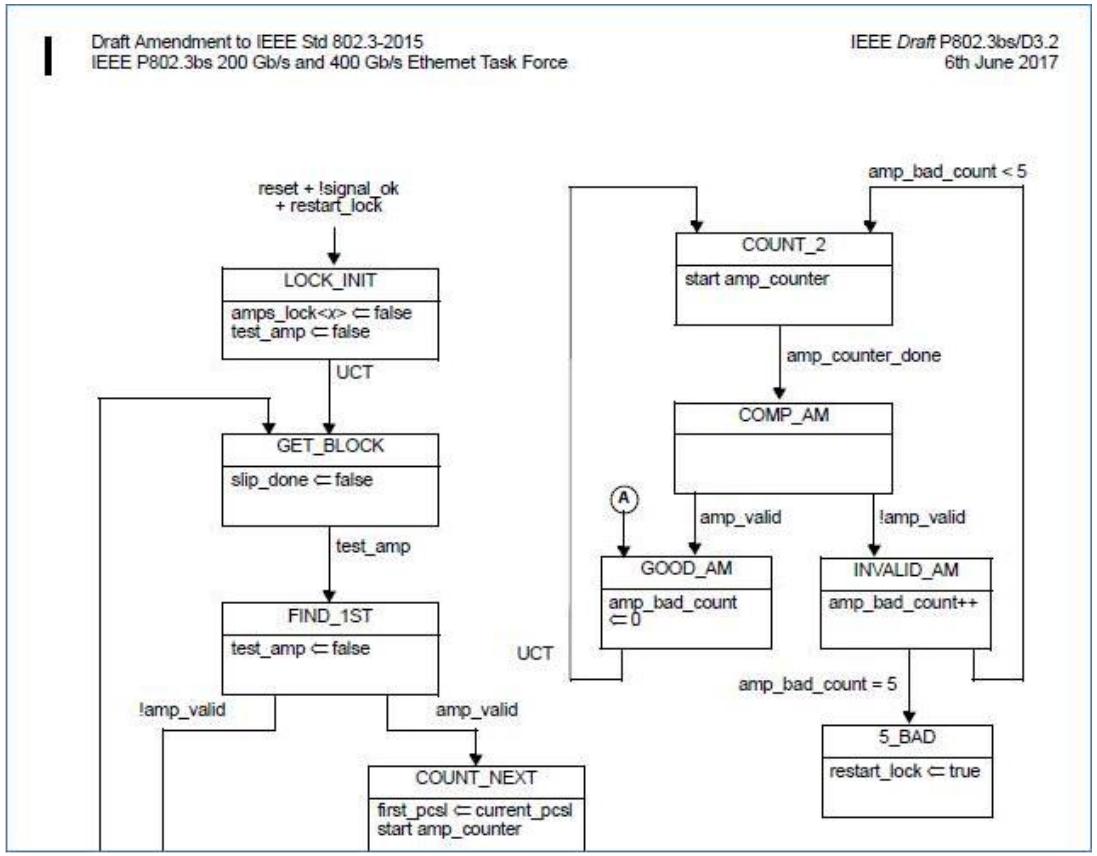
restart_lock

Boolean variable that is set by the PCS synchronization process to restart the alignment marker lock process on all PCS lanes. It is set to true after 3 consecutive uncorrected codewords are received (3_BAD state) or when 5 Alignment Markers in a row fail to match (5_BAD state) and set to false upon entry into the LOSS_OF_ALIGNMENT state.

Source: P802.3bs/D3.2 119.2.6.2.2 Variables

P802.3bs/D3.2 – AM lock state diagram

- **From INVALID_AM state, if FSM sees amp_bad_count=5, it transitions to 5_BAD state**
  - Sets restart_lock to true



Source: P802.3bs/D3.2 Figure 119-12 – Alignment marker lock state diagram

Comments on P802.3bs/D3.2

Comment #r02-6

Comment Type: T Comment Status: A

Adding hi_ser in the Fig. 119-13 seems unintended. It forces the LOSS_OF_ALIGNMENT state (LOA) which creates ambiguities for the RSFEC decode process up to the possibility of a dead-lock the link would never recover from. Reasons of doubt: a) When in LOA state restart_lock is forced false. If now during hi_ber the link is reset by the link partner the statemachine of Fig. 119-12 will enter the 5_BAD state eventually as markers are most likely no longer at expected position. Now we have an ambiguity what state the restart_lock variable should become. Fig. 119-13 enforces false, where now Fig. 119-12 enforces true. Which one wins ? (neither is a solution) b) But the main problem is now Fig. 119-13 which does not allow deskew as LOA state enforces pcs_enable_deskew=false. Hence the deskew process cannot align the lanes in such situation causing the RSFEC decoder receiving data from unaligned lanes causing permanent uncorrectable codewords which by definition in 119.2.5.3 create 16 symbol errors per codeword. This is now a dead-lock, as the hi_ser will never deassert as the threshold will be permanently exceeded hence the link will never come up again. It may be argued that the RSFEC decode process is not active when align_status is down but then also hi_ser measurement stops which then means definition of hi_ser deassertion is incorrect in 119.2.6.2. and e.g. needs to be defined purely based on time deasserting after 60..75ms.

SuggestedRemedy

I think the intention was to enforce CDMII local fault signaling and link status down when hi_ser occurs similar to the reaction to hi_ber done for 100G (Clause 82) while maintaining all RSFEC decode process to continue operating normally while hi_ser is asserted to keep monitoring. Proposed Remedy: remove the the or hi_ser from Fig. 119-13. Instead add it to Fig. 119-15 (Receive state diagram) to enforce RX_INIT state producing local fault to CDMII. In addition change definition of PCS_Status in 119.2.6.2.2 to: A boolean variable that is true when align_status is true and hi_ser is false and is false otherwise.

Response Response Status: C

ACCEPT IN PRINCIPLE.

Adding hi_ser to the state machine in Figure 119-13 was intentional. This only occurs once a high symbol error ratio is observed and FEC_bypass_indication_enable is set to one.

Modify state diagram in Figure 119-12 to remove the restart_lock conflict by removing the 5_BAD state, and have a direct transition from INVALID_AM directly to LOCK_INIT if amp_bad_count = 5.

P802.3bs/D3.3
28th July 2017

P802.3bs/D3.3 119.2.6.3 State diagrams

- **Text description of 119.2.6.3 remains unchanged**
  - It still mentions two conditions that set it to true

amp_counter

This counter counts the interval of *i* FEC codewords containing normal alignment marker payload sequences (where *i* is 4096 for the 200GBASE-R PCS, and 8192 for the 400GBASE-R PCS).

cw_A_bad_count

Counts the number of consecutive uncorrected FEC codewords for codeword A. This counter is set to zero when an FEC codeword A is received and cw_A_bad is false.

cw_B_bad_count

Counts the number of consecutive uncorrected FEC codewords for codeword B. This counter is set to zero when an FEC codeword B is received and cw_B_bad is false.

119.2.6.3 State diagrams

The 200GBASE-R PCS shall implement eight alignment marker lock processes and the 400GBASE-R PCS shall implement sixteen alignment marker lock processes as depicted in Figure 119–12. An alignment marker lock process operates independently on each lane. The alignment marker lock state diagram shown in Figure 119–12 determines when the PCS has obtained alignment marker lock to the received bit stream for a given lane of the service interface. Each alignment marker lock process looks for two valid alignment markers 278 528 × 10-bit Reed-Solomon symbols apart, on a per PCS lane basis, to gain alignment marker lock. When the alignment marker lock process achieves lock for a lane, and if a Clause 45 MDIO is implemented, the PCS shall record the PCS lane number received on that lane of the service interface in the appropriate lane mapping register (3.400 to 3.415). Once in lock, a lane goes out of alignment marker lock only when restart_lock is signaled. This occurs when the PCS synchronization process determines that three uncorrectable codewords in a row are seen, or when the alignment marker lock process sees five alignment markers in a row that fail to match the expected pattern on a given lane.

Source: P802.3bs/D3.3 119.2.6.3 State diagrams

P802.3bs/D3.3 119.2.6.2.2 Variables

- **Text description of 119.2.6.2.2 remains unchanged**
  - It still mentions two conditions that set it to true

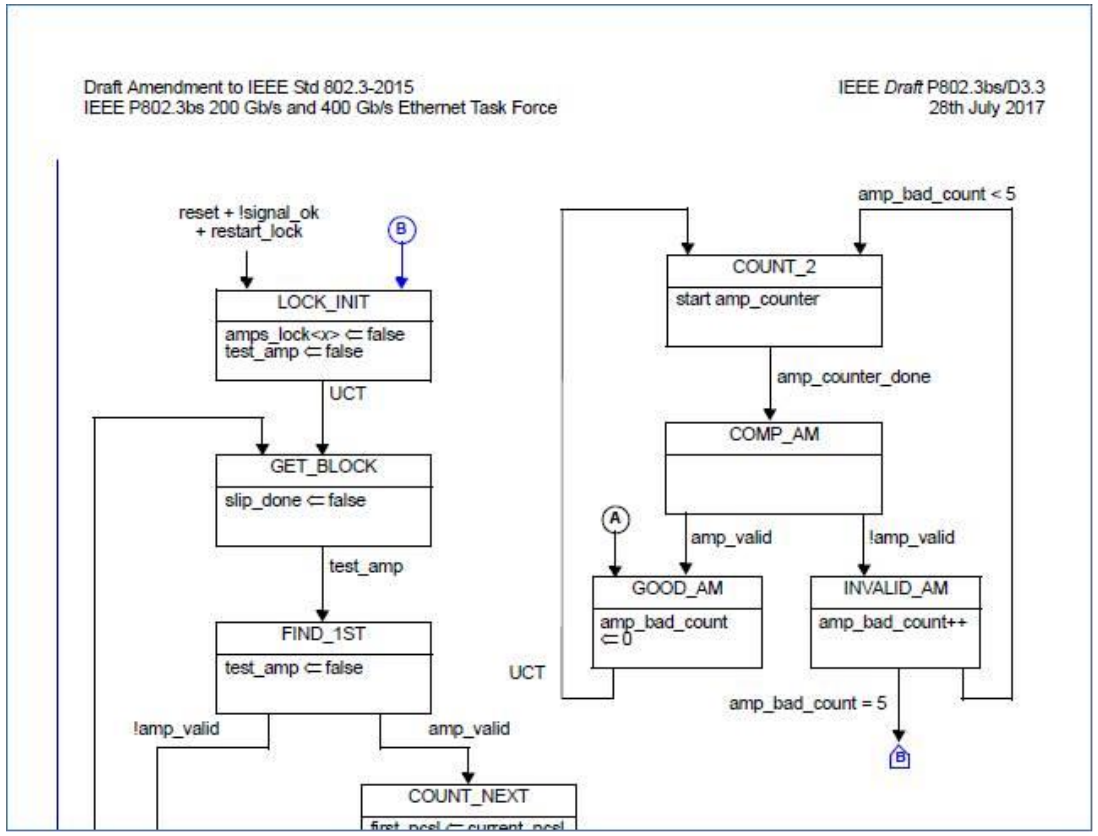
restart_lock

Boolean variable that is set by the PCS synchronization process to restart the alignment marker lock process on all PCS lanes. It is set to true after 3 consecutive uncorrected codewords are received (3_BAD state) or when 5 Alignment Markers in a row fail to match (5_BAD state) and set to false upon entry into the LOSS_OF_ALIGNMENT state.

Source: P802.3bs/D3.3 119.2.6.2.2 Variables

P802.3bs/D3.3 – AM lock state diagram

- **State machine was changed from the previous draft**
- **From INVALID_AM state, if FSM sees amp_bad_count=5, it directly transitions to LOCK_INIT state**
  - It no longer modifies restart_lock



Source: P802.3bs/D3.3 Figure 119-12 – Alignment marker lock state diagram

802.3bs-2018

802.3bs-2018 119.2.6.2.2 Variables

- **At some point after P802.3bs/D3.5 the text description of 119.2.6.2.2 was changed**
  - The restart_lock description matches the state diagram
  - It only mentions one condition that sets it to true

restart_lock

Boolean variable that is set by the PCS synchronization process to restart the alignment marker lock process on all PCS lanes. It is set to true after 3 consecutive uncorrected codewords are received (3_BAD state) and set to false upon entry into the LOSS_OF_ALIGNMENT state.

Source: 802.3bs-2018 119.2.6.2.2 Variables