DSP and FEC considerations for 800GbE and 1.6TbE

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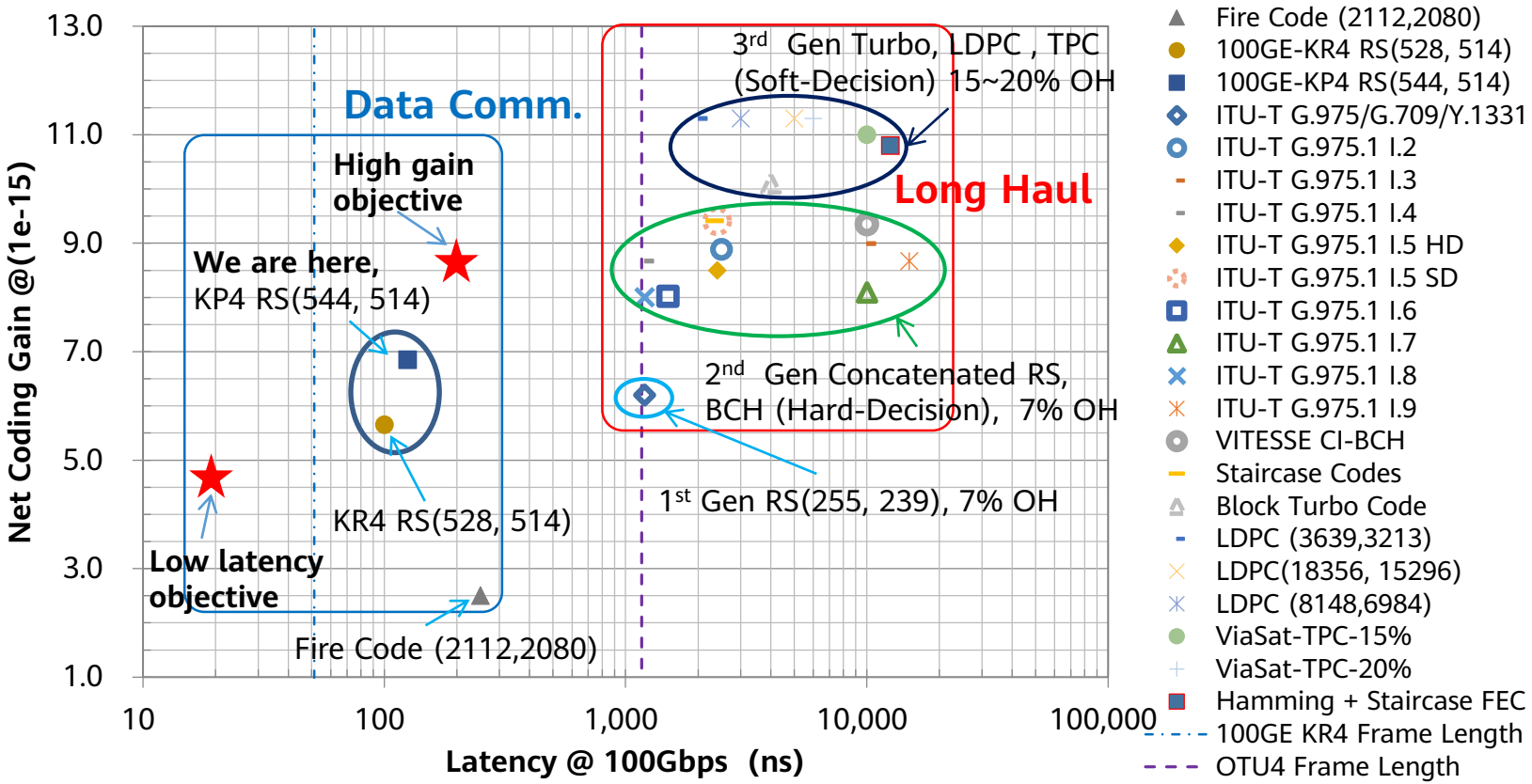
Presumptions of the Discussion

- **“Leverage existing error correction architecture (End-to-end, hard decision, RS FEC) for 200G electrical and optical links.” should always be the priority choice.**
  - Well understood by the industry, no unknown systematic issues.
  - “Improve channel” and “Use advanced DSP” are far more efficient than going for a “Stronger FEC”. FEC technologies are much less efficient when go beyond RS(544, 514).
  - RS(576, 514) with MLSE probably gives the best performance among the 12% FEC codes.
  - No solid evidence shows that existing error correction architecture cannot be leveraged.

- If a more powerful FEC is needed to address the performance concern, we should consider:
  - Appropriate objectives from requirement, technology and historical perspective.
  - Mutually exclusive relationship of FEC with advanced digital signal processing (DSP) technologies.
  - Scenarios and architecture considerations, end-to-end, segmented or concatenated.

- Only 200G electrical and intensity modulation with direct detection (IM-DD) optical systems with pulse amplitude modulation (PAM) modulations are considered, and coherent optics are outside the scope of this discussion.

Net coding gain and latency objectives



Long Haul Scenarios	Year
RS(255, 239) Gen 1, G.709/G.975	2000
Gen 2, G.975.1	2004
Gen 3, SD-LDPC	2007~2010
Staircase Code G.709.2	2012~2018
Data Comm. Scenarios	**Year**
10GE KR Fire Code	2006
100GE KR4, KP4	2012~2017
IEEE 400GE ZR/OIF-400ZR	2019~2020
Higher Gain FEC?	?
Low Latency?	?

- **High gain**: NCG = 8.0~9.0dB (BERin ~= 1e-3), latency~=120ns@100Gbps.
- Ultra-low latency: latency <20ns@100Gbps, NCG ~= 3.0~5.0dB, (BERin~=1e-8).

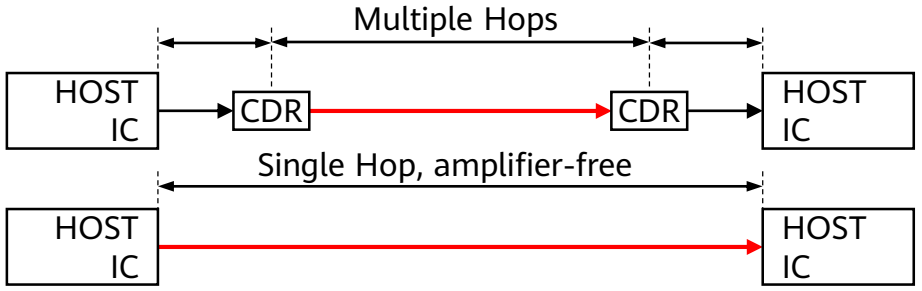
Observations for FEC development:

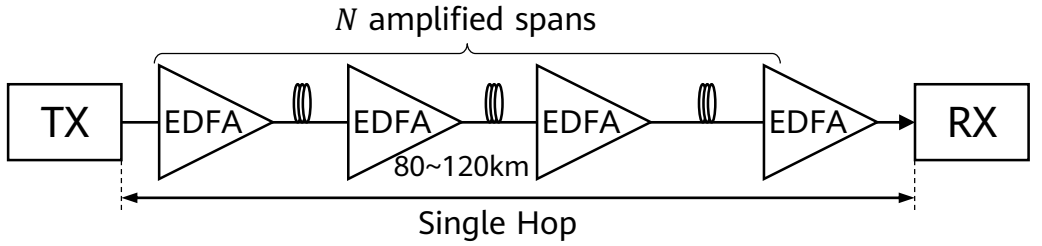
1. It took a long time for a adoption of new interoperable HD-FEC, i.e. from G.709 to G.709.2. More controversial for SD-FEC.
2. Too many options means no option, e.g. G.975.1, IEEE400G-ZR, OIF 400-ZR?.
3. There was no successful interoperable industrial practice of SD-FEC in electrical and IM-DD optical systems.

Ref: Y. Lu, L. Ma, D. Mo and L. Liang, "High Gain Low Complexity Low Latency FEC Codes for Ethernet and Backplane Applications", DesignCon 2018, Santa Clara, CA, 2018.

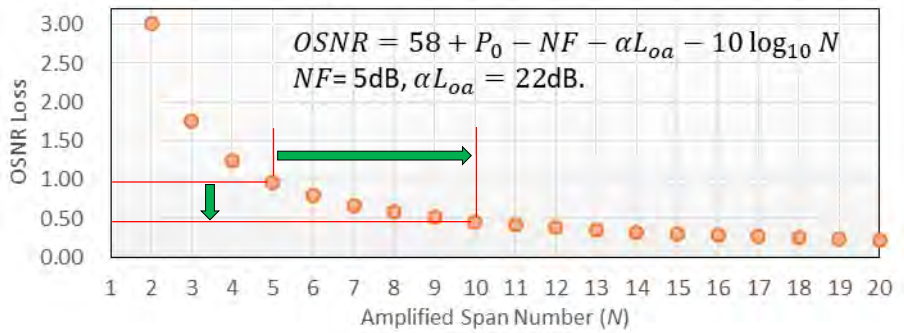
Considerations behind the FEC choices

	IM-DD: Segmented link. (Complexity & Latency)	Coherent: Amplified link. (Performance / NCG)
Net coding gain (NCG)	**8.0~9.0dB** (BERin ~= 1e-3),	>=10.8dB (BERin ~= 1e-2), < Shannon limit.
	Limited by complexity, latency and cost. Constrained in terms of area and power. Small NCG improvement is not helpful.	Small NCG improvement can provide huge benefit.
	Single span, amplifier-free. The digital signal is regenerated. ISI-dominant.	Multiple amplifier span cascaded. Noise-dominant.
Complexity	**Low**	**High**
Latency	Current: ~100ns@100G; Future: ~120ns@100G.	> 1μs@100G
	40inch backplane: ~5ns; Multi-hops. 100GE FEC latency ~100ns.	100km fiber: ~500ns; single hop. 100G OTU4 frame is ~1.164μs.
	Computing and storage applications require ultra low latency.	Do not care about the interface latency too much.

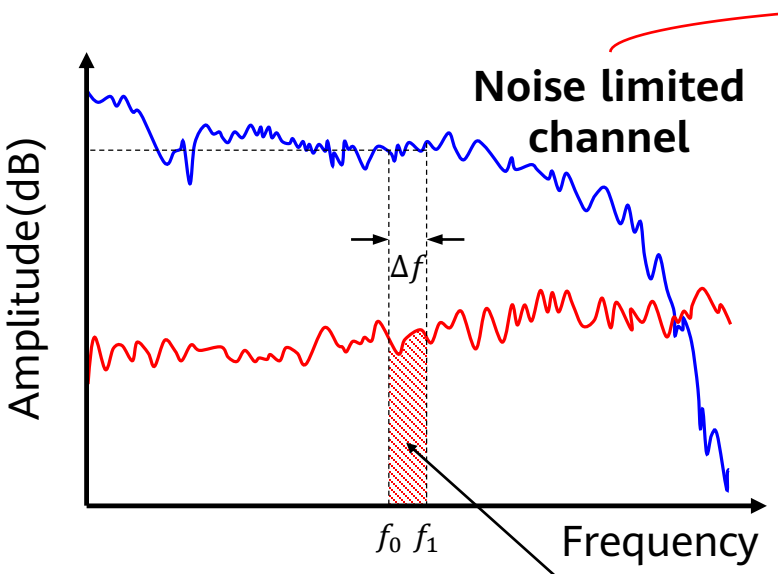




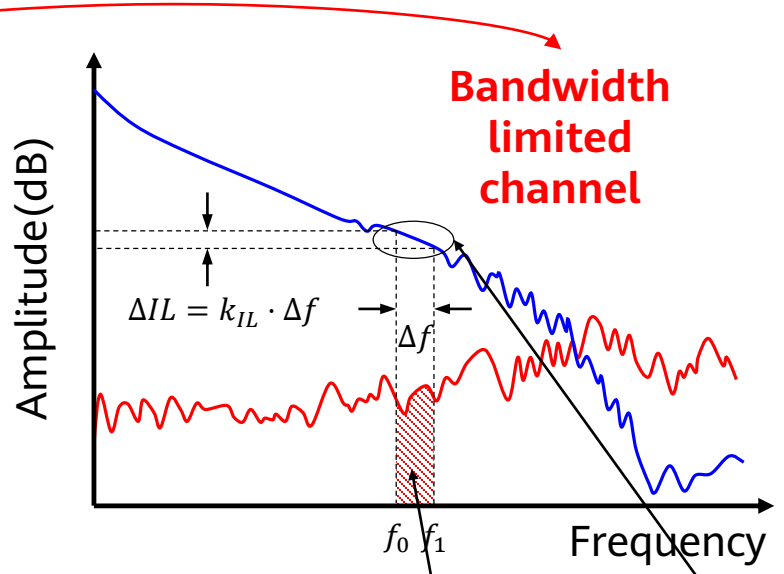
- **Segmented link**: digital signal is regenerated for each segment, the worst segment determines the NCG requirement of FEC. **Small NCG improvement gives little benefit while an end-to-end FEC can cover the worst segment.**
- **Amplified link**: analog signal is amplified for each span, **small NCG improvement gives huge benefit**. E.g. 0.5dB NCG improvement will extent the span number from 5 to 10, if each amplified span is 100km, it means 500km extension of the reach.



Net coding gain is critical for higher overhead FEC!

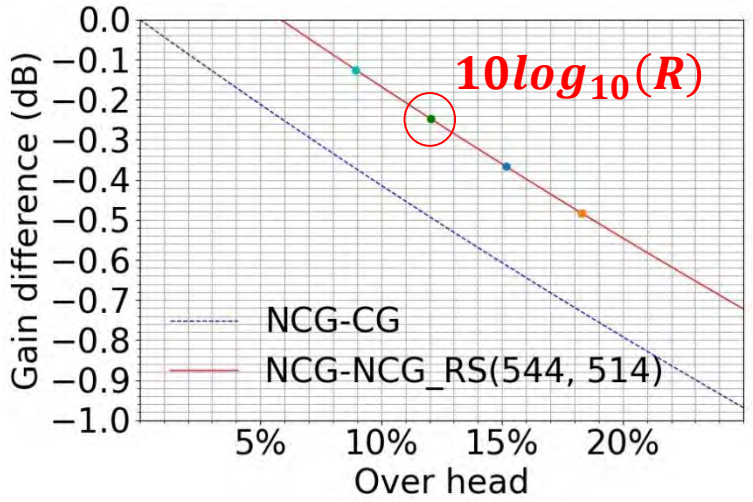


$$NCG = CG + \boxed{10 \cdot \log_{10}(R)}$$



$$NCG = CG + \boxed{10 \cdot \log_{10}(R)} + \boxed{\boldsymbol{\alpha \cdot \Delta IL}}$$

1st order approximation, α can be very complicated

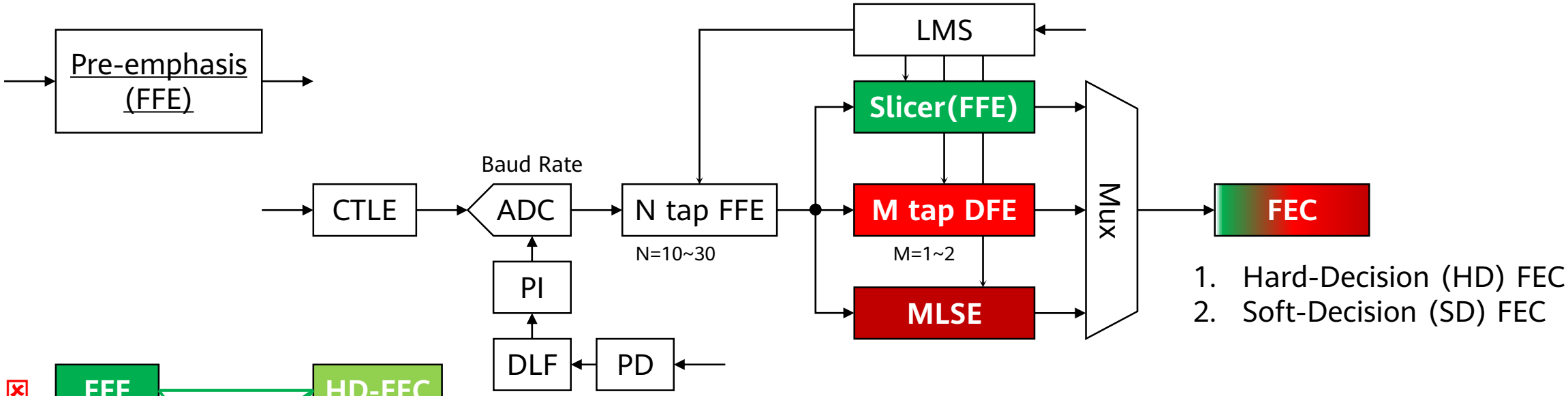


~0.25dB gain loss should be consider to upgrade RS(544, 514) to a 12% FEC.

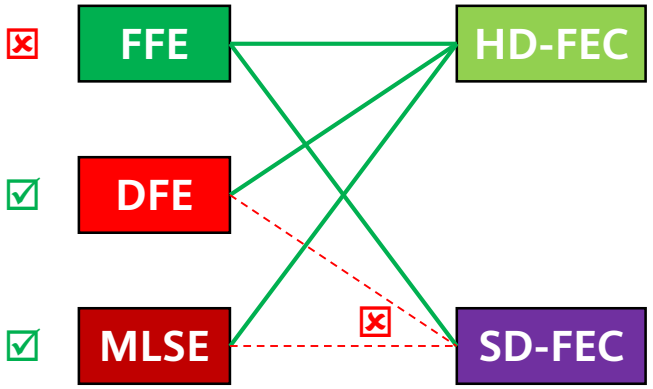
- "$\boldsymbol{10log_{10}(R)}$" is to consider the penalty by data rate increasing.
- "$\boldsymbol{\alpha \cdot \Delta IL \propto k_{IL} \cdot \Delta f}$" should be considered for bandwidth limited channels.
- Both 200G electrical and optical links are likely to be "Bandwidth limited" cases.
- Take caution when adopting a new FEC with a higher overhead!

This term is dominant for bandwidth limited systems!

Cooperation between FEC and DSP



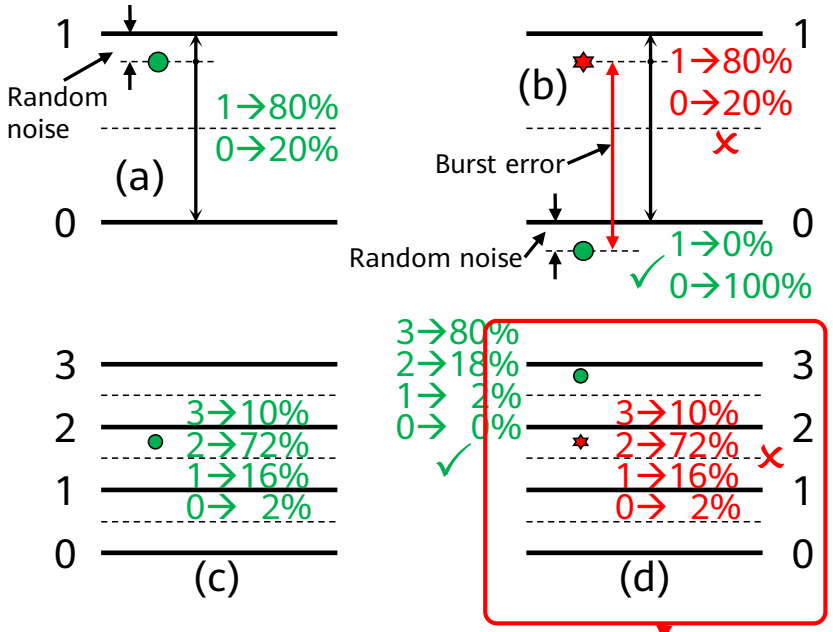
1. Hard-Decision (HD) FEC
2. Soft-Decision (SD) FEC



Exclusive relationships of DSP and FEC

- HD-FEC has the best compatibility with all the DSP algorithms.
- SD-FEC is difficult to be compatible with DFE and MLSE (Nonlinear).
  - For DFE, the propagated error leads to wrong information to the SD-FEC decoder, and is harmful to the decoding process, however DFE has much better performance than FFE.
  - For MLSE, soft-output algorithms such as SOVA, BCJR are required, but the performance is unknown, they are very costly and may be un-affordable in real applications.
- DFE is essential even for 100G not to say 200G.
  - DFE was used as reference receiver in 100G electrical links with DFE coefficient of 0.85.
  - No evidence shows that FFE is sufficient for 200G optics. MLSE is more efficient than SD-FEC. It has no overclocking and > 2dB net coding gain.

Exclusive relationship between SD-FEC and DFE

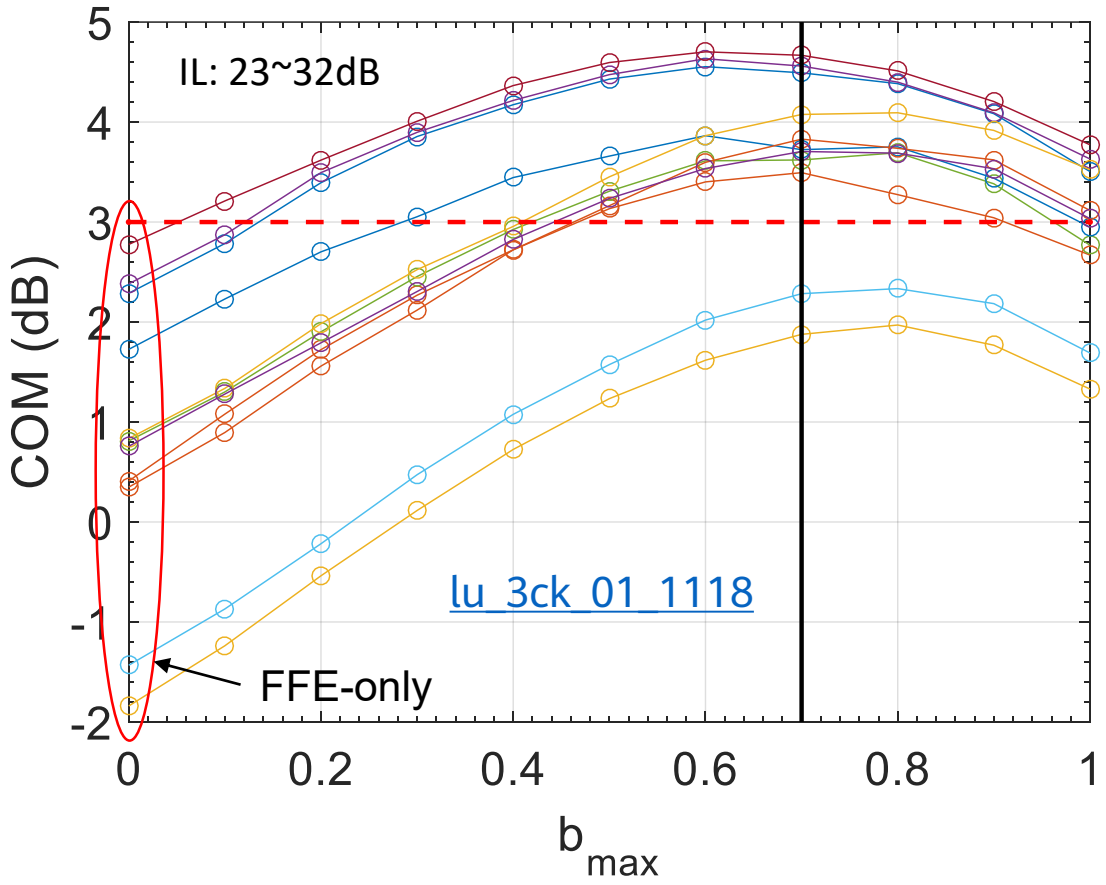


Wrong indication

b_max	0.85												
	1	2	3	4	5	6	7	8	9	10	11	12	
DataIn	1	2	3	0	1	0	3	2	0	1	3	3	1
PrecEncOut	1	1	2	2	3	1	2	0	0	1	2	1	2
Channel	1.00	1.85	2.85	3.7	4.7	3.55	2.85	1.7	0	1	2.85	2.7	3
Noise	-0.07	**0.51**	0.01	0.10	-0.09	-0.03	0.04	-0.03	0.08	-0.09	0.19	0.03	4
Channel+Noise	0.93	2.36	2.86	3.80	4.61	3.52	2.89	1.67	0.08	0.91	3.04	2.73	5
SlicerIn	0.93	1.51	1.16	2.95	2.06	1.82	1.19	0.82	-0.77	0.91	2.19	1.03	6
DFEout	1.00	2	1	3	2	2	1	1	0	1	2	1	7
SlicingError	-0.07	**-0.49**	0.16	-0.05	0.06	-0.18	0.19	-0.18	**-0.77**	-0.09	0.19	0.03	8
DFEoutError	0.00	**+1**	**-1**	**+1**	**-1**	**+1**	**-1**	**+1**	0	0	0	0	9
PrecDecOut	1.00	3	3	0	1	0	3	2	1	1	3	3	13
ErrorPrecDec	0.00	**+1**	0	0	0	0	0	0	**+1**	0	0	0	14

- The propagated errors of DFE will give "wrong information" to the SD-FEC decoder. This may lead to an error spreading in the SD-FEC decoding and crush everything. This is more severe than DFE error propagation.
- The effectiveness of SD-FEC cooperating with nonlinear equalizers such as DFE and MLSE should be explored more deeply. Because DFE and MLSE have much better performance and they have been widely deployed.

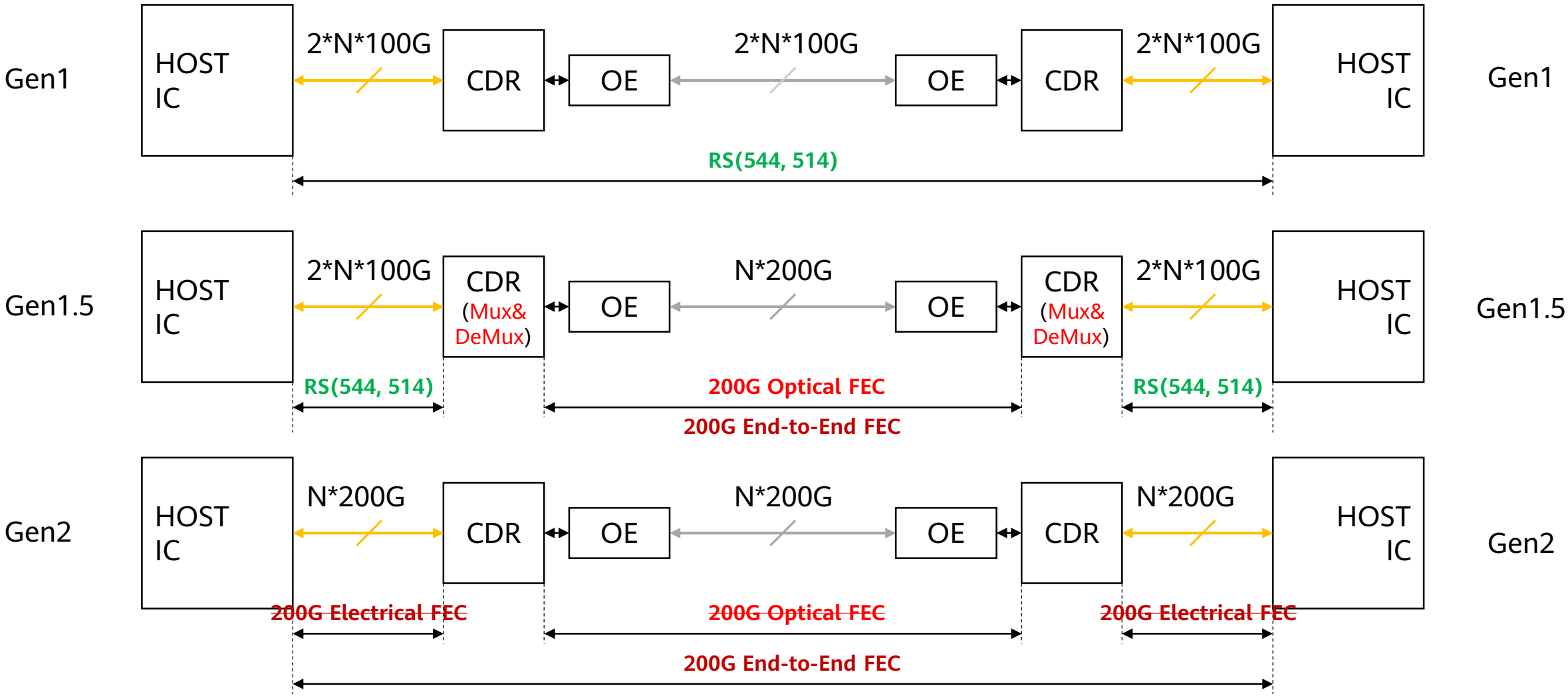
Performance penalty of FFE compared to DFE and MLSE



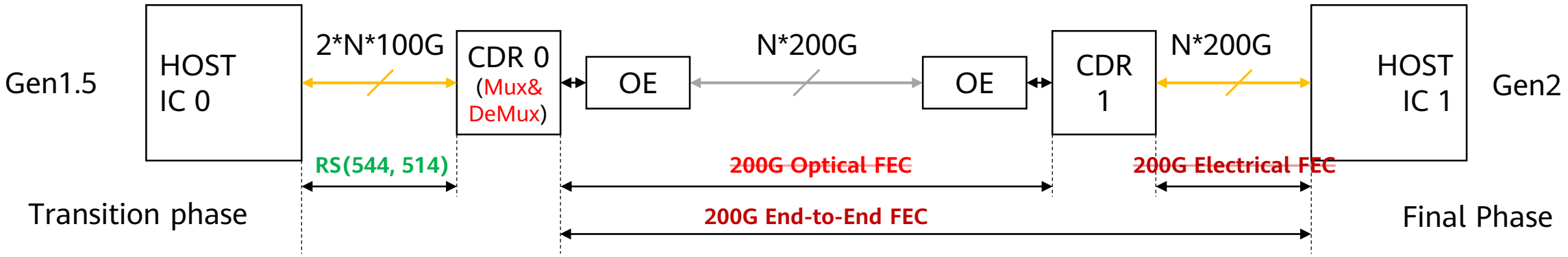
Evaluated based on 100G Electrical link. The penalty of FFE for 200G links will be larger due to the foreseen low bandwidth. For optical links, MLSE has 1~2 orders of lower BER than FFE, which corresponds to a huge improvement (2~5dB gap).

- FFE has > **2.5dB** SNR penalty compared with DFE; FFE has > **4.5dB** SNR penalty compared with MLSE (MLSE has >2dB gain over DFE).
  - Performance penalty (~1.0dB) due to error propagation of DFE and MLSE has already been accounted.
- SD-FEC can only provide < **2.0dB** net coding gain (NCG) improvement.
  - 7% Staircase ~9.41dB.
  - 15% Staircase + SD Hamming ~10.8dB.
  - NCG delta ~= **1.39dB**.
- The performance of “SD-FEC and FFE” has a huge performance gap compared with “hard decision RS code with DFE/MLSE” (~ **2dB**).

FEC architectures for 800GbE/1.6TbE

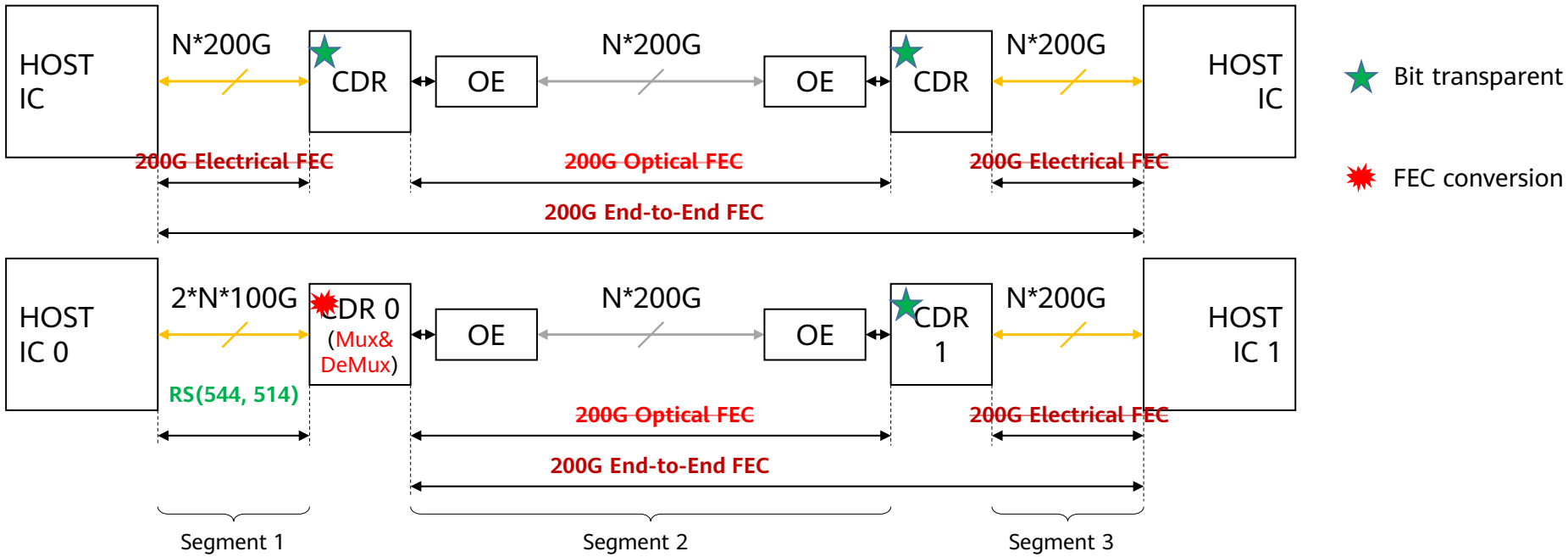


FEC architectures for 800GbE/1.6TbE (Cont'd)



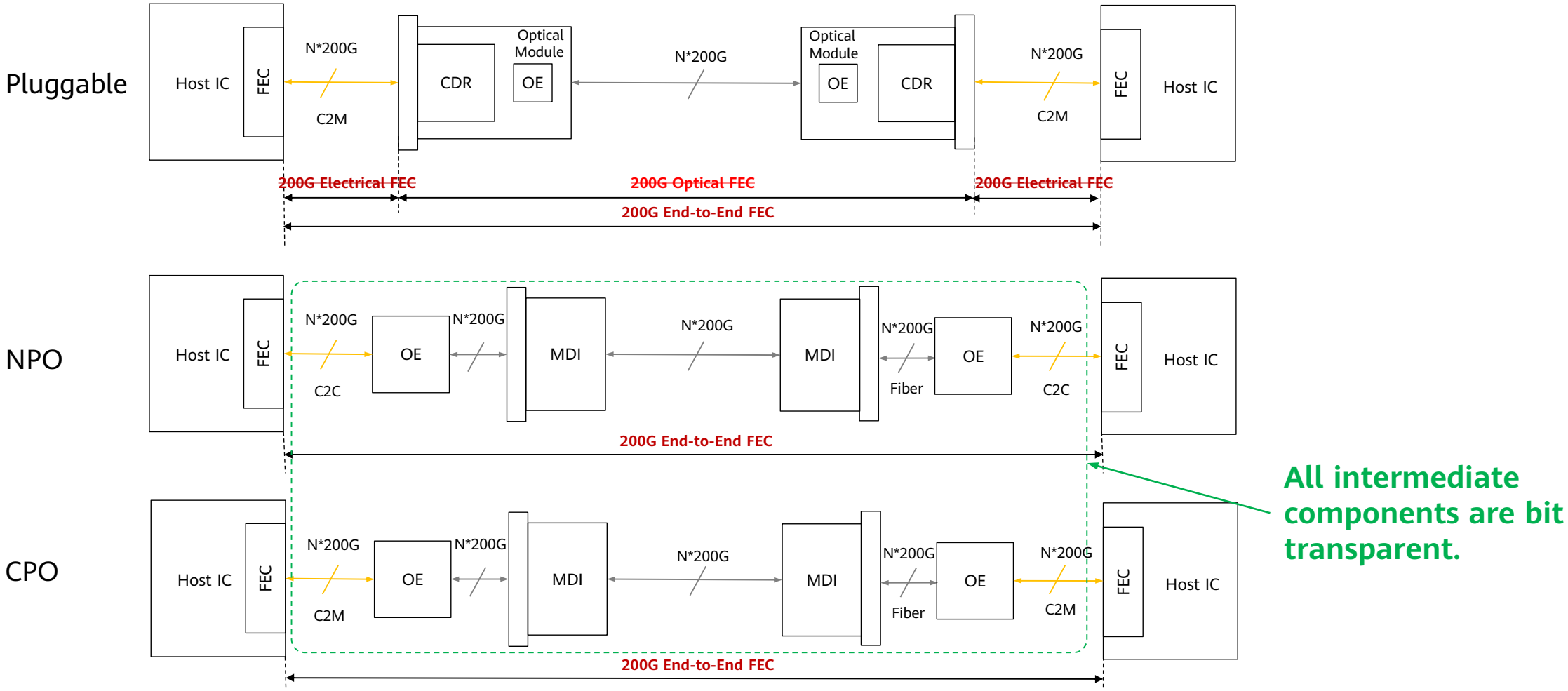
- Gen1.5 modules, 100G AUIs and 200G PMDs (**Short-term and limited market**).
  - Option 1: FEC conversion which was adopted by IEEE (**Preferred**).
  - Option 2: Concatenate RS(544, 514) with another inner FEC (**The effectiveness is questionable**).
  - Note: Options 1 and 2 has no difference from the standard perspective. RS(544, 514) decoding of Concatenated FEC architecture can be executed inside the module, if so "Concatenated FEC" becomes "Segmented FEC" .
- Gen2 modules, 200G AUIs and 200G PMDs (**Long-term broad market**).
  - Option 1: End-to-end FEC (**Preferred**).
  - Option 2: FEC conversion (**Not recommended, no gain, no future**).

Why end-to-end FEC is always preferred?



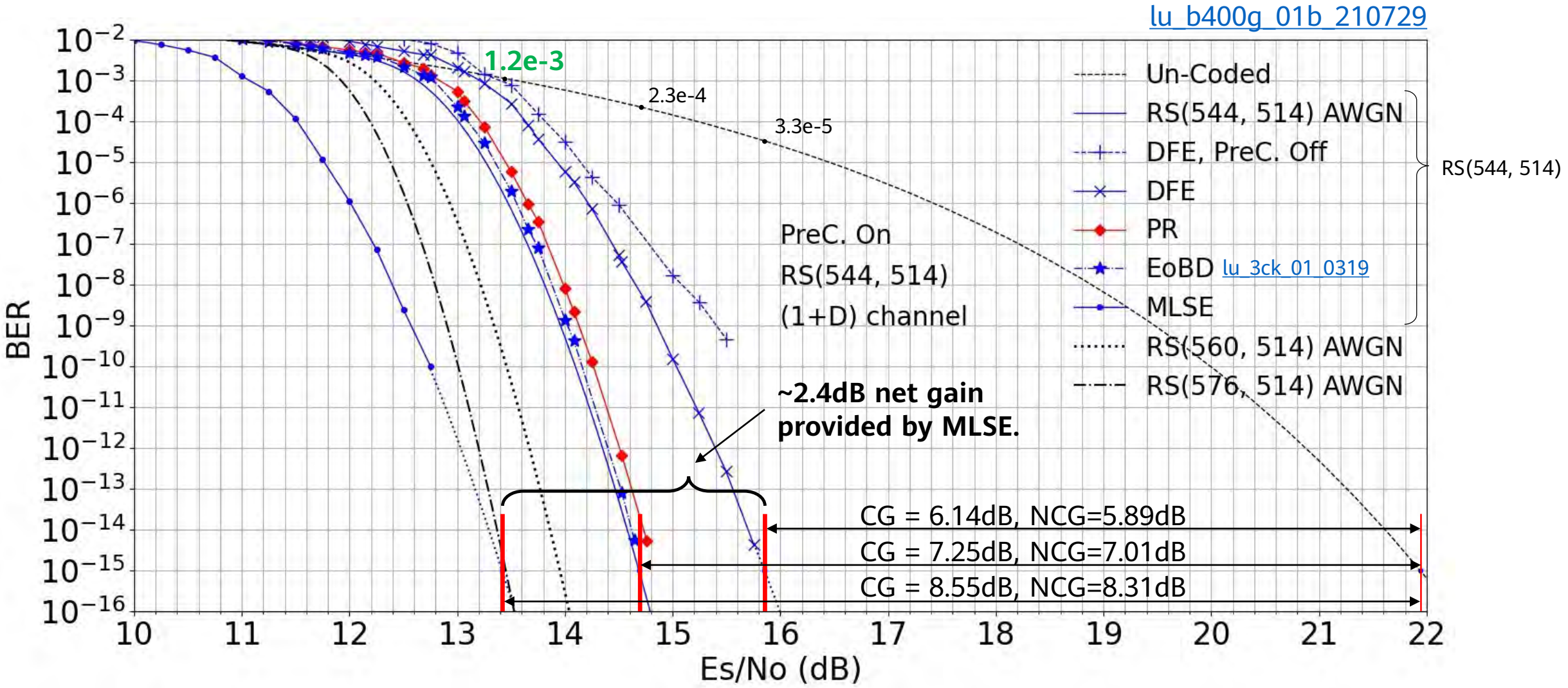
	Electrical Segment	Optical Segment	Notes
Case 1	**Tougher channel Higher BER**	Easier channel Lower BER	Choose FEC according to electrical link. (allocate 0.1dB margin for optical link) **This is likely the 200G scenario.**
Case 2	Easier channel Lower BER	**Tougher channel Higher BER**	This is 100G optical link case, electrical FEC RS(544, 514) covers end-to-end. (0.1dBo margin was allocated for electrical links ghiasi_b400g_01a_210322).
Case 3	Tie and all doable	Tie and all doable	Use the same End-to-End FEC. (allocate 0.1dB/dBo margin for each segment).
Case 4	**Tie and all tough**	**Tie and all tough**	**Not feasible, do not care.**

Why end-to-end FEC is always preferred? (Cont'd)

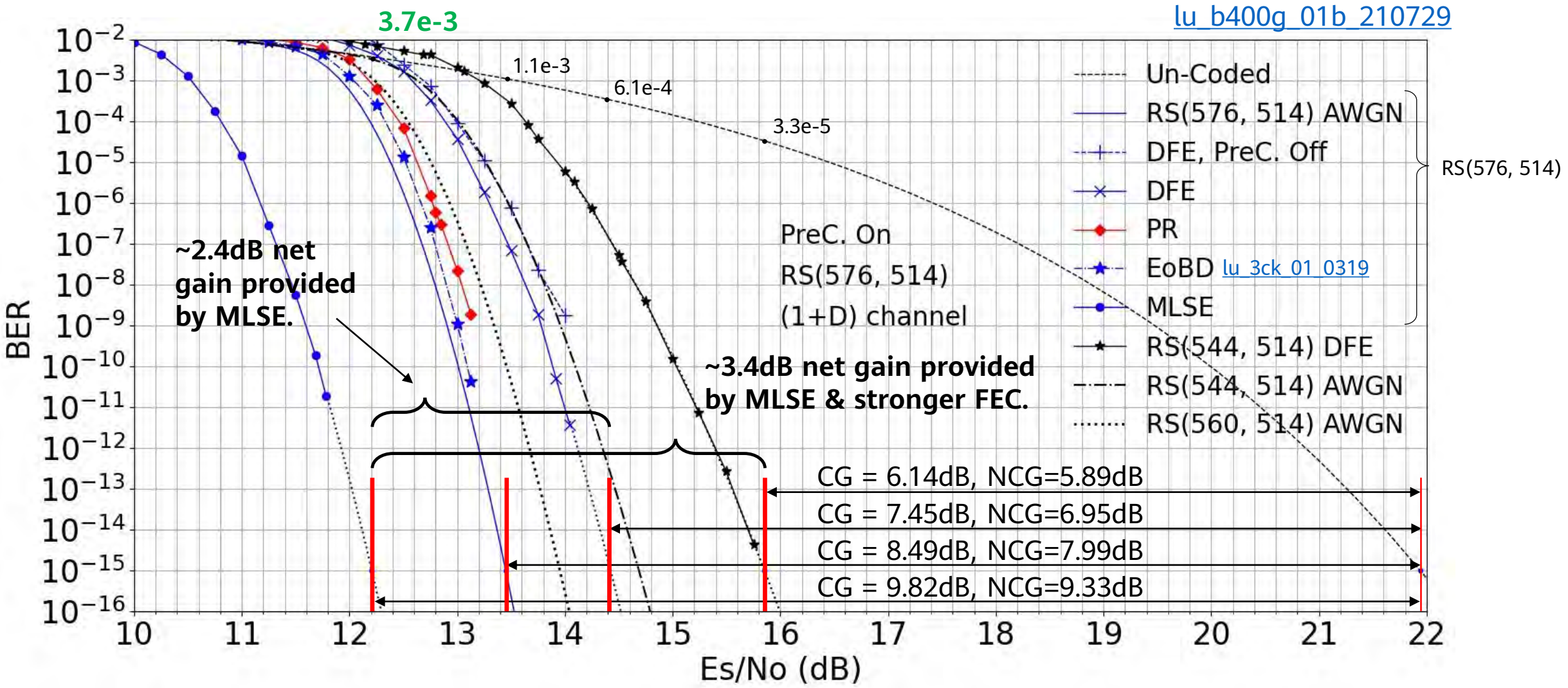


The 200G end-to-end FEC is more natural for pluggable, NPO and CPO applications.

Reference for 200G FEC: 6% OH, RS(544, 514)



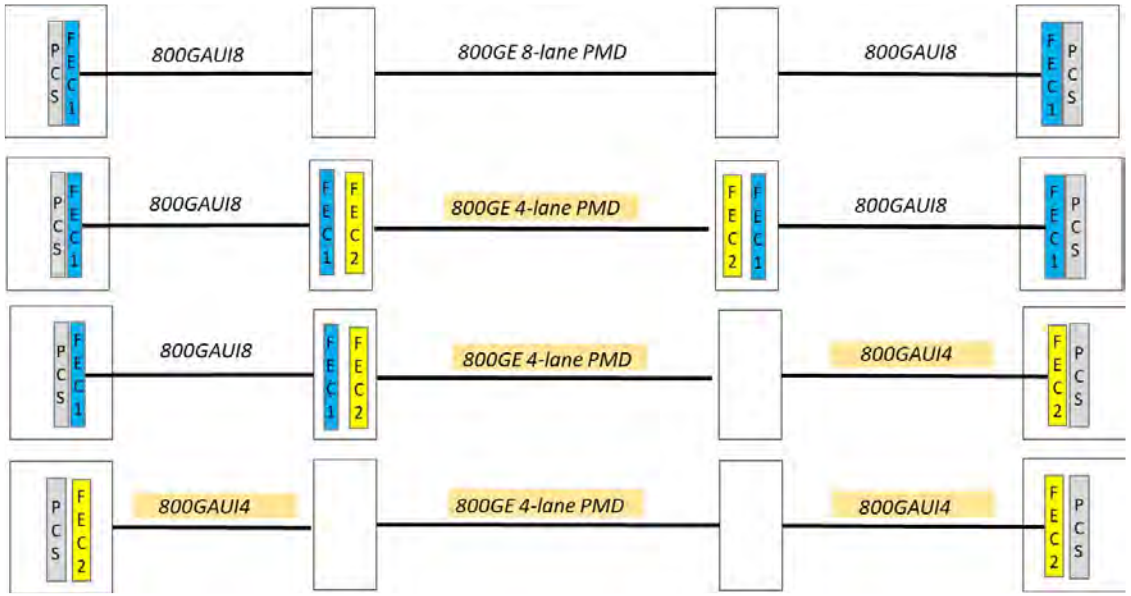
Reference for 200G FEC: 12% OH, RS(576, 514)



About the FEC architecture

shrikhande_3df_01a_220203

FEC Architecture	Illustration
End-to-End	Same FEC for all the segments. Support bit-transparent CDR.
Segmented	Different FEC for each segment. FEC are decoded and re-encoded (not needed in concatenated case) in each segment.
Concatenated	1. Use RS(544, 514) for electrical links and works as outer code and cascade with an inner FEC for the optical links. 2. The RS(544, 514) does not have to be decoded. If RS(544, 514) is decoded in the module, it is "Segmented". 3. The lane alignment, deskew and reorder are still needed. 4. Compared to segmented FEC implementation, it saves only one pair of encoders, which does not dominate in terms of complexity and latency.



Suppose a stronger FEC is really required in 200G per lane AUIs/PMDs. The architecture of "Case C : Hybrid End-to-End / Segmented" proposed in shrikhande_3df_01a_220203 seems more reasonable.

- For Gen1.5 modules, i.e. 100G AUIs and 200G PMDs.
  - Use segmented FEC architecture and do FEC conversion inside the CDR, which was adopted by IEEE.
- For Gen2 modules 200G AUIs and 200G PMDs.
  - Use End-to-End FEC architecture to support bit transparent CDR.

Summary (1)

- "**Leverage existing error correction architecture (End-to-end, hard decision, RS FEC) for 200G electrical and optical links**." should always be the priority choice.
  - Well understood by the industry, no unknown systematic issues.
  - "Improve channel" and "Use advanced DSP" are far more efficient than going for a "Stronger FEC". FEC technologies are much less efficient when go beyond RS(544, 514).
  - RS(576, 514) with MLSE probably gives the best performance among the 12% FEC codes.
  - No solid evidence shows that existing error correction architecture cannot be leveraged.
- Suppose we need a stronger FEC beyond RS(544, 514)
  - Hard decision segmented FEC is reasonable for links of 100G AUIs and 200G PMDs.
  - Hard decision end-to-end FEC is reasonable for links of 200G AUIs and 200G PMDs.
- Concatenated FEC is a special case for segmented FEC architecture
  - If the RS(544, 514) is decoded inside the CDR it becomes segmented FEC.
  - From standard and implementation perspective, there is no difference.
- With DSP considered, RS(544, 514)+Inner FEC (simple BCH, Hamming, …)
  - Hard-decision: the performance is worse than RS(576, 514).
    - Y. Lu, L. Ma, D. Mo and L. Liang, "High Gain Low Complexity Low Latency FEC Codes for Ethernet and Backplane Applications", DesignCon 2018, Santa Clara, CA, 2018.
  - Soft-decision: the performance is even worse than "RS(544, 514) + MLSE".

Summary (2)

- MLSE is far more efficient that a stronger FEC. **MLSE should be considered prior to FEC, especially the soft-decision FEC.**
- **MLSE** can provide **~2.4dB** net gain over RS(544, 514) or stronger FEC.
- **RS(576, 514) FEC** can provide **~1.0dB** net coding gain.
- **MLSE and RS(576, 514) FEC** can provide **~3.4dB** net gain.
  - Net coding gain ~= **9.33dB**
  - Pre-FEC random BER ~= **3.7e-3**.
- If we have to go back to the FFE, SD-FEC probably gives **negative gain**.
  - HD → SD FEC may give 0.4~0.5dB gain, e.g. RS(544, 514)+simple BCH.
  - MLSE → FFE gives 2.4dB loss.

Summary (3)

- Historically, an hard decision end-to-end FEC is always preferred in the industry due to its simplicity, cost-efficiency and low latency.
- There are exclusive relationships between FEC technologies (i.e. HD-FEC and SD-FEC) and DSP technologies and should be explored more deeply.
- Given a set of mixed electrical and optical generations defined in this task force, an appropriate FEC architecture should leverage several factors, including:
  - Performance including Net coding gain/overhead and its cooperation with advanced DSP technologies (i.e. “FFE+SD-FEC” vs. “HD-FEC + FFE/DFE/MLSE”).
  - Cost efficiency, e.g. area, power
  - Latency
  - Broad Market Potential (i.e. evolution to the final phase)
  - …

Thanks!
Q&A