PAM4 vs PAM 6 Modulation Choice for 200GEL

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Supporters

- John Calvin, Keysight
- Piers Dawe, NVIDIA
- Mike Dudek, Marvell
- Brandon Gore, Samtec
- Richard Mellitz, Samtec
- Rick Rabinovich, Keysight
- Pavel Zivny, Tektronix

Introduction

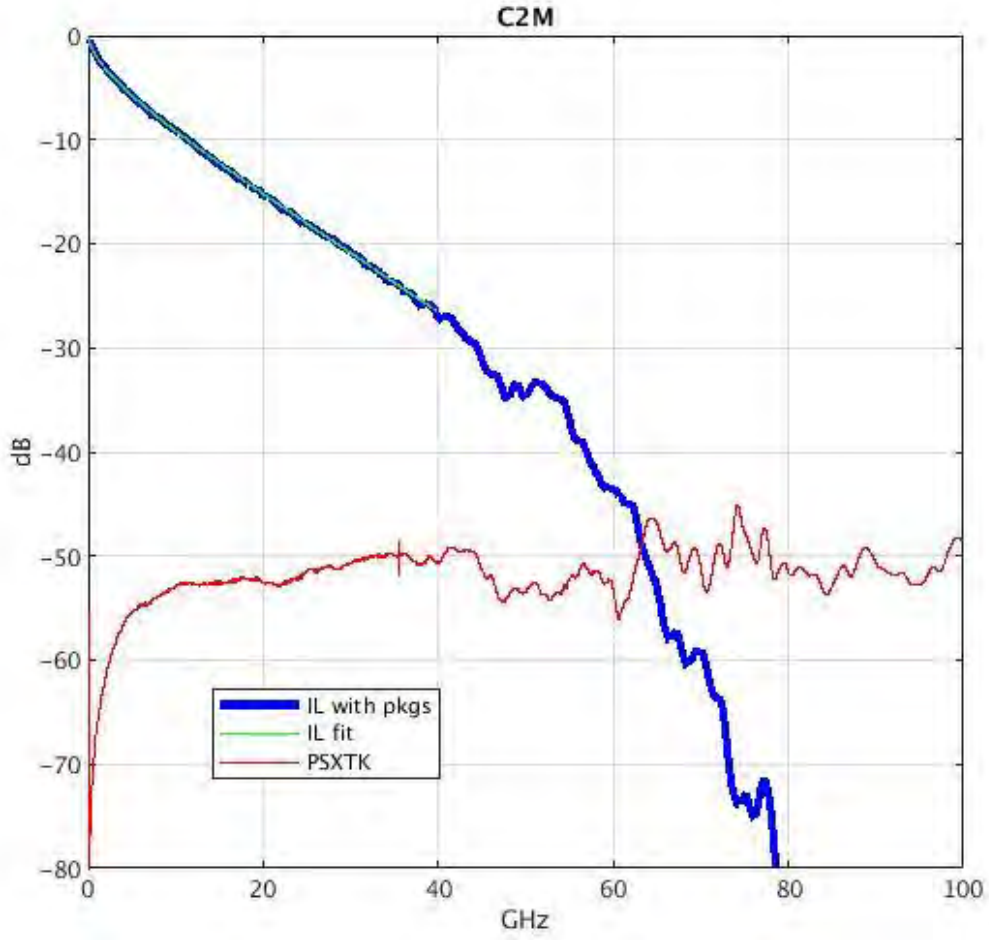
- Study two representative channels to show PAM4 versus PAM6 performance:
  - VSR (C2M) channel for pluggable modules
  - CR channel with co-packaged-copper and 0.5 m passive cable

- We compare PAM4 versus PAM6 choice for modulation at the same data rate, 212.5 Gb/s
  - PAM6 has lower baud rate compared to PAM4 [1]
    - PAM4: 106.25 GBd
    - PAM6: 85 GBd

[1]: https://www.ieee802.org/3/B400G/public/21_03/healey_b400g_01a_210329.pdf

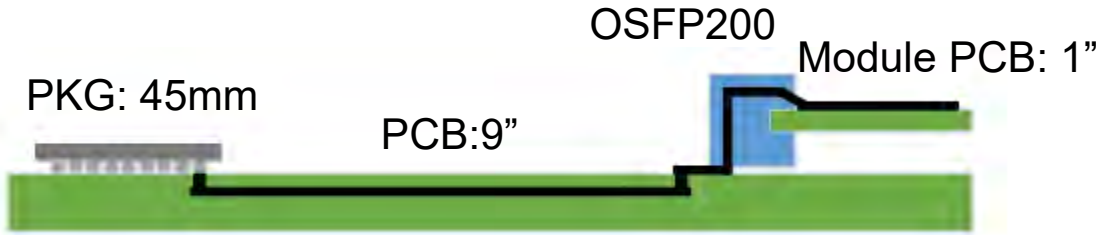
Channels

VSR or C2M Channel



Refer to backup slide for return loss plot

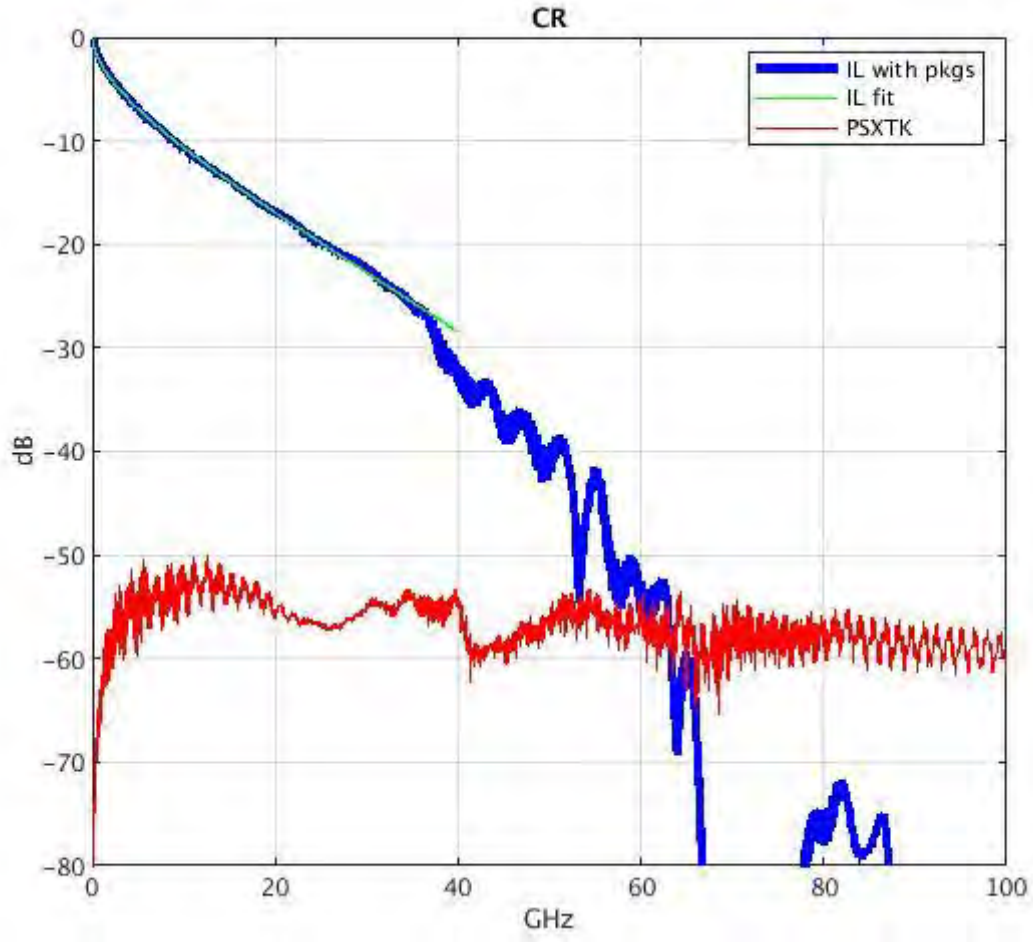
Bump to Bump C2M Channel:
Switch to Pluggable Module Retimer



PCB: 1.5 dB/inch @ 53 GHz; Zo = 95 ohm
PKG: 5 dB/inch @ 53 GHz; Zo = 86 ohm
Includes 7-FEXT and 8-NEXT
Die and bump parasitics are included

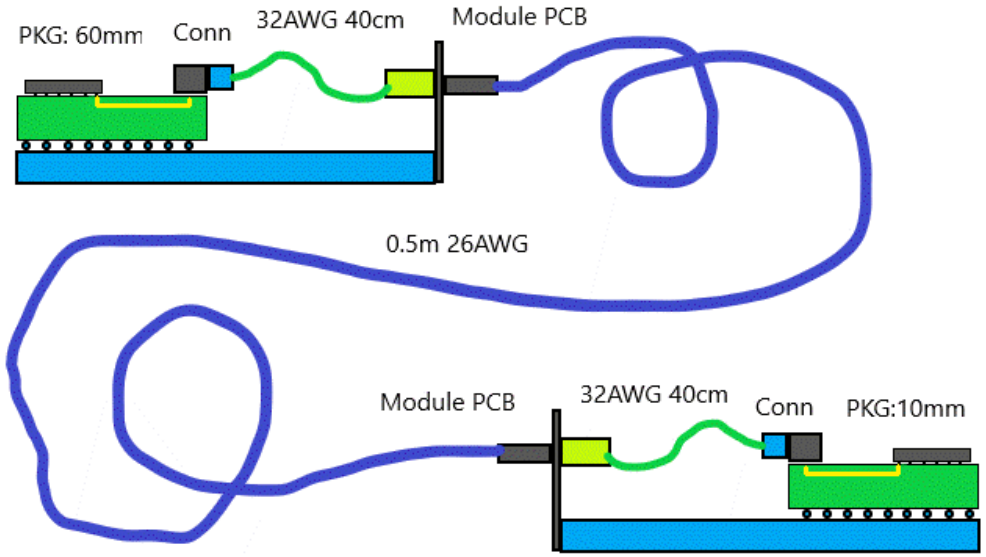
*Picture sourced from:
https://www.ieee802.org/3/B400G/public/21_08/kocsis_b400g_01a_210826.pdf

CR Channel



Refer to backup slide for return loss plot

Bump to Bump Cabled Channel:
Co-Packaged-Copper with OSFP200 Connectors



PKG: 5.0 dB/inch @ 53 GHz; Zo = 86 ohm
Includes 7-FEXT + 8-NEXT
Cable 18 dB/m @ 53 GHz for 32 AWG
Cable 7.5 dB/m @ 53 GHz for 26 AWG
Die and bump parasitics are included

PAM4 and PAM6 Simulation Configuration

PAM4 Config File

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0,0]	nF	[TX RX]
L_s	[0,0]	nH	[TX RX]
C_b	[0,0]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[0,0; 0,0]	mm	[test cases]
z_p (NEXT)	[0,0; 0,0]	mm	[test cases]
z_p (FEXT)	[0,0; 0,0]	mm	[test cases]
z_p (RX)	[0,0; 0,0]	mm	[test cases]
C_p	[0,0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.45	V	
A_fe	0.45	V	
A_ne	0.55	V	
AC_CM_RMS	0	V	[test cases]
L	4		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02: 0]		[min:step:max]
c(1)	[-0.2:0.02:0]		[min:step:max]
N_b	24	UI	
b_max(1)	1		
b_max(2..N_b)	.9 0.3*ones(1,11) 0.1*ones(1,11)]		
b_min(1)	0.3		
b_min(2..N_b)	[0.05 -0.03*ones(1,22)]		
g_DC	[-20:2:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\200GEL_KR_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	9.7	dB
DER_0	0.0001	
T_r	0.00284	ns
FORCE_TR	1	logical
Local Search	2	
BREAD_CRUMBS	1	logical
SAVE_CONFIG2MAT	1	logical
PLOT_CM	0	
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3500	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0]	[port1 port2]
TDR_W_TXPKG	0	
N_bx	21	UI
Tukey_Window	1	logical
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.01	UI
eta_0	2.00E-09	V^2/GHz
SNR_TX	34	dB
R_LM	0.97	

Table 93A–3 parameters		
Parameter	**Setting**	**Units**
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	0.006141	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	*[0 3.8206e-04 9.5909e-05]*	
board_tl_tau	*5.790E-03*	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	*110.3*	mm
z_bp (NEXT)	*110.3*	mm
z_bp (FEXT)	*110.3*	mm
z_bp (RX)	*110.3*	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	**0**	**logical**
Floating Tap Control		
N_bg	3	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	32	UI span for floating taps
bmaxg	0.05	max DFE value for floating taps
B_float_RSS_MAX	0.02	rss tail tap limit
N_tail_start	26	(UI) start of tail taps limit
ICN & FOM_ILD parameters		
f_v	0.784	*Fb
f_f	0.784	*Fb
f_n	0.784	*Fb
f_2	40.000	GHz
A_ft	0.600	V
A_nt	0.600	V
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
new		

PAM6 Config File

Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	85	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0,0]	nF	[TX RX]
L_s	[0,0]	nH	[TX RX]
C_b	[0,0]	nF	[TX RX]
z_p select	[1]		[test cases to run]
z_p (TX)	[0,0; 0,0]	mm	[test cases]
z_p (NEXT)	[0,0; 0,0]	mm	[test cases]
z_p (FEXT)	[0,0; 0,0]	mm	[test cases]
z_p (RX)	[0,0; 0,0]	mm	[test cases]
C_p	[0,0]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.45	V	
A_fe	0.45	V	
A_ne	0.55	V	
AC_CM_RMS	0	V	[test cases]
L	6		
M	32		
filter and Eq			
f_r	0.75	*fb	
c(0)	0.54		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	[-0.06:0.02: 0]		[min:step:max]
c(1)	[-0.2:0.02:0]		[min:step:max]
N_b	24	UI	
b_max(1)	1		
b_max(2..N_b)	.9 0.3*ones(1,11) 0.1*ones(1,11)]		
b_min(1)	0.3		
b_min(2..N_b)	[0.05 -0.03*ones(1,22)]		
g_DC	[-20:2:0]	dB	[min:step:max]
f_z	34	GHz	
f_p1	34	GHz	
f_p2	85	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.0625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\200GEL_KR_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	9.7	dB
DER_0	0.0001	
T_r	0.00355	ns
FORCE_TR	1	logical
Local Search	2	
BREAD_CRUMBS	1	logical
SAVE_CONFIG2MAT	1	logical
PLOT_CM	0	
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3500	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0]	[port1 port2]
TDR_W_TXPKG	0	
N_bx	21	UI
Tukey_Window	1	logical
Noise, jitter		
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A_DD	0.01	UI
eta_0	2.00E-09	V^2/GHz
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R_LM	0.95	

Table 93A–3 parameters		
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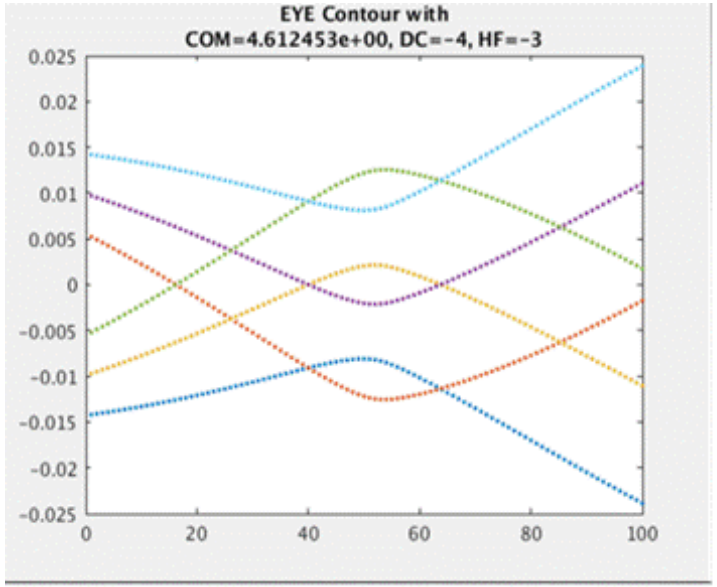
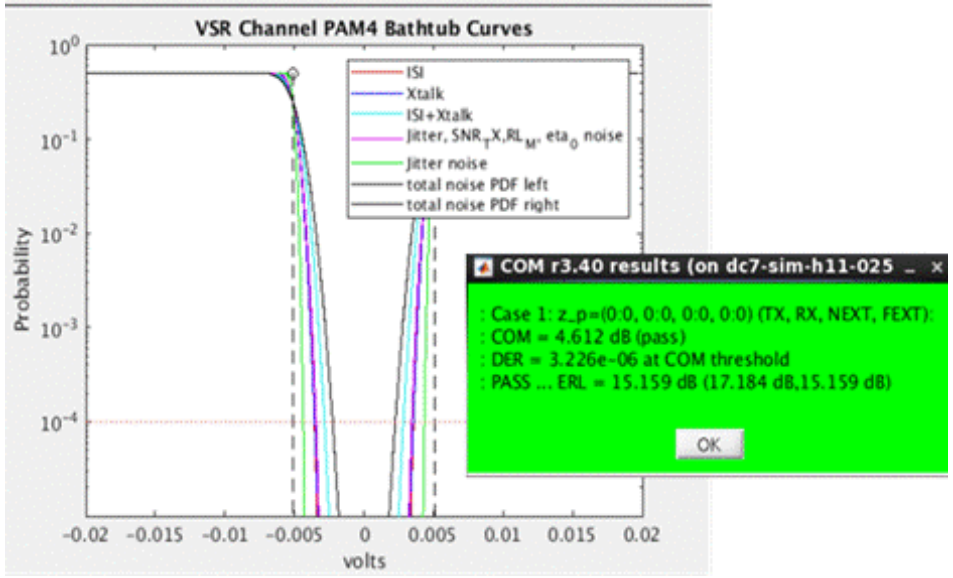
z_bp (NEXT)	*110.3*	mm
z_bp (FEXT)	*110.3*	mm
z_bp (RX)	*110.3*	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	**0**	**logical**
Floating Tap Control		
N_bg	3	0 1 2 or 3 groups
N_bf	3	taps per group
N_f	32	UI span for floating taps
bmaxg	0.05	max DFE value for floating taps
B_float_RSS_MAX	0.02	rss tail tap limit
N_tail_start	26	(UI) start of tail taps limit
ICN & FOM_ILD parameters		
f_v	0.784	*Fb
f_f	0.784	*Fb
f_n	0.784	*Fb
f_2	40.000	GHz
A_ft	0.600	V
A_nt	0.600	V
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
new		

COM Results

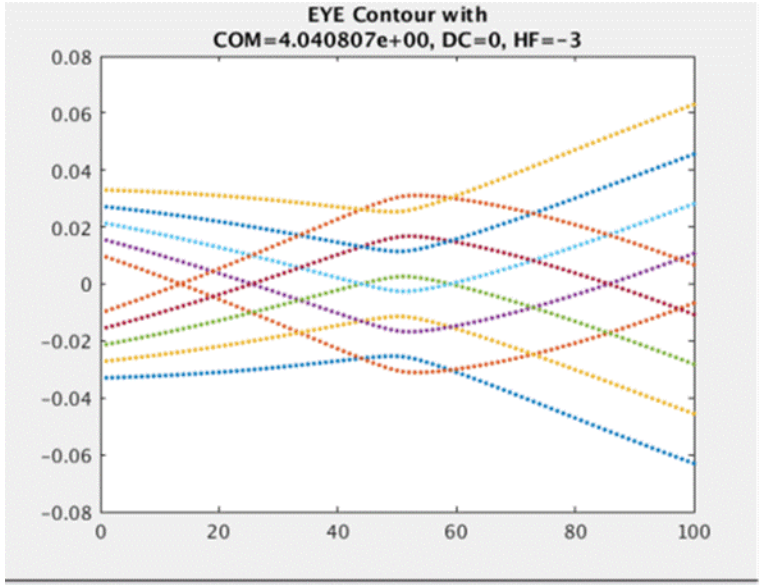
VSR Channel Results

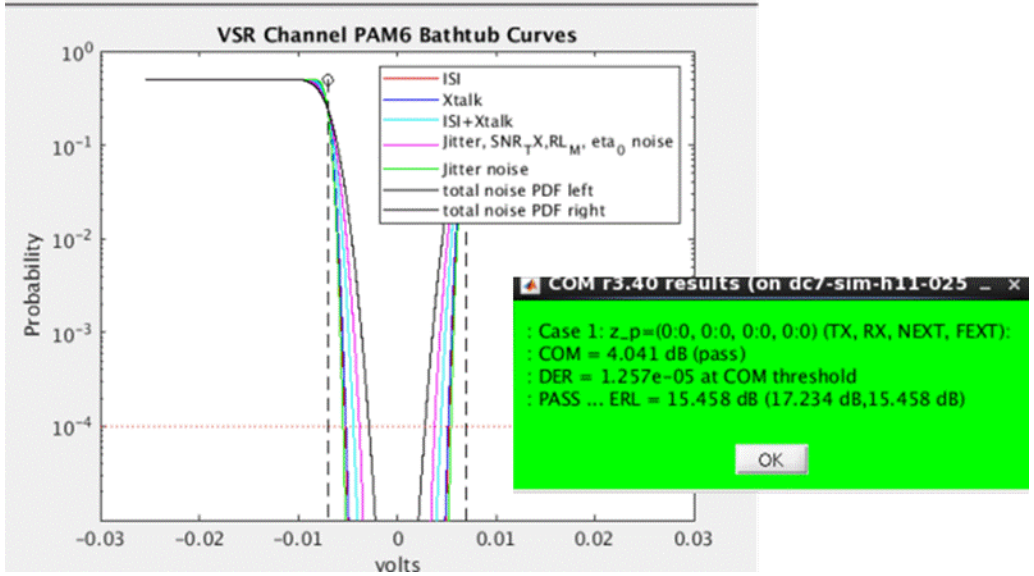
PAM4





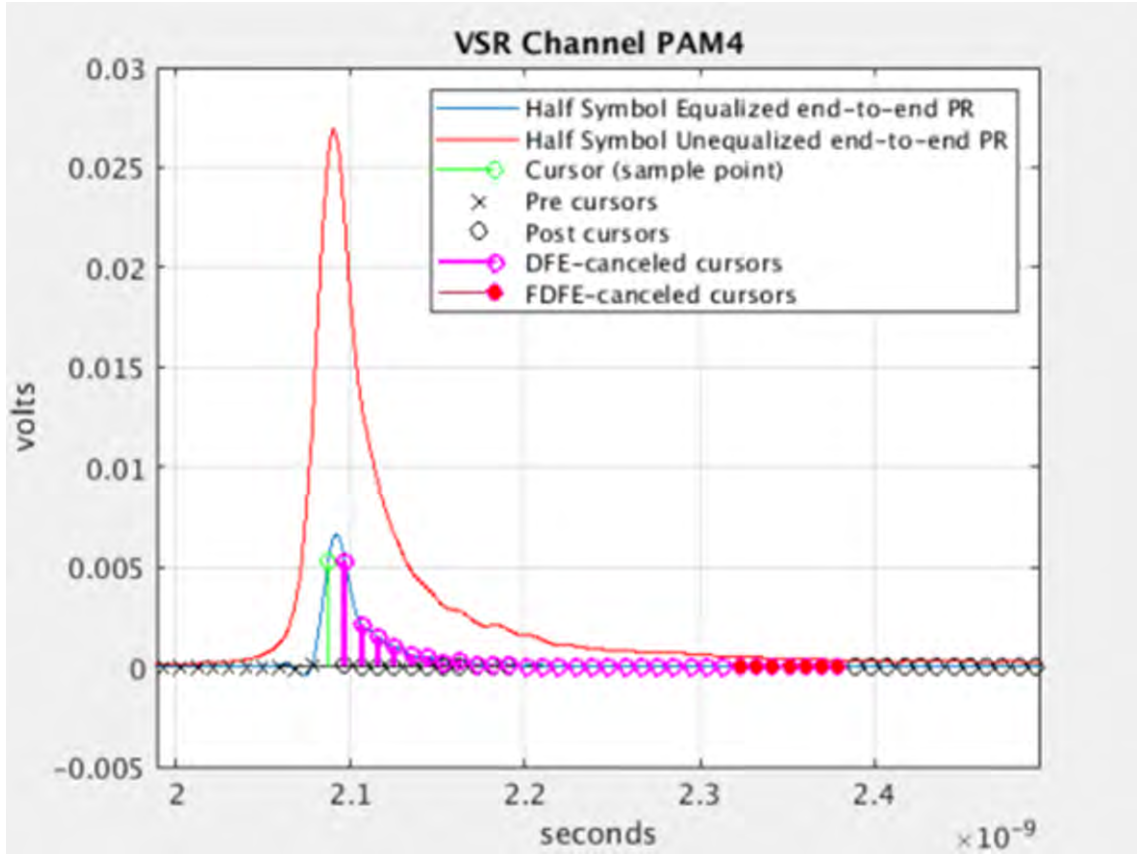
PAM6



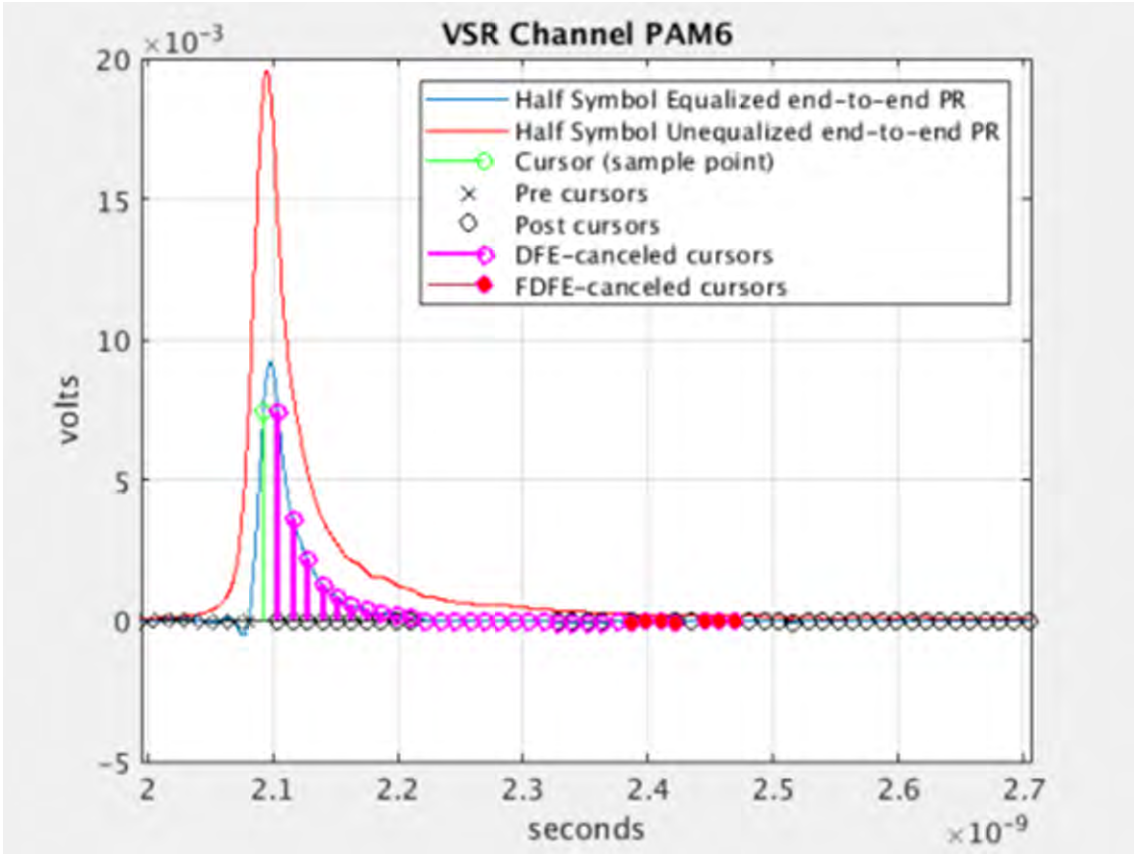


VSR Channel Results

PAM4

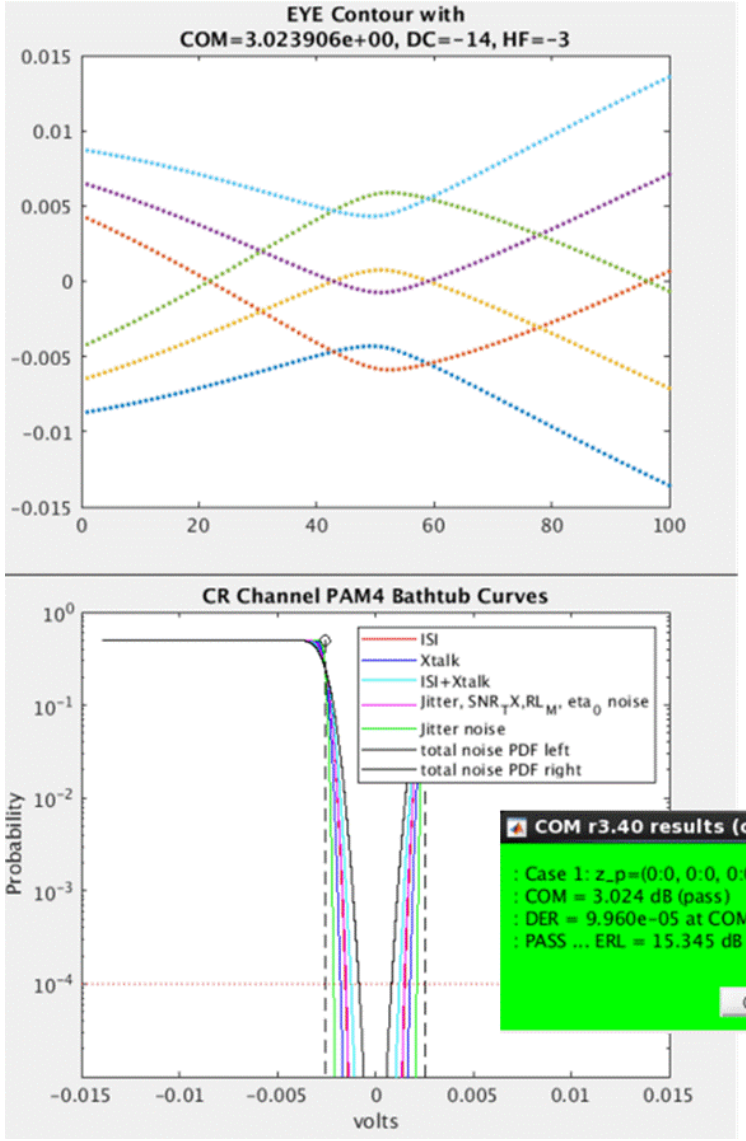


PAM6

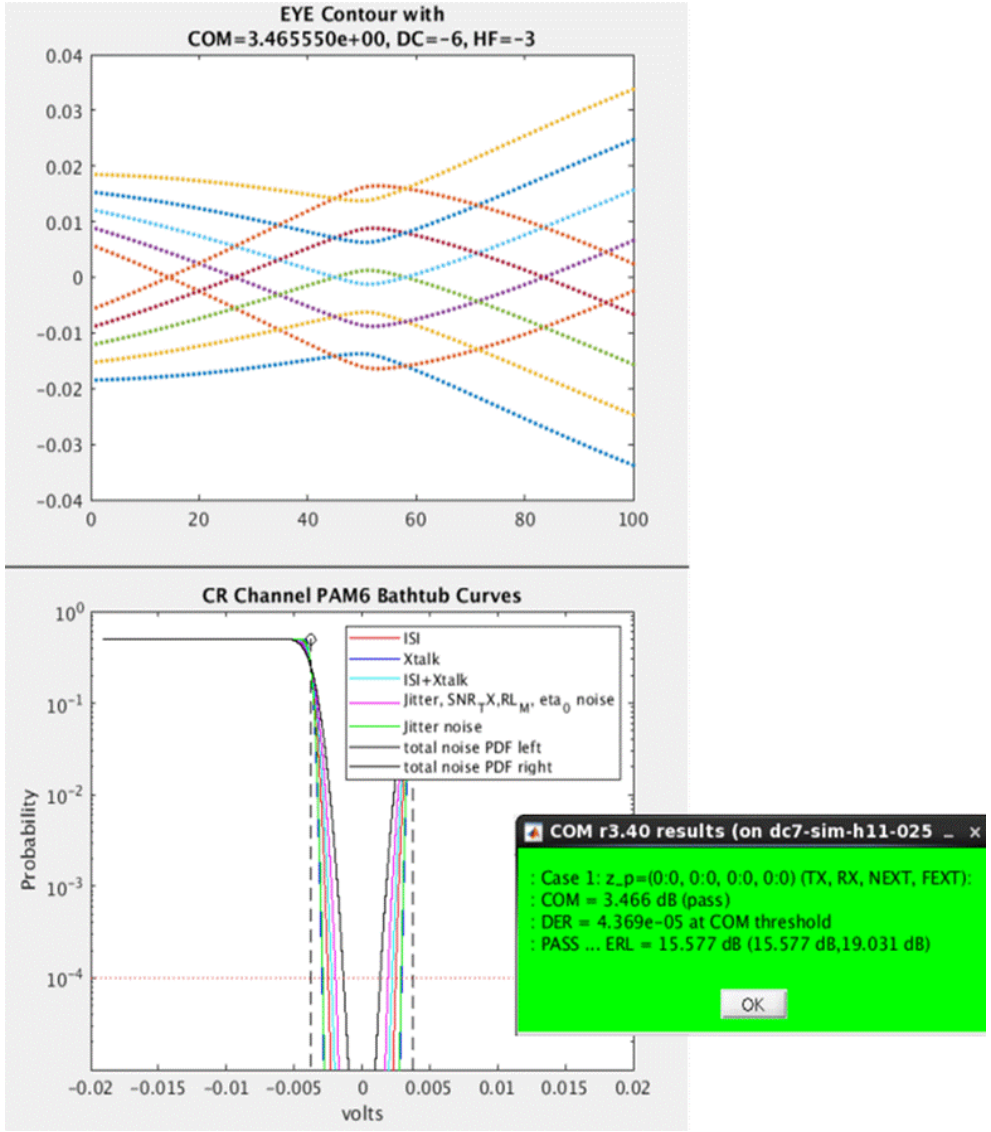


CR Channel Results

PAM4

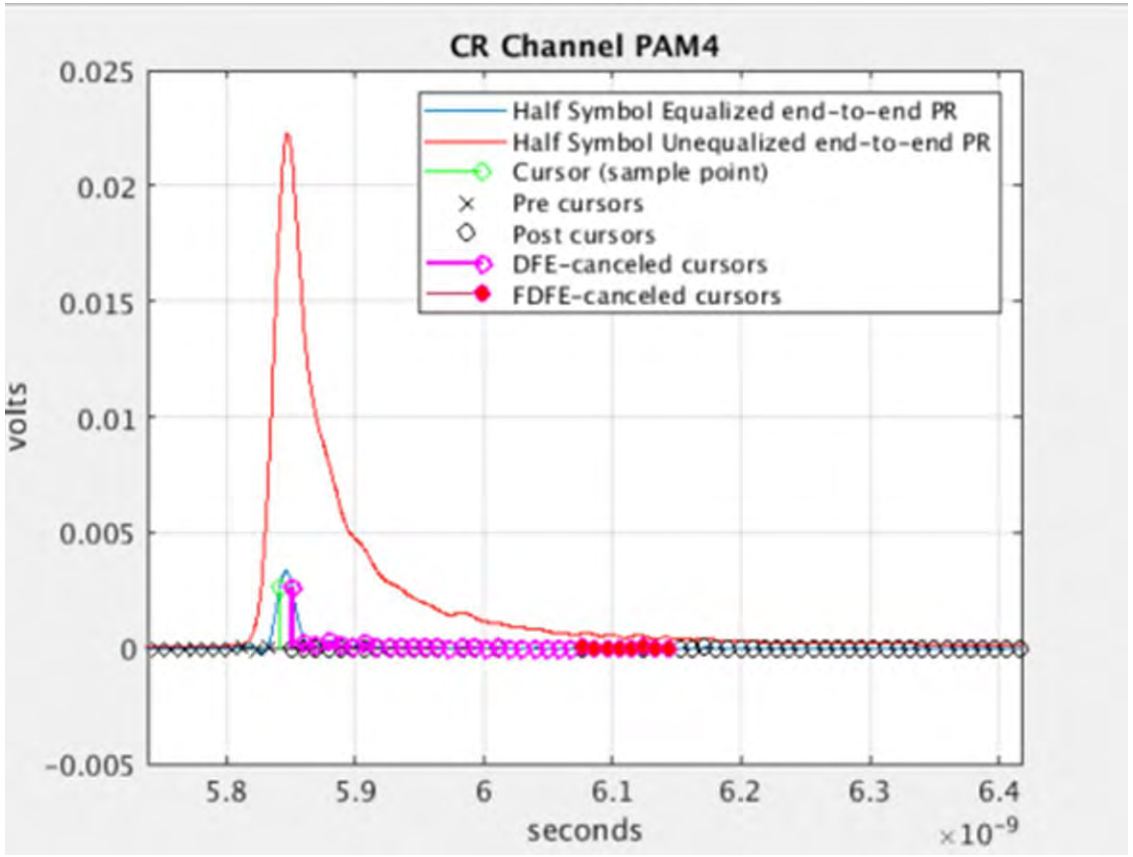


PAM6

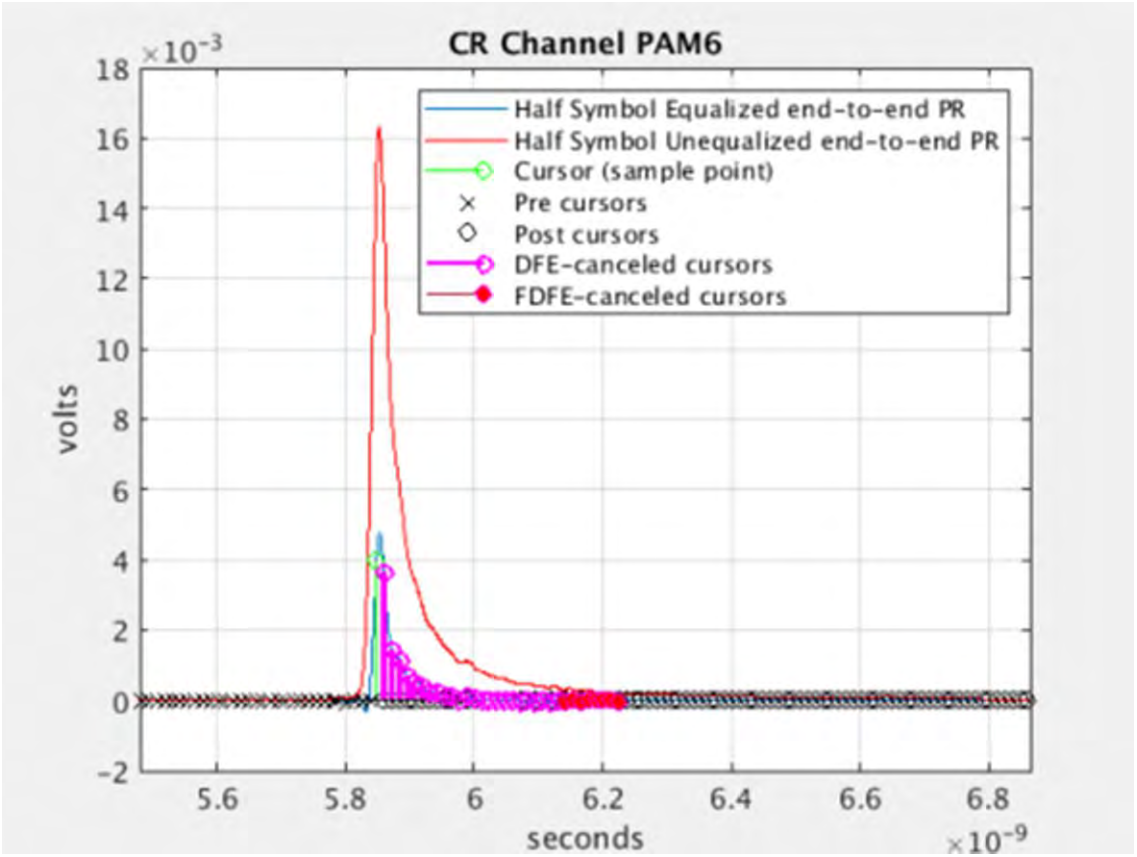


CR Channel Results

PAM4



PAM6

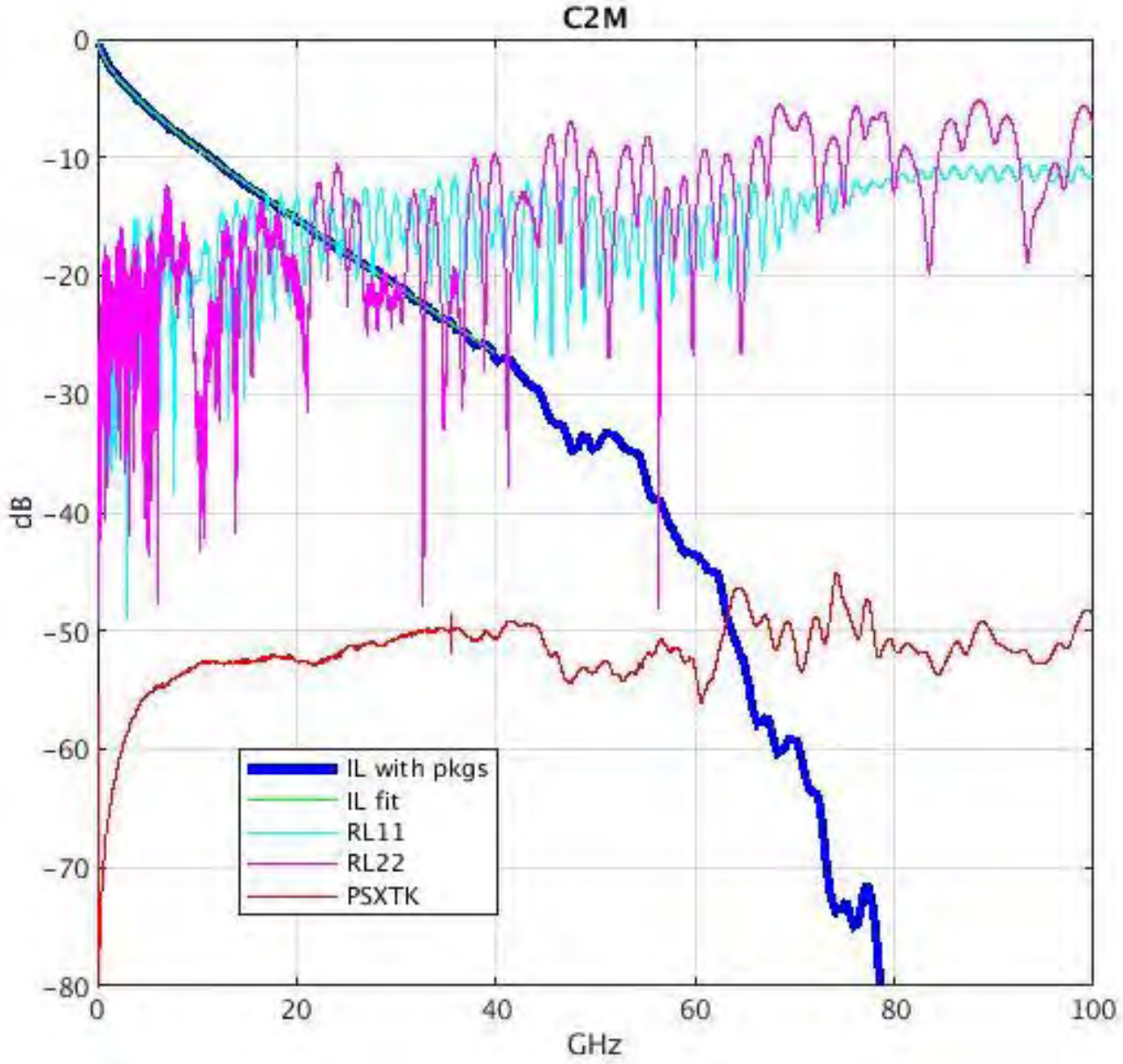


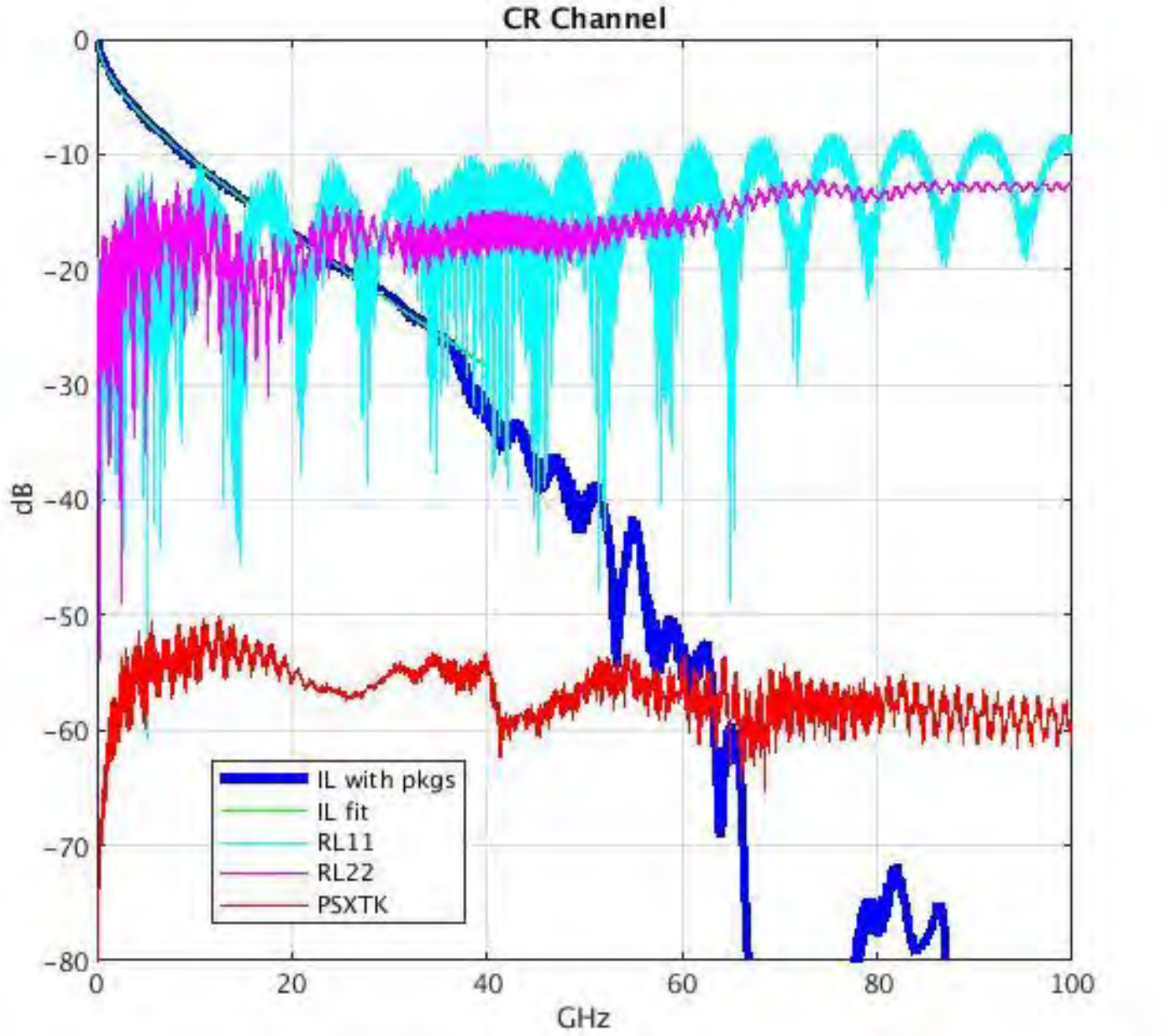
Conclusion

- For C2M channels:
  - PAM4 works better than PAM6 and is the best choice
- For CR channels:
  - PAM4 is good enough and considering other reasons, it is the preferred choice
- PAM4 is the better and preferred modulation choice for 200GEL for the following reasons:
  - Backward compatible with legacy speeds which are also PAM4 in 50G and 100G
  - Line side Optics is already proceeding with PAM4. It is the best choice for Host side Electrical interface as well to avoid rate mismatches
  - Preliminary COM analysis suggests PAM4 is better or at most comparable performance to PAM6.
  - PAM6 will likely need stronger FEC compared to PAM4. This would result in line rate increase thereby giving up the baud rate advantage.
  - Linearity requirements for PAM6 will be harder to meet than PAM4

Thank You!

Backup


C2M
0
-10
-20
-30
-40
-50
-60
-70
-80
dB
0
20
40
60
80
100
GHz
IL with pkgs
IL fit
RL11
RL22
PSXTK


CR Channel
0
-10
-20
-30
-40
-50
-60
-70
-80
dB
0
20
40
60
80
100
GHz
IL with pkgs
IL fit
RL11
RL22
PSXTK