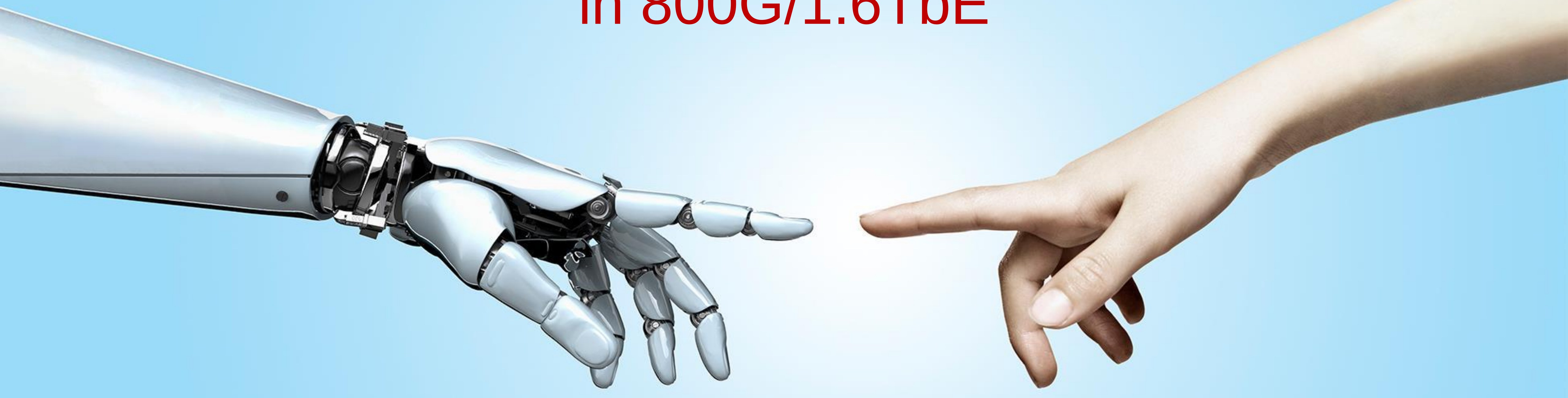
FEC Code and Scheme Observation in 800G/1.6TbE



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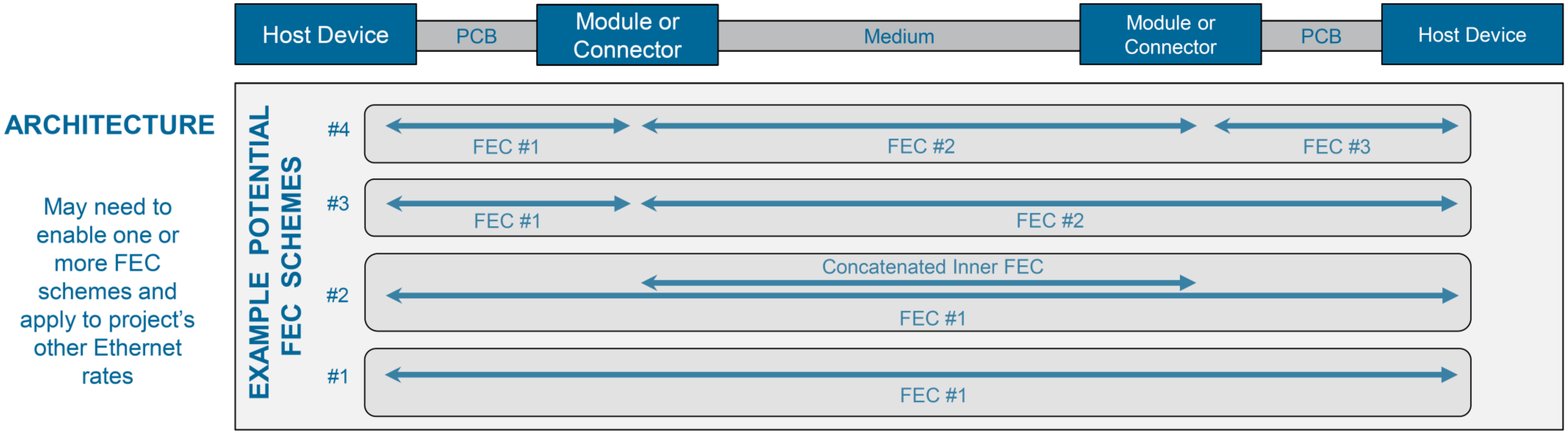
Motivation

- In Project Overview - IEEE P802.3df: 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet of Study Group



- **An initial holistic approach to start** is recommended to develop an architecture that would support one or more FEC schemes
  - This requires significant analysis and technical decisions by the Task Force

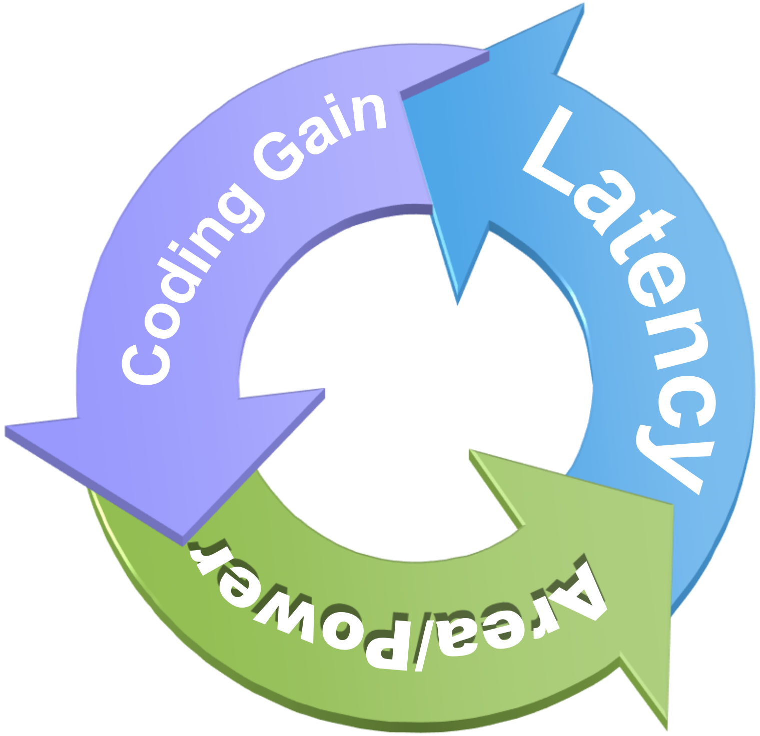
- In this presentation, we share observation of FEC related topic of logic layer to help move forward.

Terminology of Forward Error Correction

- **FEC Code (Algorithm): General term from information theory perspective**
  - "In telecommunication, information theory, and coding theory, forward error correction (FEC) or channel coding is a technique used for controlling errors in data transmission over unreliable or noisy communication channels. The central idea is that the sender encodes the message in a redundant way, most often by using an ECC.
  - The redundancy allows the receiver to detect a limited number of errors that may occur anywhere in the message, and often to correct these errors without re-transmission. FEC gives the receiver the ability to correct errors without needing a reverse channel to request re-transmission of data, but at the cost of a fixed, higher forward channel bandwidth.
  - https://en.wikipedia.org/wiki/Error_correction_code#Forward_error_correction
- **FEC Scheme (Architecture): Defining how a particular FEC code is used in applications**
  - Similar terminology in RFC 5052 Forward Error Correction (FEC) Build Block: "An FEC scheme defines the ancillary information and procedures which, combined with an FEC code or algorithm specification, fully define how the FEC code can be used with CDPs"
- **In Ethernet standard, physical layer (especially PCS/PMA), electrical and optical lane technologies will further influence the FEC code and scheme selection.**

Key Performance Factors to Evaluate a FEC Code

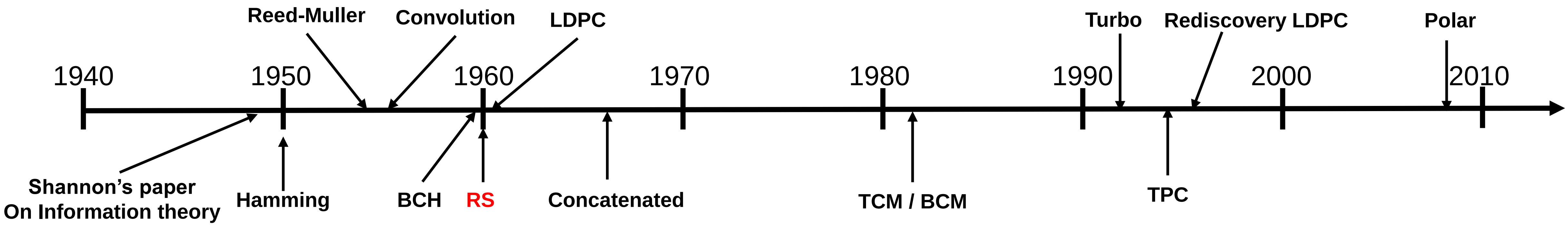
- Tradeoff needed on additional overhead of transceivers and links, with error correct performance.
- The commonality and difference between electrical and optical link will both influence FEC code selection.



- In general, longer FEC codeword and higher error correction performance will lead to higher latency.
- Higher parallelism in circuit implementation can lower latency by some degree.

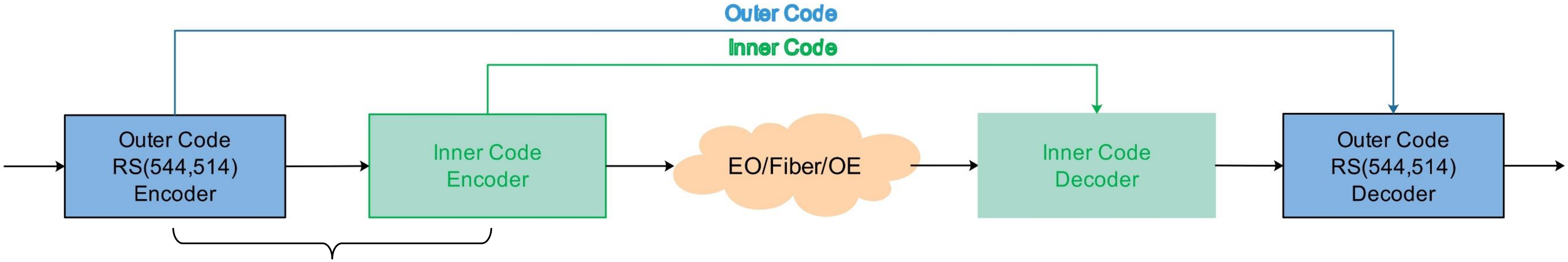
- Hardware implementation complexity can be mostly represented by area and power.
- Higher parallelism in circuit implementation will generally increase area and power.
- Tradeoff needed between area/power and latency, which is mostly an implementation challenge, and does not impact interoperability.

History of Forward Error Correction Code



- RS(544,514), which is widely used in 50, 200, 400GbE, etc., is a linear systematic block code based on GF(2^{10}) and can be expressed with linear algebra.
- RS/BCH and most Hamming codes can be built on similar linear algebra and theory.
- RS/BCH/Hamming codes can be used as basic components to build higher capability FEC codes in industry, such as Concatenated, CFEC, oFEC, TPC, etc.

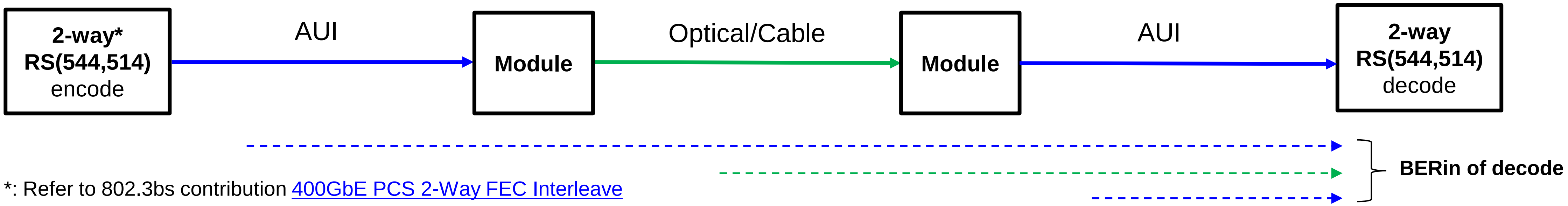
Further Information of a Concatenated FEC Code



Example of a Concatenated FEC code

- Concatenated FEC code consists of an outer code and an inner code, which work together to correct the errors in the message and is first introduced by G.D. Forney' paper *Concatenated codes* in 1965.
- In general, outer code has higher coding gain than inner code. As an example, for 400GBASE-ZR specified in 802.3cw, staircase FEC is used as the outer code and soft decision Hamming code is used as the inner code.
- Using RS(544,514) as the outer code and BCH/Hamming as the inner code is another example in industry, similar structure as I.4 of ITU-T G.975.1 : Forward error correction for high bit-rate DWDM submarine systems.

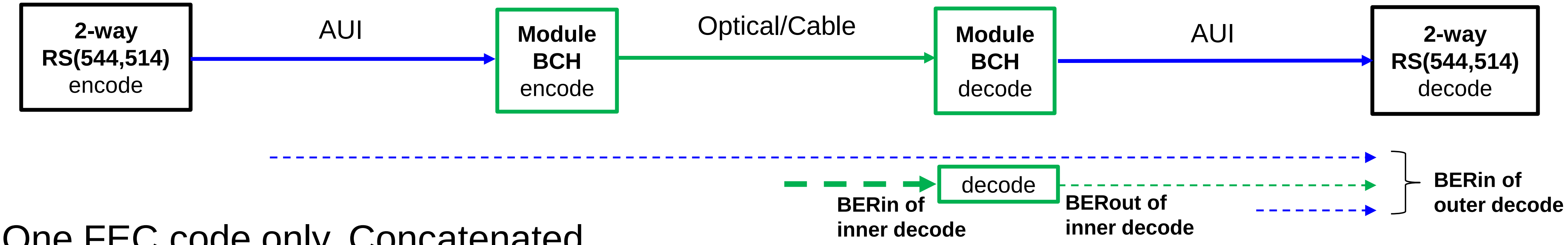
FEC Scheme A: End to End



*: Refer to 802.3bs contribution 400GbE PCS 2-Way FEC Interleave

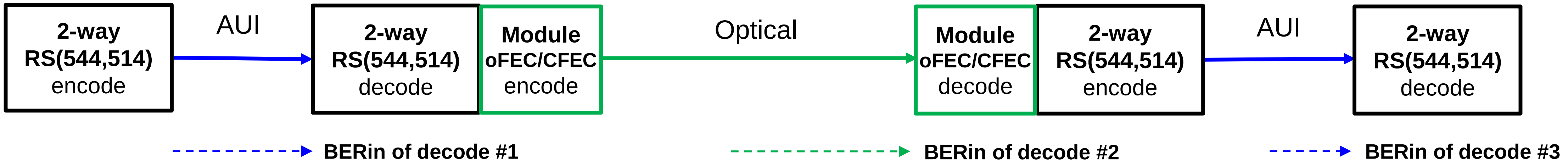
- One FEC code only.
- At the end of receive side, one decoder corrects all errors caused by the whole link, such as two instances of AUI and the optical or copper cable link.
- Any FEC code can fit in this scheme in principle, such as RS, BCH, Hamming, Concatenated, CFEC, oFEC, etc.
- Reuse of RS(544,514) from 802.3bs/cu/ck is most likely to enable backward compatibility to 100 Gb/s per lane AUI and PHY.

FEC Scheme B: Encapsulated or Concatenated



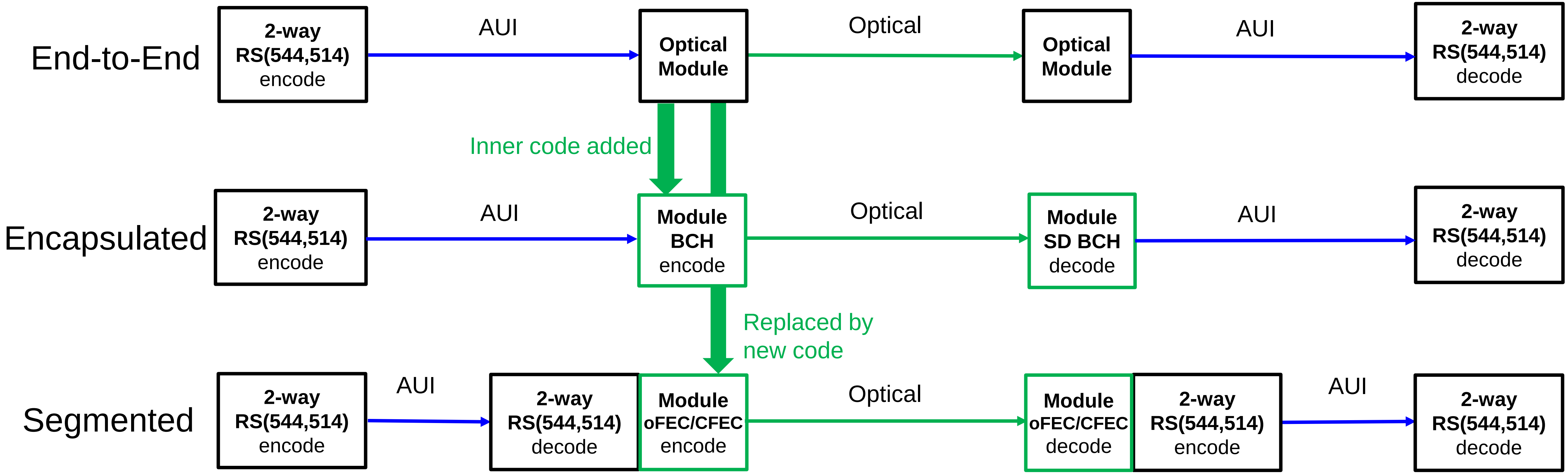
- One FEC code only, Concatenated.
- At receive side of the inner decoder, it corrects errors caused by the inner link only, such as the optical link.
- At receive side of the outer decoder, it corrects errors caused by all of the link, such as two instances of AUI and the left-over errors from the optical or copper cable link.
- Use RS(544,514) from 802.3bs/cu/ck as the outer code for both random and burst error tolerance and SD/HD BCH/Hamming as the inner code to lower the raw BER is one approach to enable 100 Gb/s and 200 Gb/s per lane optical link.

FEC Scheme C: Segmented



- Three independent FEC codes for three segments (part of a link).
- At receive side of each segment, such as AUI or optical link, the decoder will correct errors caused by its corresponding segment only.
- Reuse of RS(544,514) from 802.3bs/cu/ck is most likely for 100 Gb/s per lane AUIs. For 200 Gb/s per lane optical link, FEC code selection depends on the target BER.
- Higher performance FEC code, most likely >8dB CG comparing to ~6.4dB of RS(544,514) code, is needed if optical link is operating at BER of ~2E-3.

A Hybrid Architecture to Enable All FEC Schemes



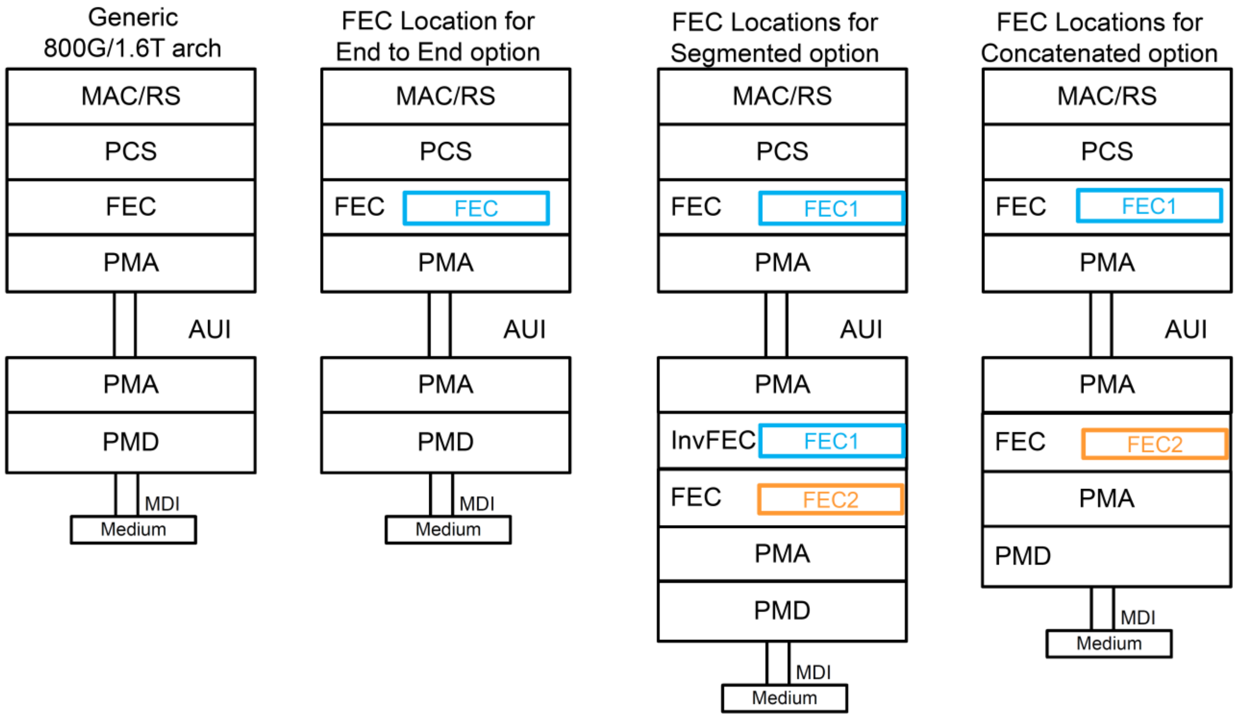
- In 802.3bs, we agreed on E2E FEC scheme based on RS(544,514). But in 802.3cw, this scheme is extended to segmented FEC scheme to use CFEC.
- The differences between encapsulated and segmented scheme from implementation perspective is whether to terminate RS(544,514). A new FEC in the module, weak or strong, is added either way.

Separated FEC Sublayer within Logic Layer Stack

- Refer to Slide #27 of gustlin_3df_01_220118;
  - FEC1 is 2-way interleaved RS(544,514) and FEC2 can be a new inner BCH/Hamming code or oFEC/CFEC.

FEC in a Possible 800GbE/1.6TbE Architecture

- How 200G/Lane FEC options fit into the architecture



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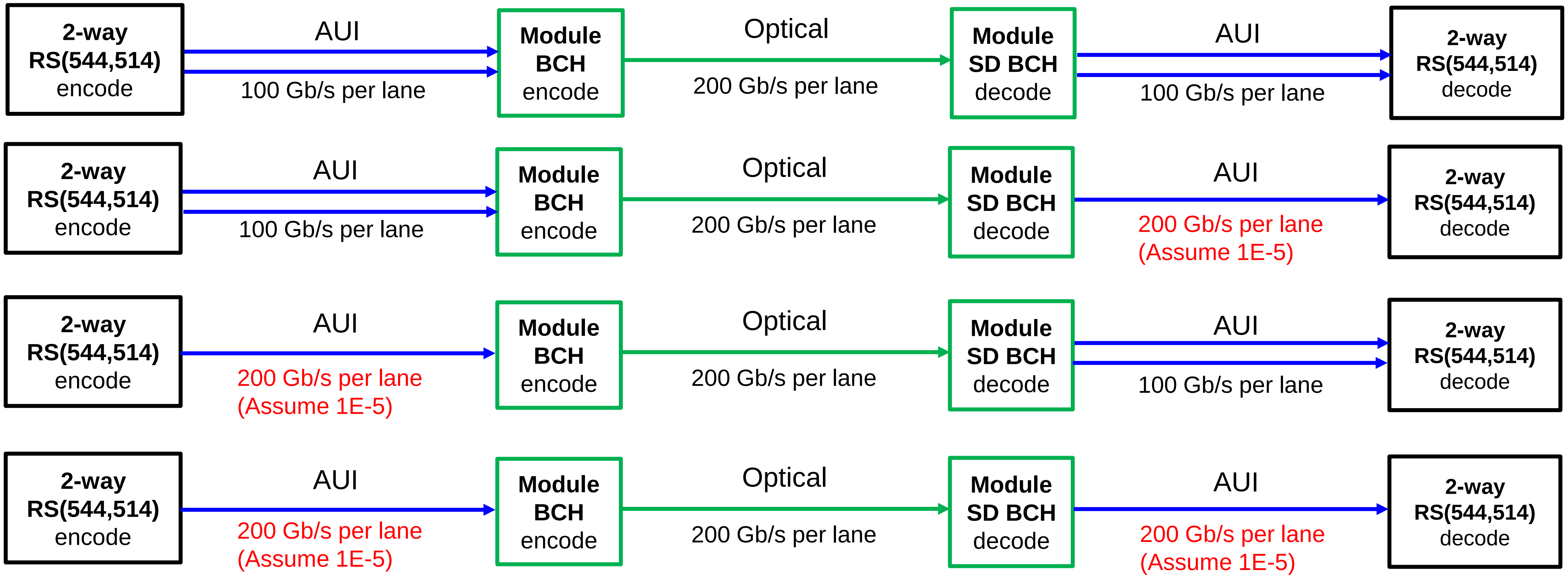
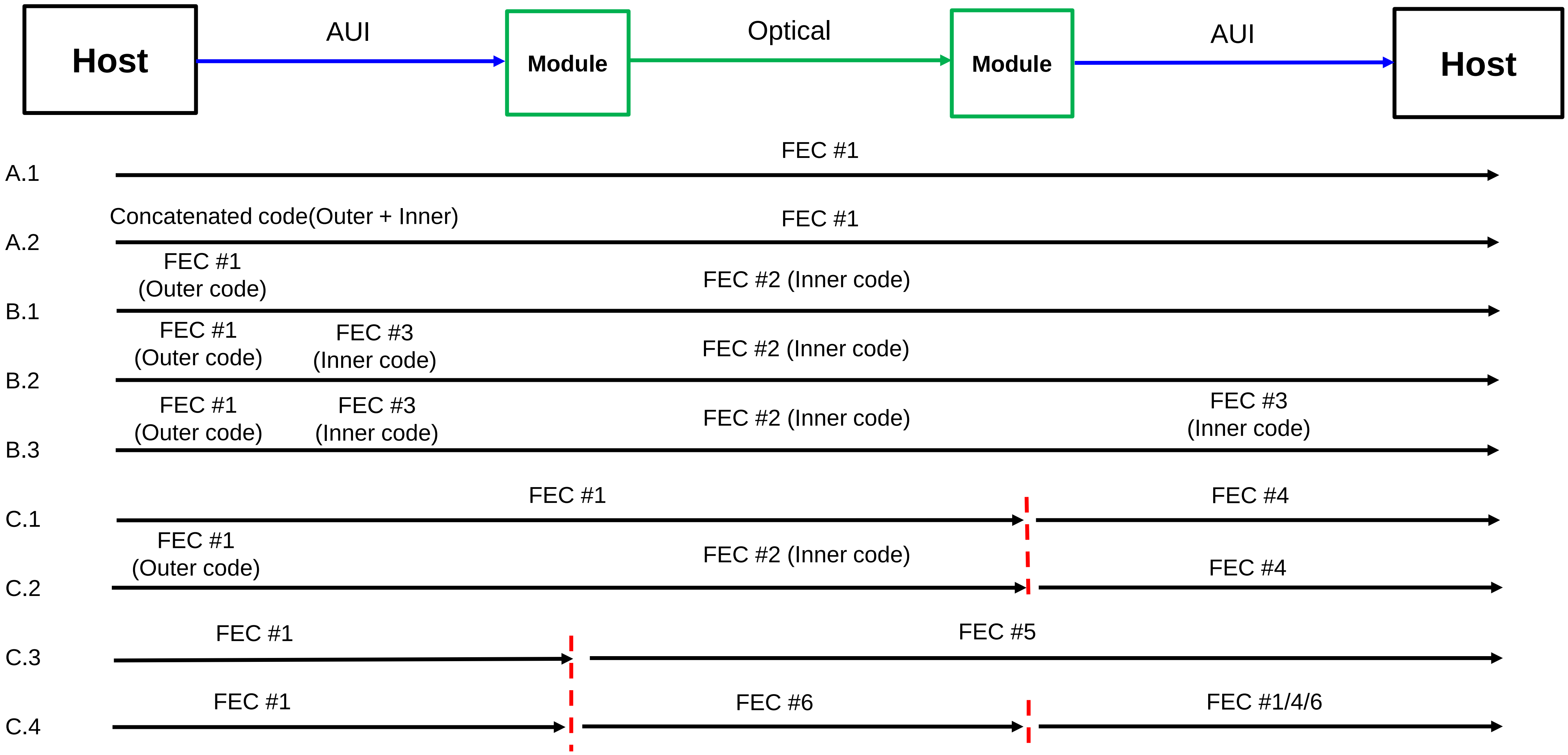
FEC Scheme Example with Concatenated FEC Code

- Assuming 200 Gb/s per lane AUI has similar BER (~1E-5) and error behavior as 100 Gb/s per lane AUI, it will make FEC scheme simple, just doubling the bit rate.
- Assuming 200 Gb/s per lane optical link operates at ~2E-3, the inner code can help to lower this raw BER to match the far end outer decode RS(544,514) performance.
  - This inner code has a short codeword, operating on a per-lane style to enable simple FEC scheme conversion.



FEC Scheme Evolution: Terminate and Regenerate between Different FEC Codes



- Selecting FEC #1 will be one of the key step for P802.3df architecture forward.

Summary:

- **FEC scheme relates to FEC code**
  - "Concatenated" is an academia terminology for FEC code, "Encapsulated" can be used for FEC scheme.
  - A well designed logic layer architecture can support different FEC schemes.
- **FEC code selection depends on the pre-FEC BER**
  - 200 Gb/s per lane AUI, feasibility of ~1E-5?
  - 200 Gb/s per lane IM-DD optical, feasibility of ~2E-3?
  - 800 Gb/s Coherent Lite? Feasibility of 4.5E-3 or ~2E-2?
  - 200 Gb/s per lane CR PHY?
- **To define a rough pre-FEC BER target of PMDs/AUI can help logic layer architecture work move forward.**
  - Shall we start from 2-way interleaved RS(544,514) as in 802.3bs/cu/ck?

Thank you