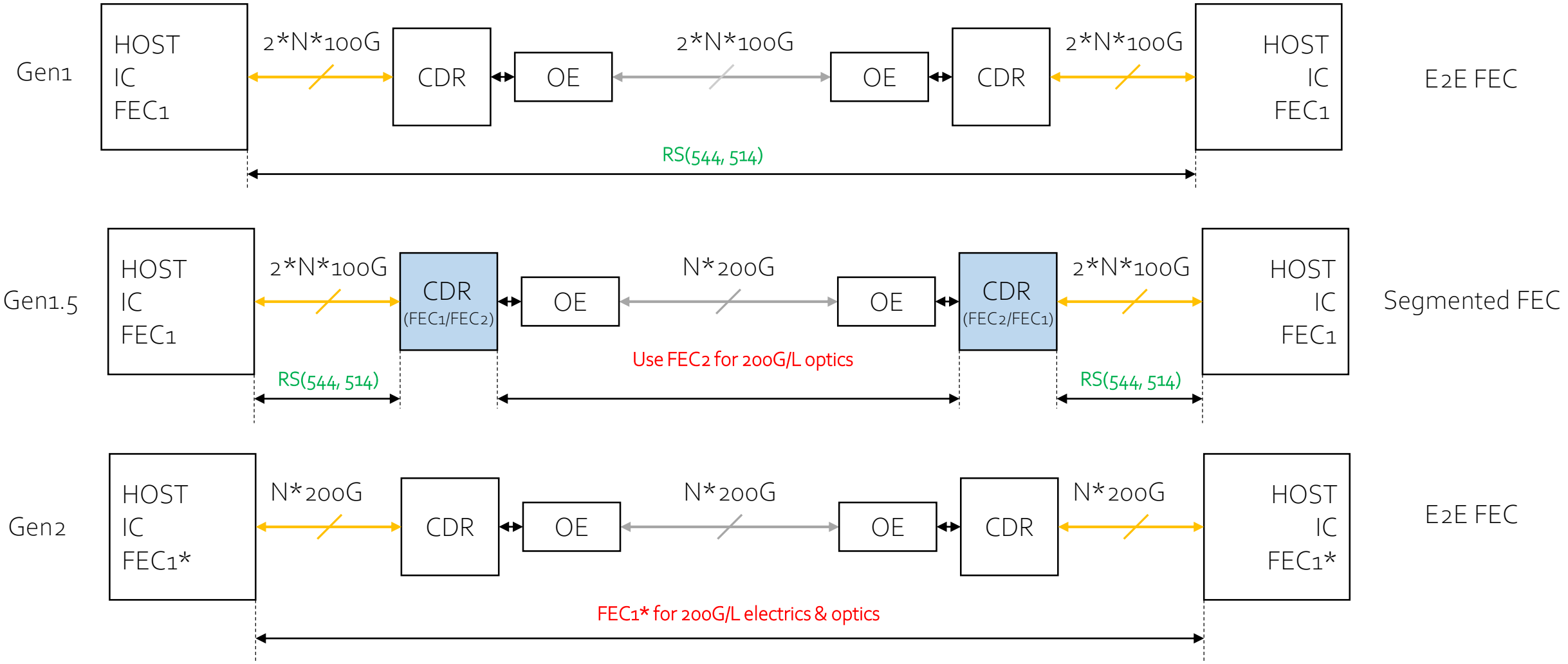
Further Consideration on FEC architecture for 800G and 1.6T

Leon Bruckman (Huawei), Yan Zhuangyan (Huawei)

Purpose

- Propose FEC architecture to support 100G/lane and 200G/lane 800GE PHYs applications and migration.
- Baseline proposal for 8*100G PCS

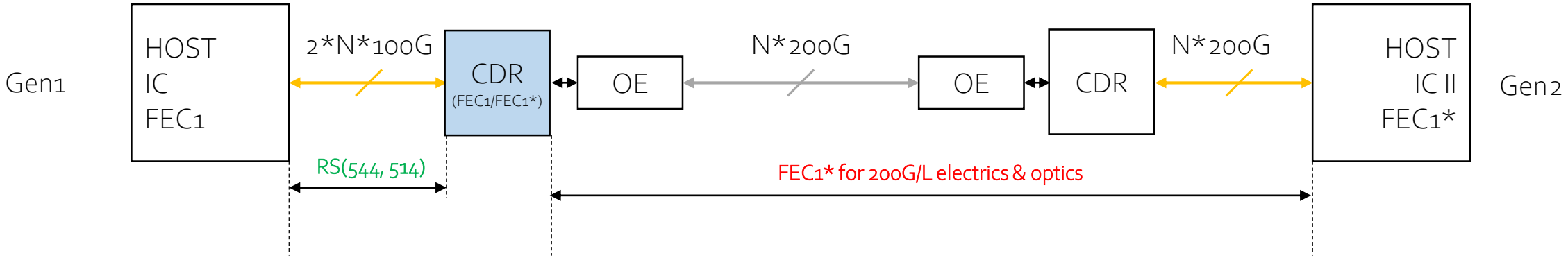
FEC architecture for generations of 800G/1.6T



- End-to-End FEC architecture is the best for Gen1 and Gen2 interconnects (performance discussion can refer to lu_3df_01b_220215.pdf).
- While for Gen1.5, a segmented FEC architecture with terminated FEC for 200G/L optics is preferred.
- FEC1* may be different from FEC1, and it may be the same as FEC2

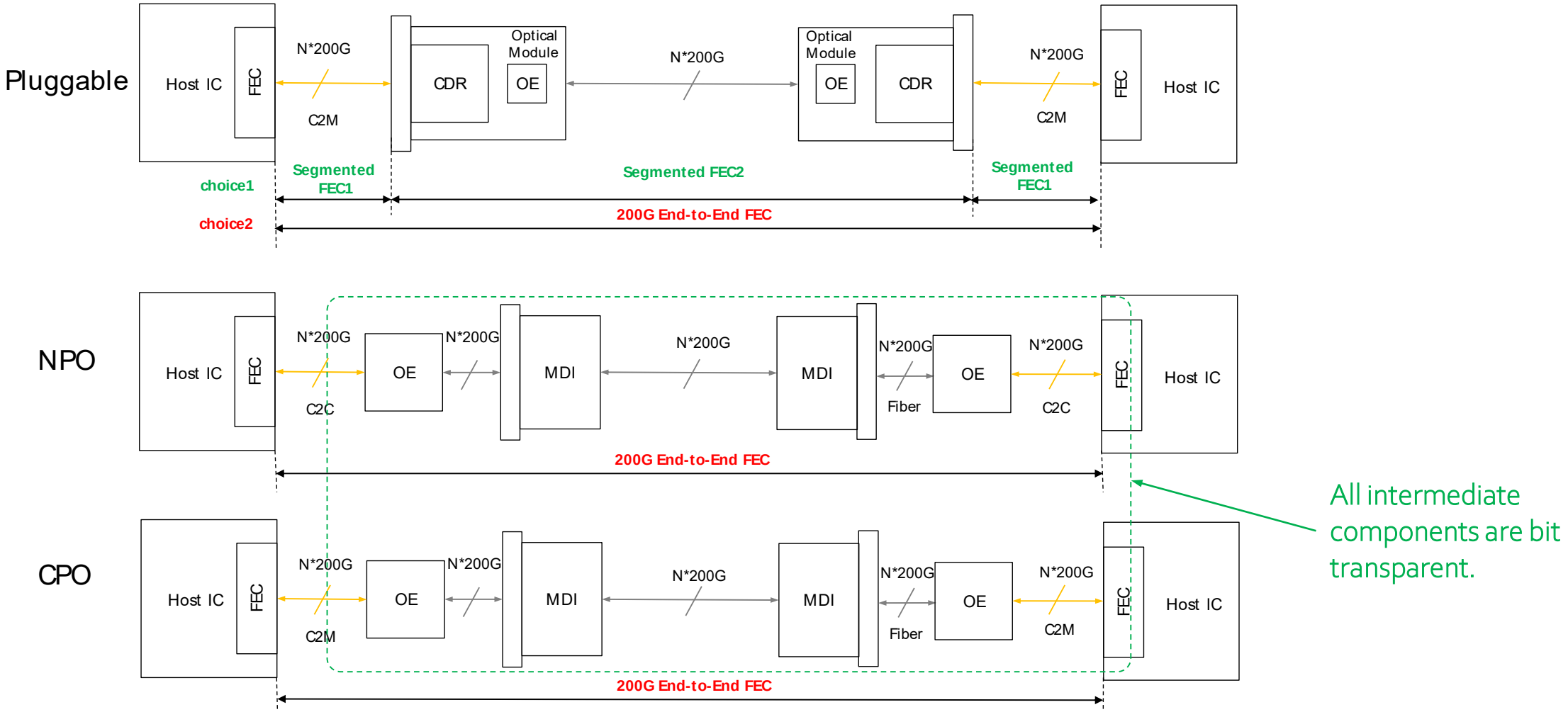
Ways to support Gen1.5 interconnecting Gen2

Choice#1: Gen1.5 CDR has to support FEC#2 (besides FEC#1).



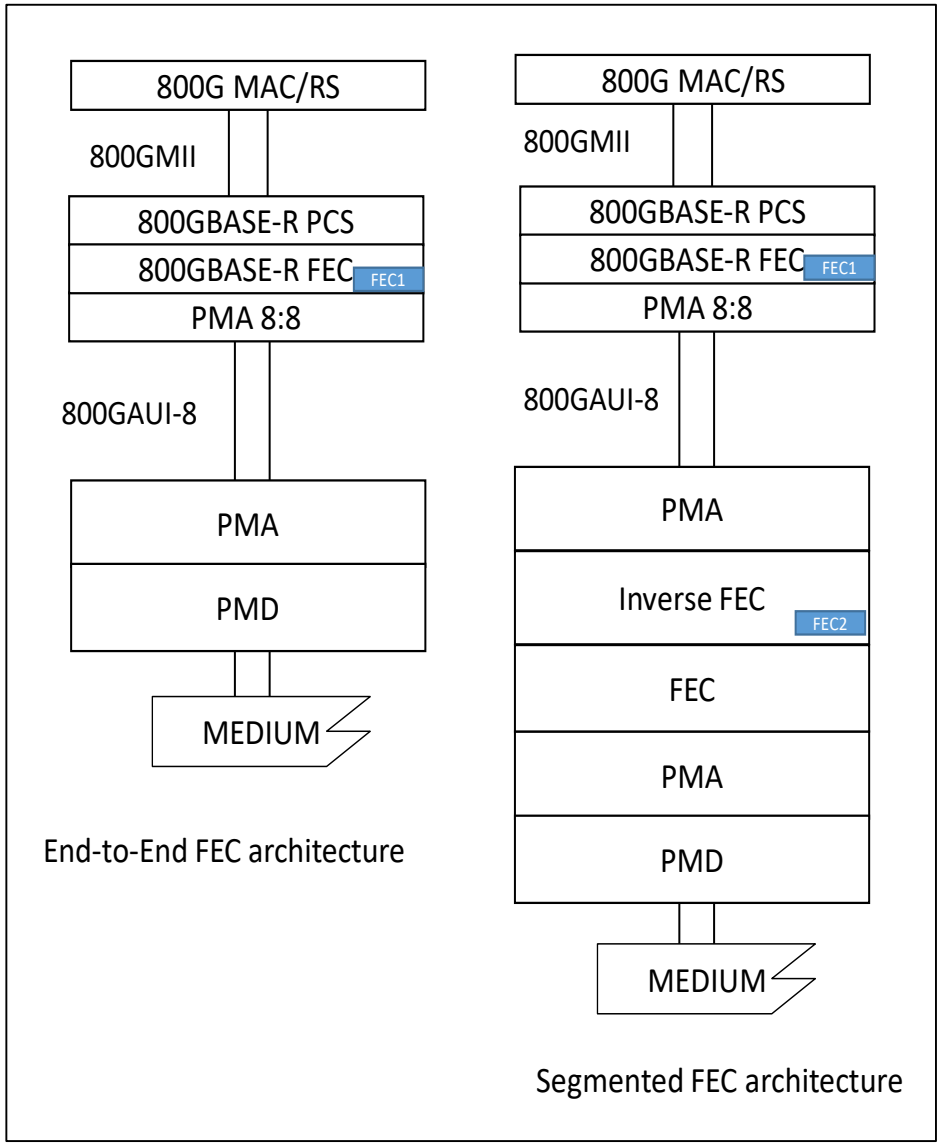
- Segmented FEC architecture can be used for interconnections between Gen1 and Gen2 PHYs.
- Assuming this is an interim solution during the 100G/lane to 200G/lane transition, use the simple and straight forward solution
  - Latency penalty more relevant in short reach applications – Are these the main target of Gen1.5 ?
  - Power penalty: Are DC operators planning to use Gen1.5 massively, or wait for Gen2 for massive deployment ?
- Provide "good enough" solution for Gen1.5 and concentrate effort on Gen1 and Gen2

Applications of 200G/L – CPO/NPO



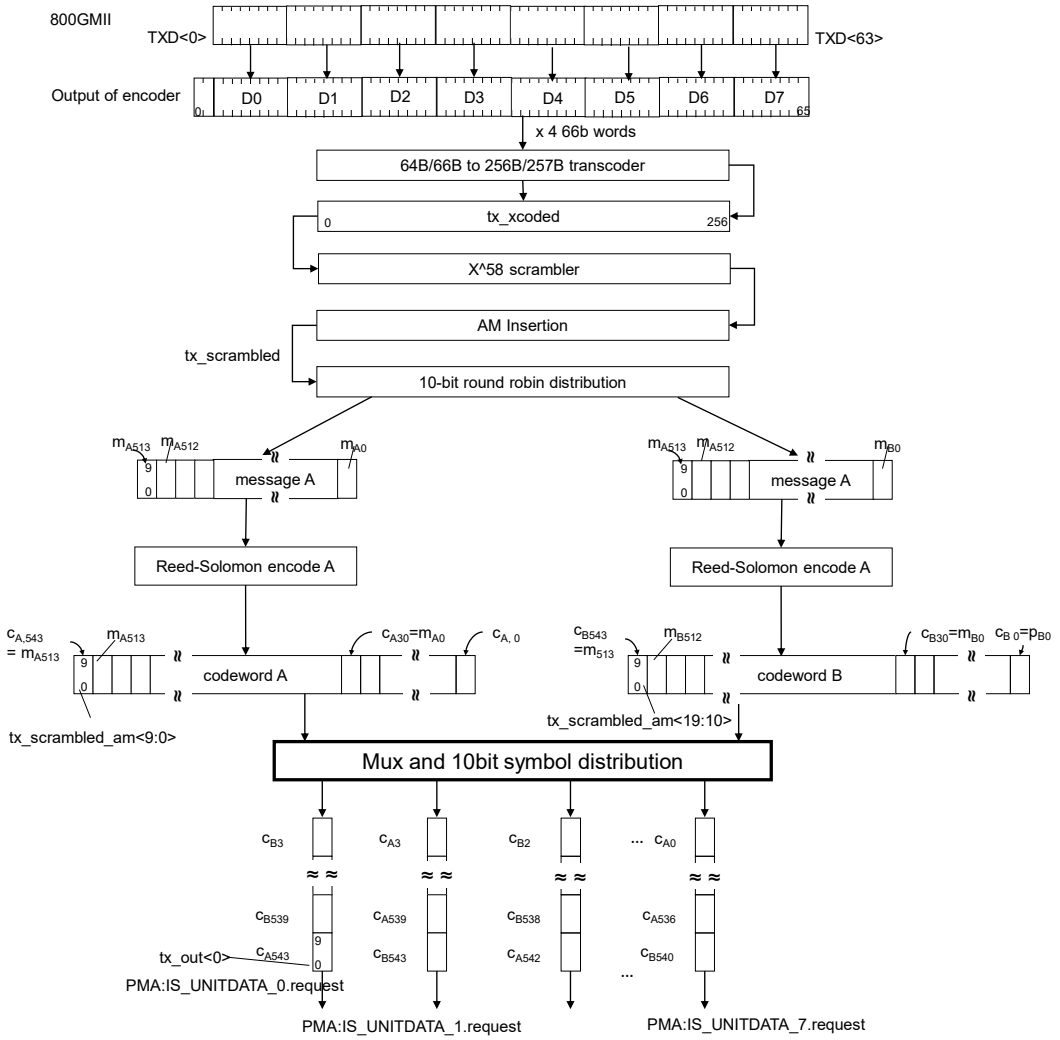
- The 200G/L end-to-end FEC architecture is more natural for pluggable, NPO and CPO applications.
- Does not compromise the CPO and NPO power saving advantage

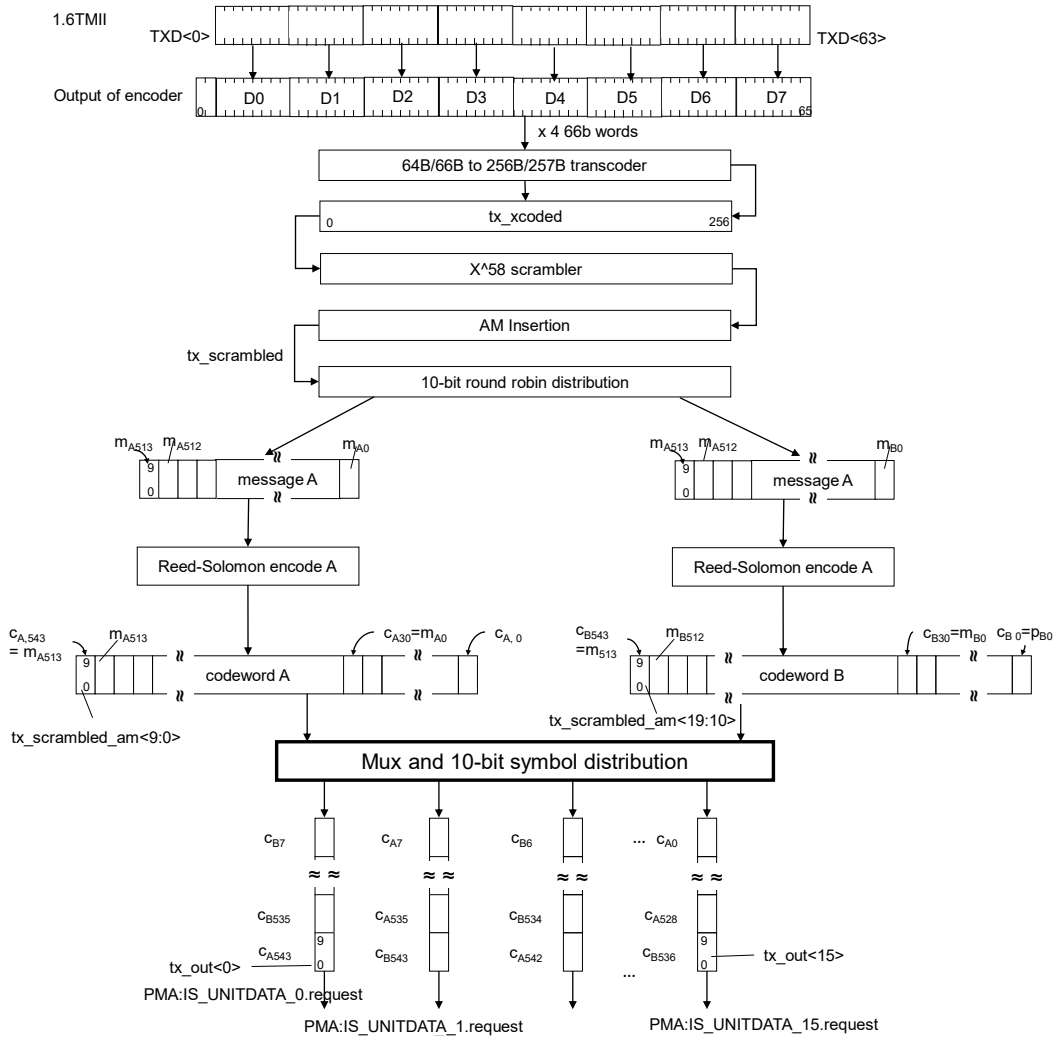
Architecture for 800GbE



- Gen1 and Gen2 can use End-to-End FEC architecture to support the 100G/L and 200G/L PHYs.
- While for Gen 1.5, if a stronger FEC is needed for 200G/L optics, the segmented FEC architecture can be used to provide a terminated FEC for difficult channels.

800GBASE-R and 1.6TBASE-R transmit bit distribution





- Reuse 200GBase-R and 400GBase-R bit distribution defined in Clause 119.
- 8 FEC lanes for 800G and 16 FEC lanes for 1.6T.

Baseline points for 8*100G/L (Gen1) and 1.6TbE PCS, FEC and PMA

- Reuse as much as possible the 200GbE/400GbE architectures in 802.3bs.
- Separate the PCS and FEC sublayers.
  - gustlin_3df_01_220118.pdf
- End to End FEC, possibly reusing RS(544, 514) and interleaving.
- Segmented (terminated) FEC for Gen1.5
- Increase lane rate to 106.25Gb/s.
  - Take advantage of 802.3ck work
- 8 FEC lanes for 800Gb/s and 16 FEC lanes for 1.6Tb/s.
- Reuse Clause 120 PMA – Small adaptations

Summary

- End-to-end FEC architecture is good for Gen1(100G/L), Gen2(200G/L) PHYs.
- Segmented FEC architecture recommended for Gen 1.5.
- As fast path to 800G early adopters, 100G/lane based 800GbE and 1.6TbE should be simple:
  - In general, reuse the 200G/400G architecture defined in 802.3bs with increased lane rate (106.25Gb/s).
  - 8 FEC lanes for 800Gb/s and 16 FEC lanes for 1.6TGb/s.
  - Investigate burst error performance
- Propose
  - Adopt 8*100G/16*100G PCS baseline as stated in this presentation.
  - Concentrate effort on end to end FEC for Gen1 and Gen2, and on segmented FEC for Gen1.5

Thanks!