Concatenated Code for 800 GbE & 1.6 TbE

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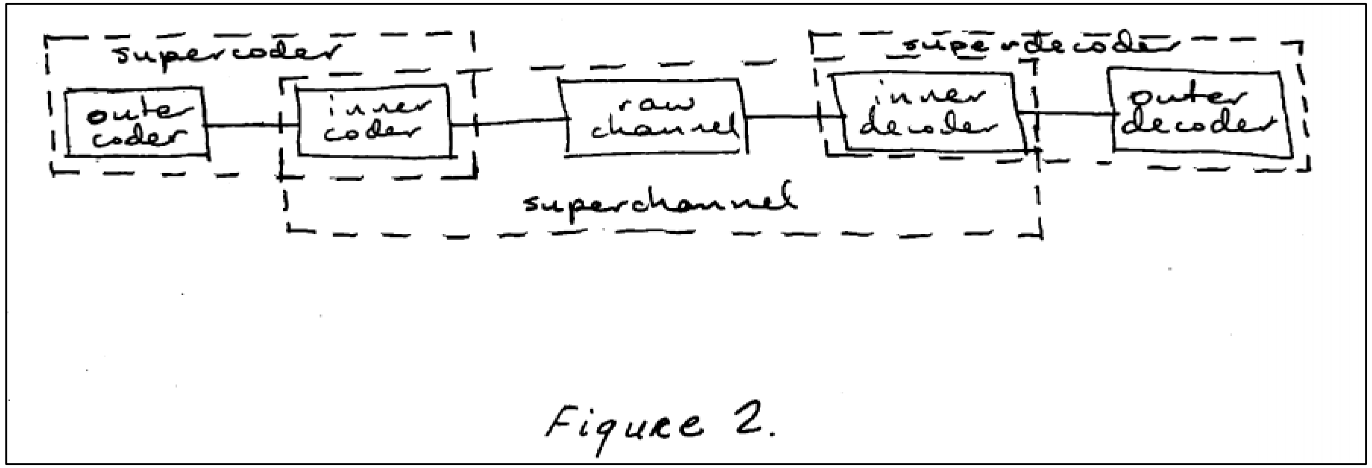
Concatenated Code Revisit

- **Concatenated code is a <u>FEC code</u> constructed with two or more codes.**
  - *"By concatenating codes, we can achieve very long codes, capable of being decoded by two decoders suited to much shorter codes"* [1].



  - Concatenated code could achieve similar coding gain as single FEC codes of the same overhead, but with much lower implementation complexity.
- **Concatenated code could be used in all FEC architectures/schemes 802.3df has discussed.**

[1] "Concatenated Codes", 1965, G. David Forney

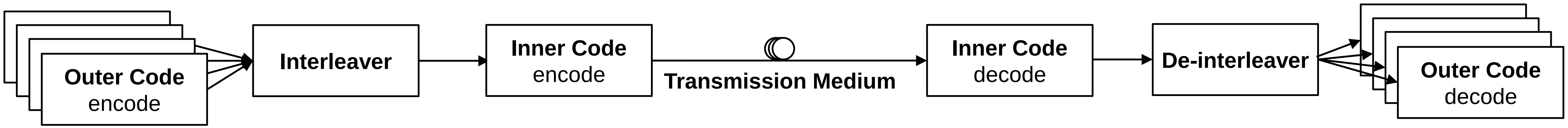
NCG of Concatenated Code vs NCG of Inner Code

- **Concatenated code is a FEC code, overall NCG is the only metric to evaluated its performance.**
  - Discussing the NCG of the inner code with different outer code configurations is not a reliable method to measure the effectiveness of a concatenated code.
  - Overall NCG of a concatenated FEC is affected by the code selection of the outer and inner codes, additional interleaver design, etc.
    - CFEC uses double extended eHamming(128,119) code as the inner code, with a convolutional interleaver, which brings ~1.4 dB of extra NCG comparing to its outer code at 1E-15 post-FEC BER.
    - BCH(144,136) as a inner code could contribute ~1.7dB of NCG to the outer 2-way interleaved RS(544,514).
    - However, eHamming(128,119) is a stronger code than BCH(144,136) due to higher overhead.

Outer Code	Outer Code NCG @1E-15	Inner Code	Overall NCG @1E-15	NCG improvement by inner code
(512x510) Staircase	9.38 dB	eHamming(128,119)	10.78 dB	1.4 dB
2-way RS(544,514)	6.95 dB	BCH(144,136)	8.6 dB	1.65 dB

Constructing a Concatenated Code

- **Component codes of concatenated code can be well-studied codes such as RS and BCH/Hamming.**
  - ITU-T has standardized various concatenated codes in G.975.1.
    - RS(255,239) + CSOC, BCH(3860,3824) + BCH(2040,1930), RS(1023,1007) + BCH(2047,1952), ...
  - Interleaver is typically used between the outer and inner codes for the codes above to randomize clustered errors due to uncorrectable errors left by the inner code.
  - Deep interleaver means additional power and latency.

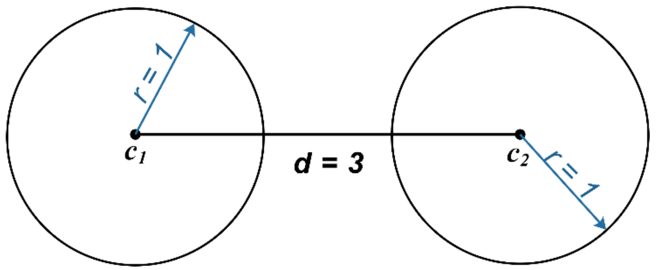


Simplified Diagram of ITU-T Standardized Concatenated Codes

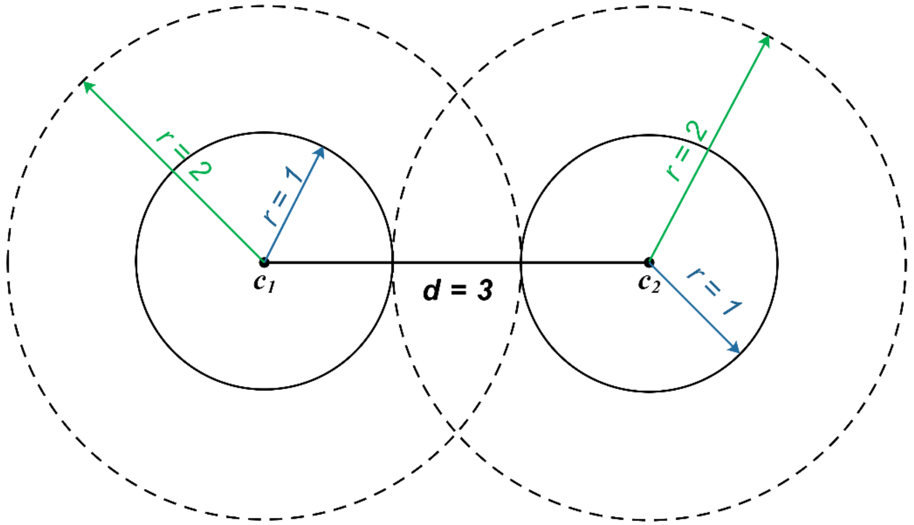
- **The RS + BCH concatenated code in this contribution has the same basic concept.**
  - The outer RS FEC has a 2-way codeword interleaver, and interleaved data is distributed into BCH encoder.
  - The inner BCH has relatively short codeword length to minimizing the effect of error clustering upon false-decoding.

Introduction to Hard-Decision and Soft-Decision Decoding

- Hard-decision decoding is well known by the group.
  - HD decoder can correct $\left\lfloor \frac{d-1}{2} \right\rfloor$ errors.
- Soft-decision decoding is a decoding technique based on generic hard-decision decoders.
  - SD and HD decoders share the same encoder.
- SD decoding could improve the net coding gain (NCG) theoretically by 3 dB comparing to HD decoding[2].
  - Usually with significant cost in chip area and power especially for some complex codes like RS.
  - SD could correct up to (d-1) errors.
  - Shorter binary codes could benefit from SD decoding with affordable cost.
- NCG improvement of SD decoding over HD should be evaluated on the same code.



HD decoding of a Hamming code with d = 3

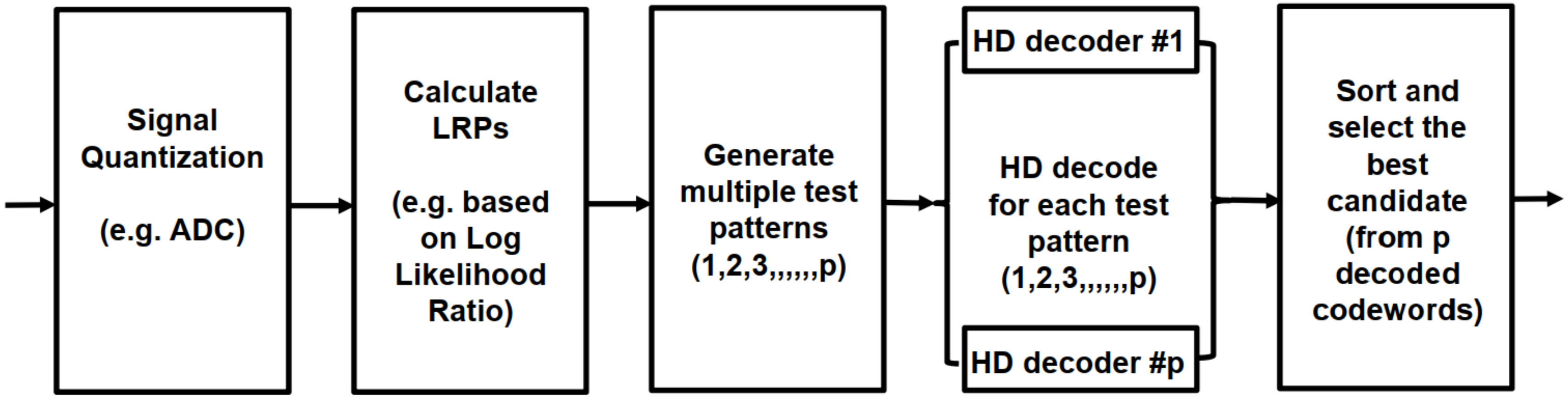


SD decoding of a Hamming code with d = 3

[2]. "Error Control Coding (Second Edition)", 0-13-0042672-5, 2004, by Shu Lin & Daniel Costello Jr.

Implementation Example of Soft-Decision Decoding

- Chase-2 decoding[3] algorithm is an efficient soft input hard output (SIHO) decoder that tries out a number of most likely error patterns, generated based on a number of least reliability positions (LRP).



- For example, we can select all combinations up to 3 bits within the 6 LRPs, flipping them to generate 42 test patterns (candidate codewords).
  - Decode each of these 42 candidates and find the one with highest probability to be correct.

[3]. "A class of algorithms for decoding block codes with channel measurement information", D. Chase, IEEE Transactions on Information Theory, 1972 Vol.18

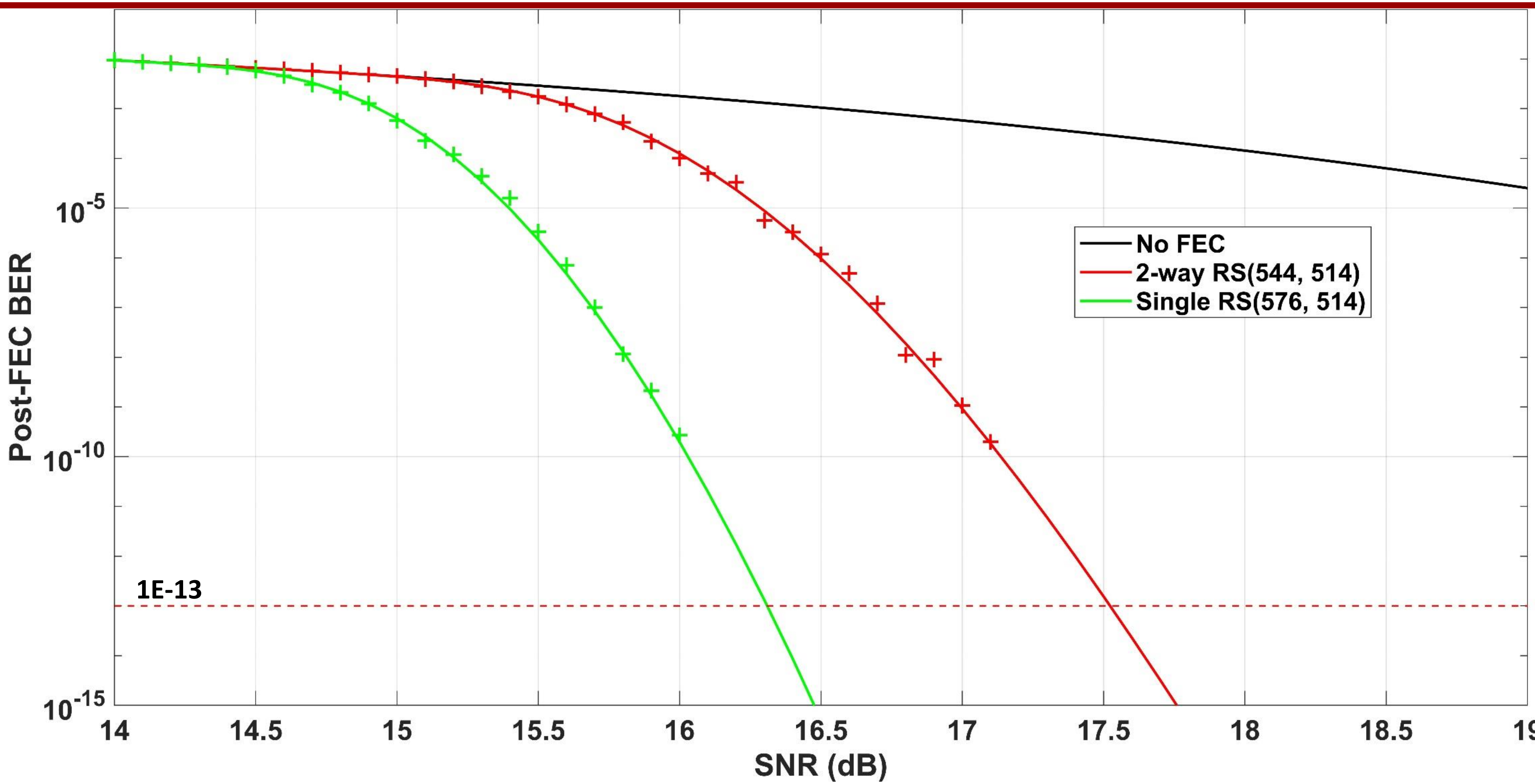
More Information of Concatenated Code for Ethernet

FEC code			Operating rate	Latency[1], *ns*	Relative Area
Outer Code	Hard Decision RS	2-way RS(544,514)	850G	51.2	~4.00
		2-way RS(544,514)	212.5G	89.6	1.00 (Synthesized, 7nm)
Inner Code	Hard Decision BCH/Hamming	BCH(144,136)	225G	1.6	0.003
		eBCH(76,68)	~240G[3]	1.6	0.002
	Soft Decision BCH/Hamming (LRP = 6)[2]	BCH(144,136)	225G	9.6	0.17
		eBCH(76,68)	~240G[3]	9.6	0.11

1: Latency is evaluated based on 1.25 GHz clock frequency (0.8 ns per cycle).
2: Latency and/or area will go higher along with the performance if more LRP is selected.
3: Extra overhead is considered for single carrier 800Gb/s coherent transceivers.

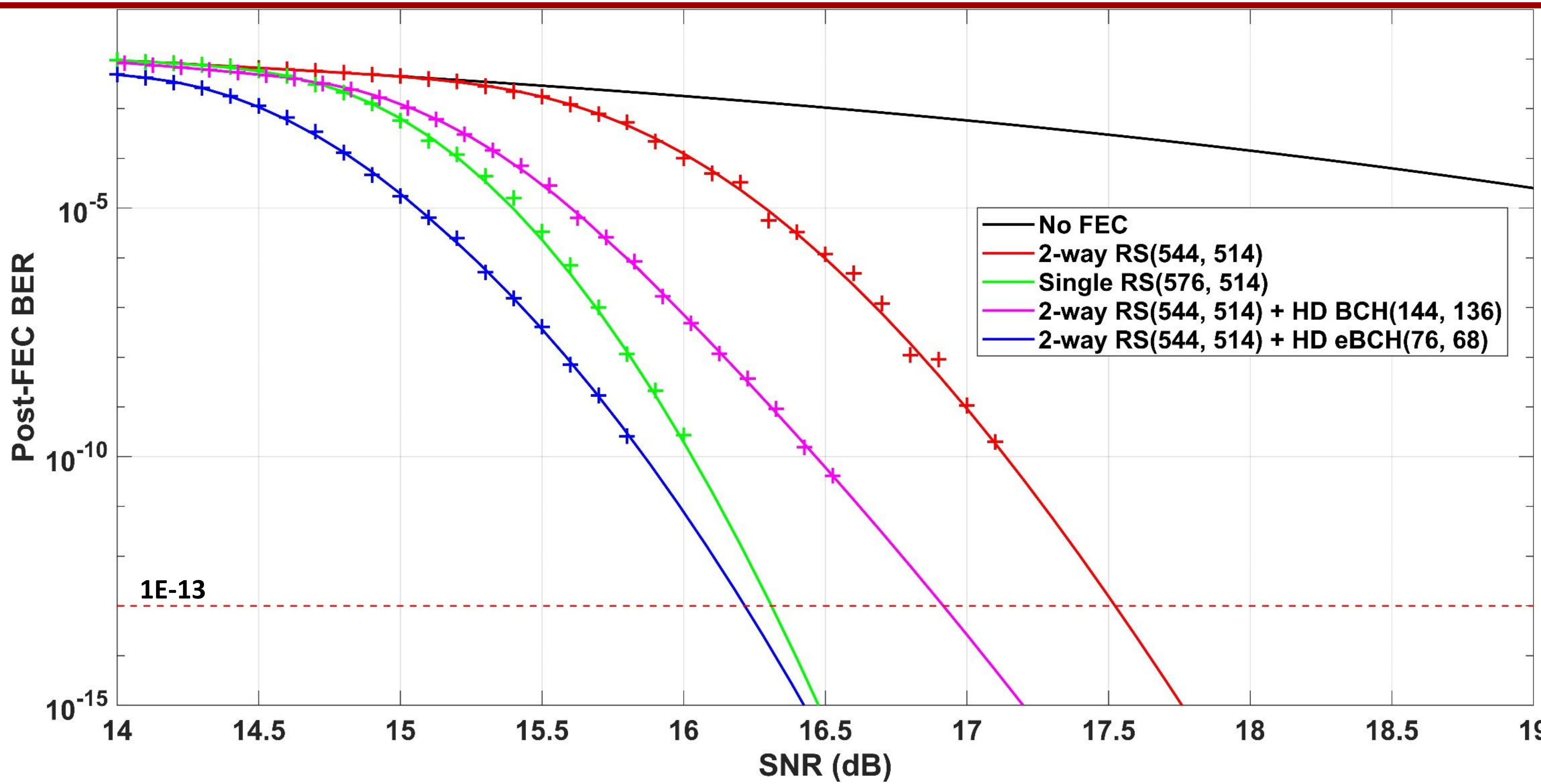
- Latency and area cost of various inner codes are evaluated.
- Power consumption evaluation is in progress.
  - SD BCH(144,136) at 225 Gb/s throughput is estimated to take ~90mW when using 6 LRPs and 42 test patterns.

Performance of HD RS FEC



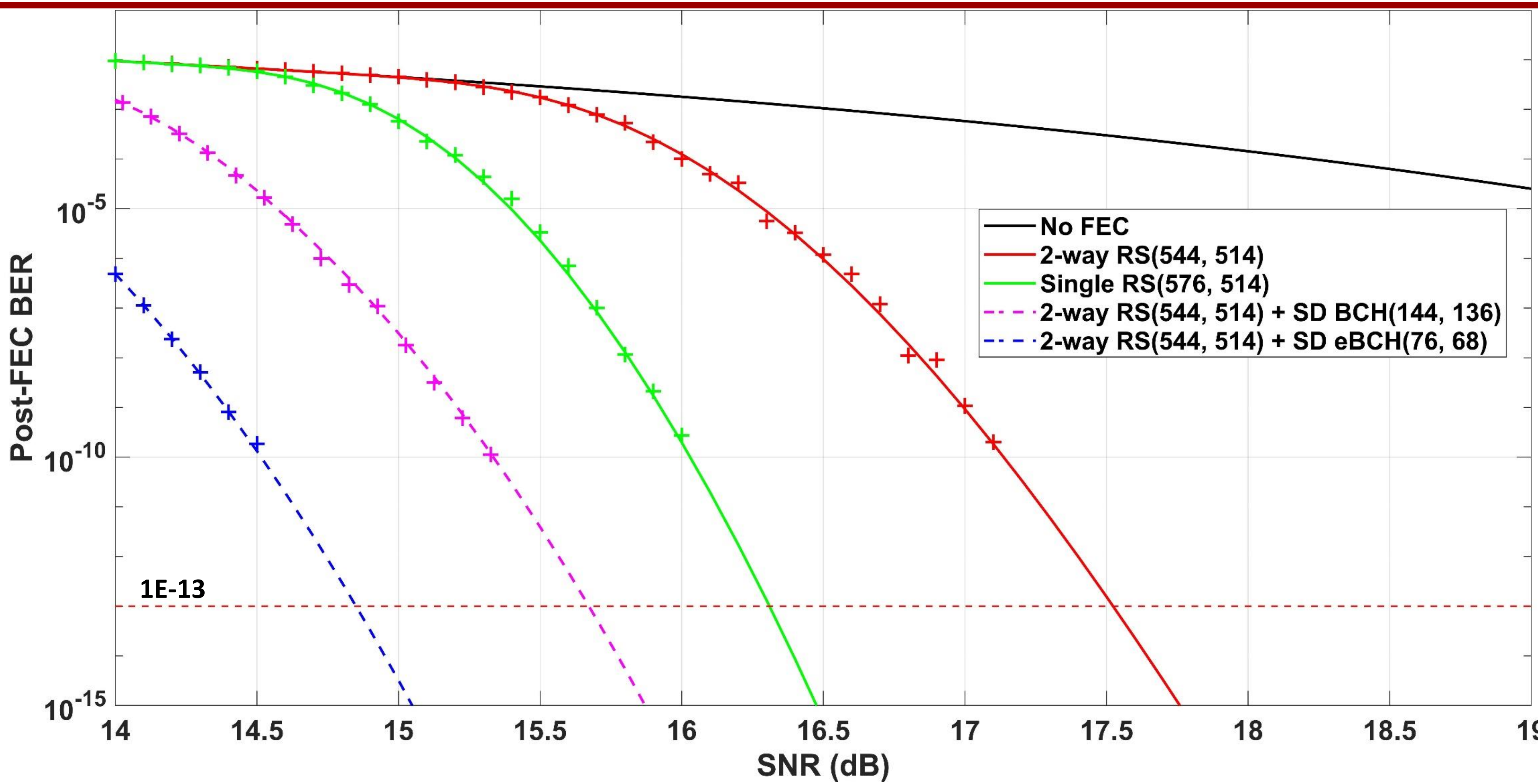
FEC Code	Pre-FEC BER	AUI BER	Post-FEC BER	NCG (dB)	FEC Latency	Inner Code Rate	AUI Rate	Optical Rate
2-way RS(544,514)	2.89E-4	1E-5	1E-13	6.50	51.2 ns	--	8x106.25 Gb/s or 4x212.5 Gb/s	4x212.5 Gb/s
Single RS(576,514)	1.29E-3			7.46	70.4 ns		8x112.5 Gb/s or 4x225 Gb/s	4x225 Gb/s

Performance of Concatenated FEC with Inner HD Decoding



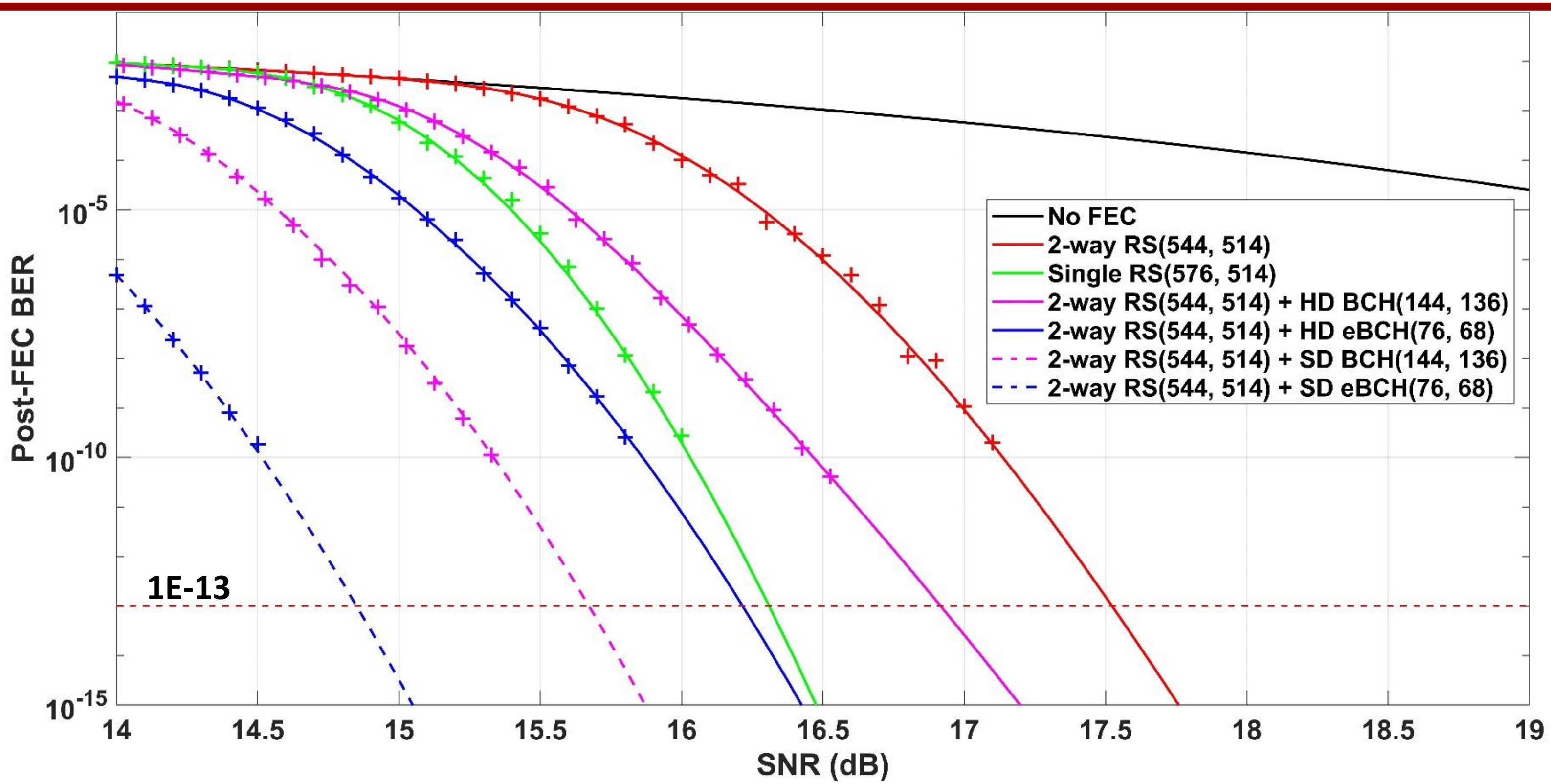
FEC Code	Pre-FEC BER	AUI BER	Post-FEC BER	NCG (dB)	FEC Latency	Inner Code Rate	AUI Rate	Optical Rate
2-way RS(544,514) + HD BCH(144,136)	6.60E-4	1E-5	1E-13	6.86	52.8 ns	18/17	8x106.25 Gb/s or 4x212.5 Gb/s	4x225 Gb/s
2-way RS(544,514) + HD eBCH(76,68)	1.43E-3			7.33	52.8 ns	19/17		4x237.5 Gb/s or 1x950 Gb/s

Performance of Concatenated FEC with Inner SD Decoding



FEC Code	Pre-FEC BER	AUI BER	Post-FEC BER	NCG (dB)	FEC Latency	Inner Code Rate	AUI Rate	Optical Rate
2-way RS(544,514) + SD BCH(144,136)	2.47E-3	1E-5	1E-13	8.11	60.8 ns	18/17	8x106.25 Gb/s or 4x212.5 Gb/s	4x225 Gb/s
2-way RS(544,514) + SD eBCH(76,68)	5.04E-3			8.69	60.8 ns	19/17		4x237.5 Gb/s or 1x950 Gb/s

Performance Comparison



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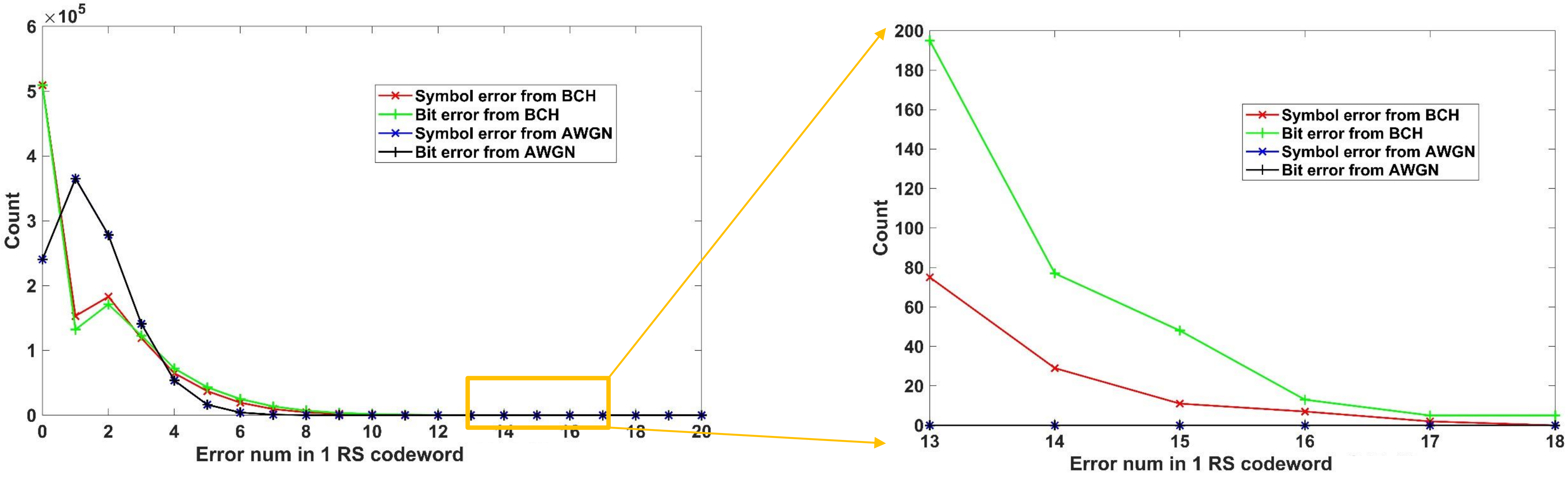
Mathematical Analysis of Concatenated FEC

- **Error pattern comes out of the inner code decoder will not be statistically random.**
  - Each false decoded inner code will exhibit concentrated error patterns to the outer codeword.



Error distribution analysis of uncorrectable codewords from inner code

  - Simulation is one way to prove the feasibility but theoretical analysis will be more convincing.
  - More theoretical analysis is underway to evaluate the performance in a mathematical way.

Summary

- **Concatenated code is analyzed to contribute to 802.3df architecture discussions.**
  - AUI can be kept at the same rate as RS(544,514) overhead.
  - For a given code and pre-FEC BER, soft-decision decoding could improve the net coding gain.

Thank you