

224G PAM4 CR+/CR Channel COM Analysis

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Intel

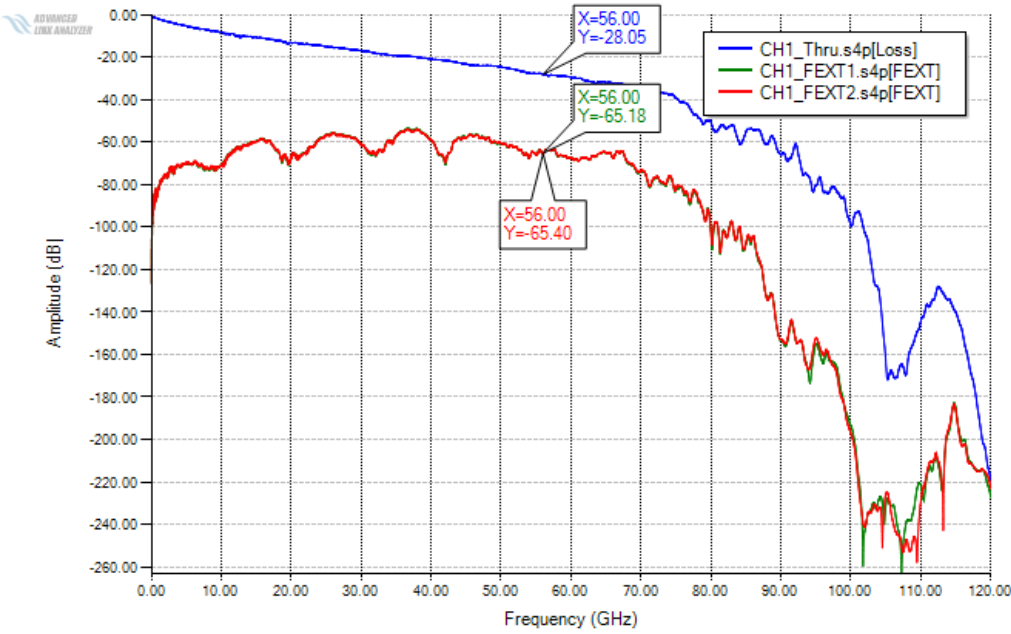
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OUTLINE

- **802.3df CR+/CR-PAM4 Channel Characteristics**
- **802.3df CR+/CR-PAM4 COM Assumptions/Models/Parameters**
- **802.3df CR+/CR-PAM4 COM Configurations**
- **802.3df CR+/CR-PAM4 COM Analysis Results**
- **Summary and Next Steps**

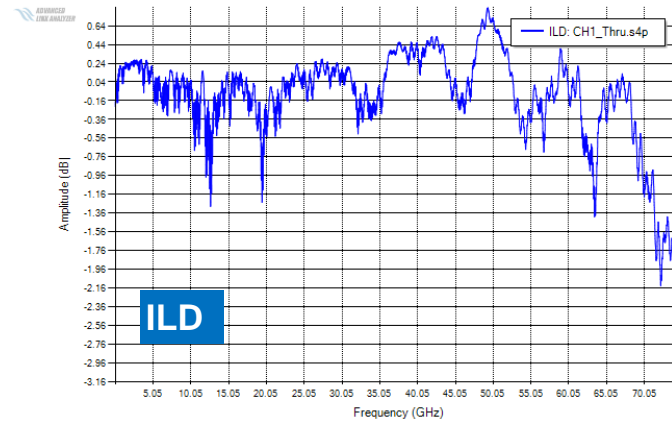
Case A: 224 Gbps-PAM4 CR+ Channel Characteristics

Channel Viewer: [29] FR: Sdd21

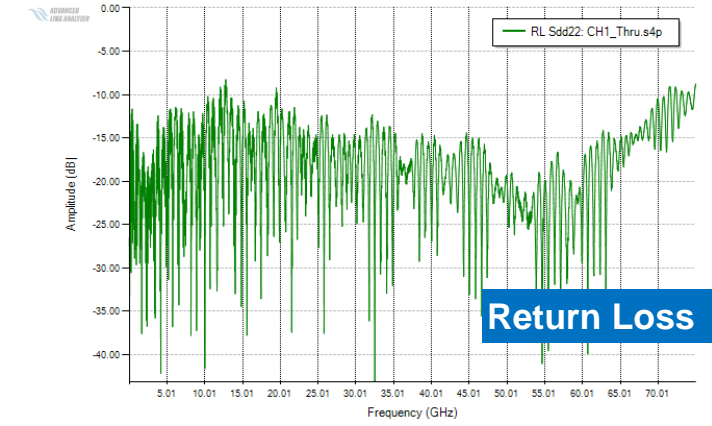


- IL: 28.05dB @ 56GHz
- ILD \approx 1dB (<56GHz)
- RL \approx 10dB (<56GHz)
- FEXT < 54dB (<56GHz)

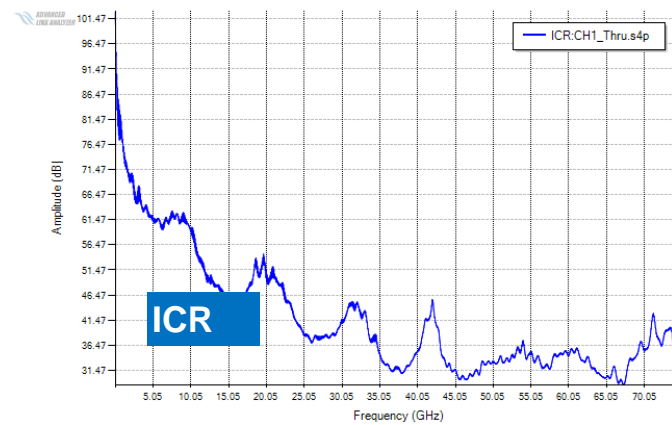
Channel Viewer: [8] CP: ILD



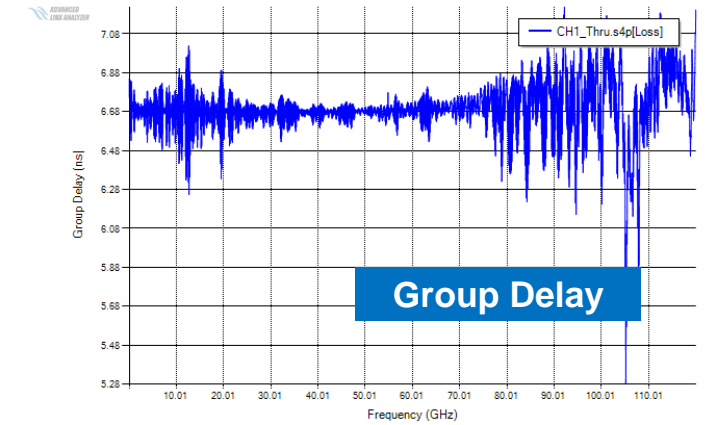
Channel Viewer: [9] CP: Return Loss



Channel Viewer: [10] CP: ICR



Channel Viewer: [27] FR: Sdd21



See: [li_3df_01_220322.pdf](#)

Case A: 224 Gbps-PAM4 CR+ COM

Assumptions/Models/Parameters

- Summary
 - TX/RX die model: 3-segment LC model based on Intel 224Gbps PAM4 TC*
 - TX/RX package model: 2-segment TL model based on Intel test package & technology roadmap*
 - TX characteristics
 - Output amplitude ($A_v/A_{fe}/A_{ne}$): 0.51625/0.51625/0.608 (increased ~25% from 100GBASE-CR1)
 - Rise/Fall Time (T_R): $0.31875 \cdot UI$ (~2.85ps @ 112Gbd, 3ps @106.25Gbd)
 - Jitter/Noise/Nonlinearity
 - A_{DD} , σ_{RJ} , $SNRTX$, RLM : Same as 100GBASE-CR1
 - EQ
 - 8 taps FIR: 6 pre-taps and 1 post-tap
 - RX characteristics
 - Noise filter BW (f_r): $0.5 \cdot \text{Baud Rate}$
 - Noise: η_0 (TBD)
 - EQ: CTLE (scaled from 100GBASE-CR1), DFE (TBD)
 - DER: 10^{-4} (Same as 100GBASE-CR1)

Note: *: See [mli_3df_02a_220316](#)

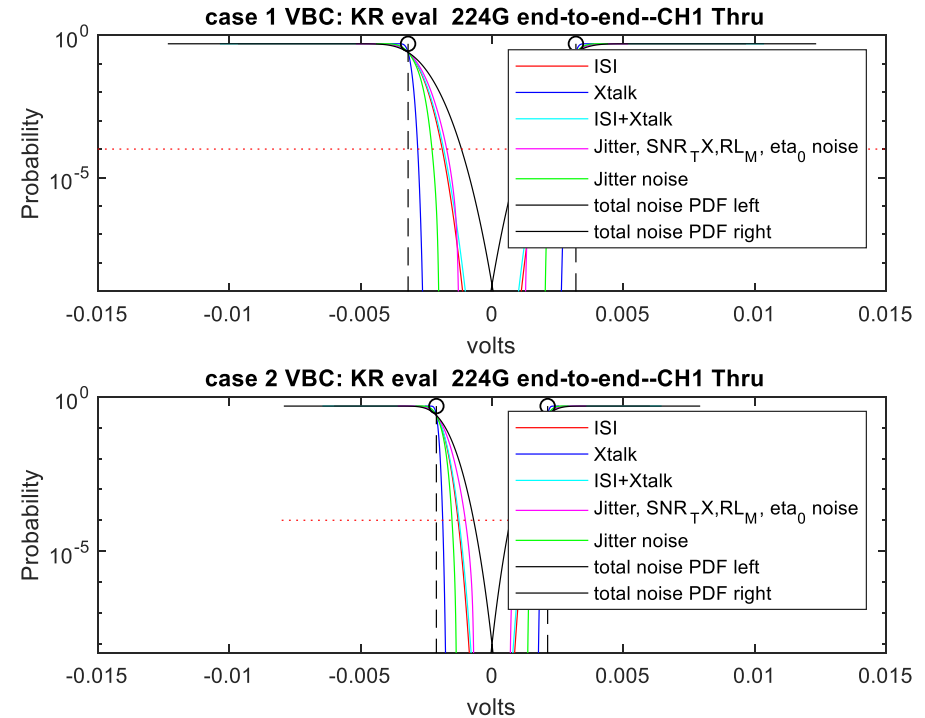
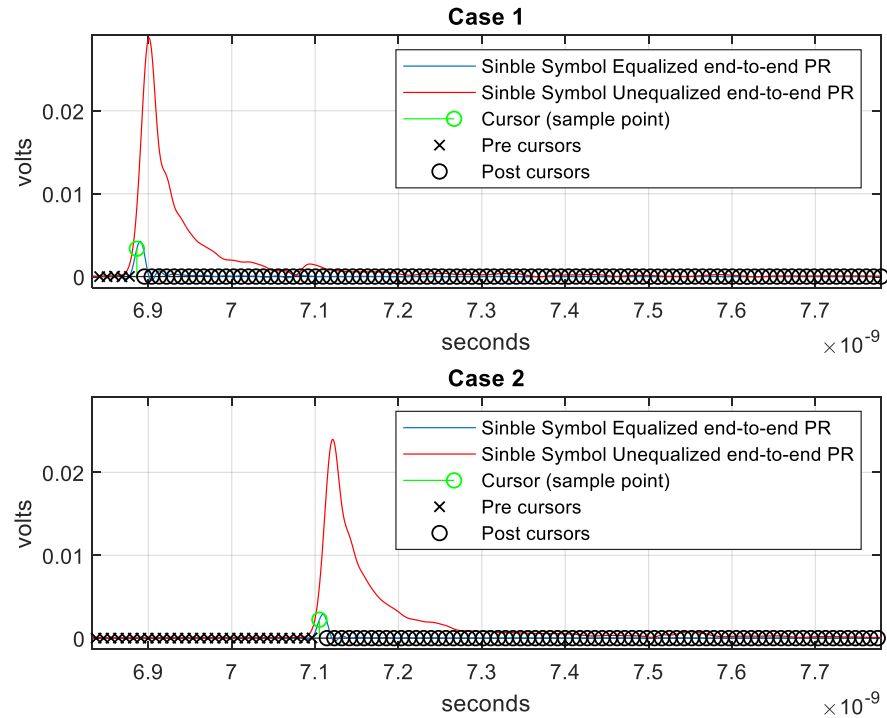
Case A: 224 Gbps-PAM4 CR+ COM Configuration

Table 93A-1 parameters				I/O control			Table 93A-3 parameters		
Parameter	Setting	Units	Information				Parameter	Setting	Units
f_b	112	GBd		DIAGNOSTICS	1	logical	package_tl_gamma0_a1_a2	[0 0.00089 0.000155]	
f_min	0.05	GHz		DISPLAY_WINDOW	1	logical	package_tl_tau	0.006141	ns/mm
Delta_f	0.01	GHz		CSV_REPORT	1	logical	package_z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
C_d	[0.4e-4 0.4e-4; 0.9e-4, 0.9e-4; 1.1e-4, 1.1e-4]	nF	[TX RX]	RESULT_DIR	\\results\CEI200LR_{date}\		Table 92-12 parameters		
L_s	[0.13, 0.13; 0.15, 0.15; 0.14, 0.14]	nH	[TX RX]	SAVE_FIGURES	0	logical	Parameter	Setting	
C_b	[0.3e-4, 0.3e-4]	nF	[TX RX]	Port Order	[1 3 2 4]		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
z_p select	[1 2]		[test cases to run]	RUNTAG	LR_eval_		board_tl_tau	5.790E-03	ns/mm
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]	COM_CONTRIBUTION	0	logical	board_z_c	100	Ohm
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]	Operational			z_bp (TX)	110.3	mm
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]	COM Pass threshold	3	dB	z_bp (NEXT)	110.3	mm
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]	ERL Pass threshold	8	dB	z_bp (FEXT)	110.3	mm
C_p	[0.4e-4 0.4e-4]	nF	[TX RX]	DER_0	0.0001		z_bp (RX)	110.3	mm
R_0	50	Ohm		T_r	0.002845982	ns	C_0	[0.29e-4]	nF
R_d	[50 50]	Ohm	[TX RX]	FORCE_TR	1	logical	C_1	[0.19e-4]	nF
A_v	0.51625	V		Local Search	2		Include PCB		
A_fe	0.51625	V		BREAD_CRUMBS	1	logical	0	logical	
A_ne	0.608	V		SAVE_CONFIGZMAT	1	logical	Floating Tap Control		
AC_CM_RMS	0	V	[test cases]	PLOT_CM	0		N_bg	TBD	0 1 2 or 3 groups
L	4			TDR and ERL options			N_bf	TBD	taps per group
M	32			TDR	1	logical	N_f	TBD	UI span for floating taps
filter and Eq				ERL	1	logical	bmaxg	TBD	max DFE value for floating taps
f_r	0.5	*fb		ERL_ONLY	0	logical	B_float_RSS_MAX	TBD	rss tail tap limit
c(0)	0.5		min	TR_TDR	0.01	ns	N_tail_start	TBD	(UI) start of tail taps limit
c(-1)	[-0.4:0.02:0]		[min:step:max]	N	3500		ICN & FOM_ILD parameters		
c(-2)	[0:0.02:0.2]		[min:step:max]	beta_x	0		f_v	0.742	*Fb
c(-3)	[-0.1:0.02: 0.1]		[min:step:max]	rho_x	0.618		f_f	0.742	*Fb
c(-4)	[-0.1:0.02: 0.1]		[min:step:max]	fixture delay time	[0 0]	[port1 port2]	f_n	0.742	*Fb
c(-5)	[-0.1:0.02: 0.1]		[min:step:max]	TDR_W_TXPKG	0		f_2	80.000	GHz
c(-6)	[-0.1:0.02: 0.1]		[min:step:max]	N_bx	21	UI	A_ft	0.600	V
c(1)	[-0.2:0.02:0]		[min:step:max]	Tukey_Window	1	logical	A_nt	0.600	V
N_b	TBD	UI		Noise, jitter			Receiver testing		
b_max(1)	TBD			sigma_RJ	0.01	UI	RX_CALIBRATION	0	logical
b_max(2..N_b)	TBD			A_DD	0.02	UI	Sigma BBN step	5.00E-03	V
b_min(1)	TBD			eta_0	TBD	V^2/GHz			
b_min(2..N_b)	TBD			SNR_TX	33	dB			
g_DC	[-20:1:0]	dB	[min:step:max]	R_LM	0.95				
f_z	44.8	GHz							
f_p1	44.8	GHz							
f_p2	112	GHz							
g_DC_HP	[-6:1:0]		[min:step:max]						
f_HP_PZ	0.7	GHz							

Notable changes from 100GBASE-CR1

See [mli_3df_02a_220316](#) for die and PKG parameters

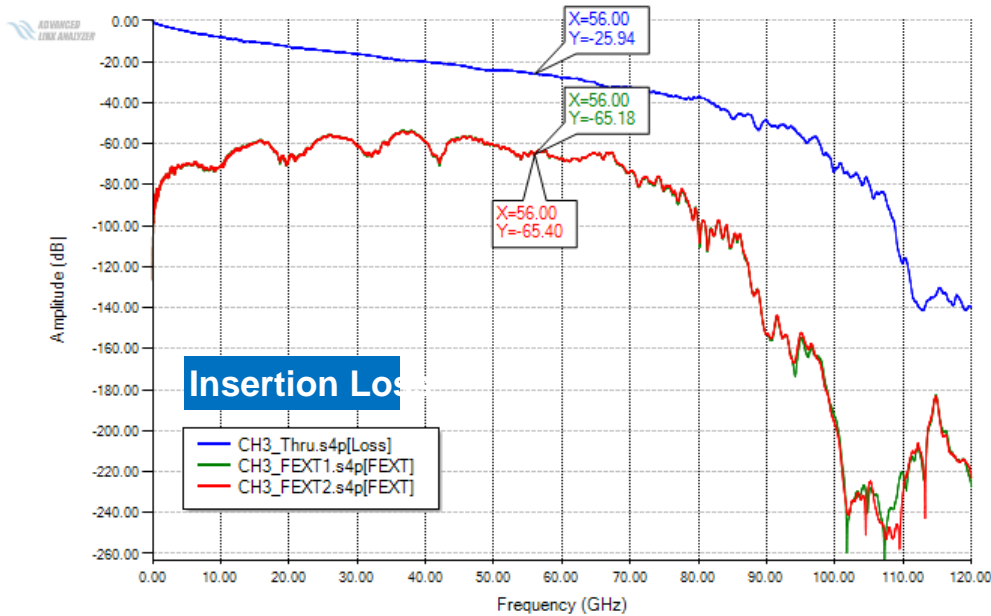
Case A: 224 Gbps-PAM4 CR+ COM Analysis Results



- COM = 3.517dB w/ [12, 12]mm pkg (Case 1), 3.049dB w/ [31, 29]mm pkg (Case 2)

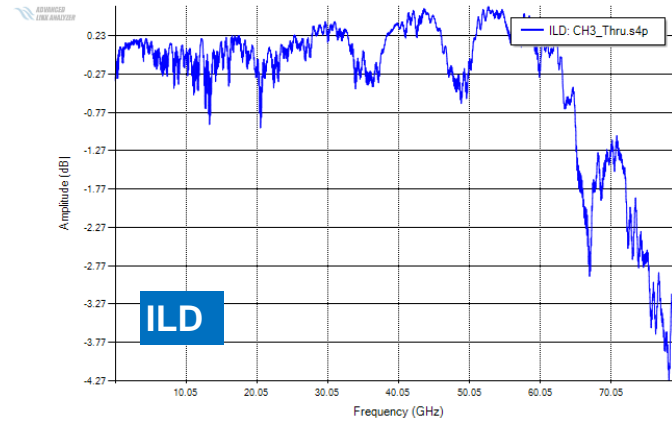
Case B: 224 Gbps-PAM4 CR Channel Characteristics

Channel Viewer: [12] FR: Sdd21

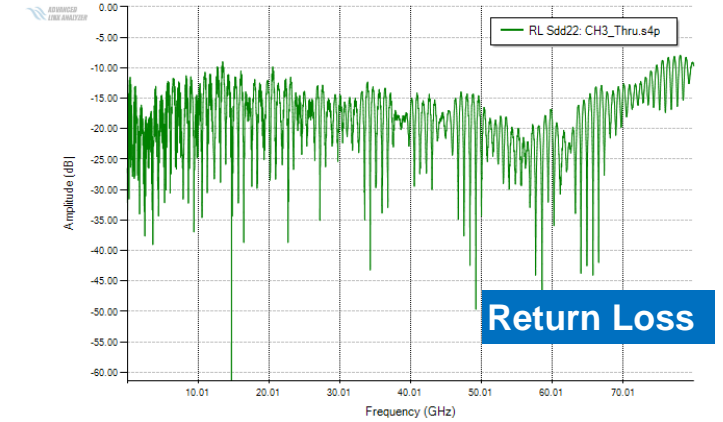


- IL: 25.94dB @ 56GHz
- ILD \approx 1dB (<56GHz)
- RL \approx 10dB (<56GHz)
- FEXT < 54dB (<56GHz)

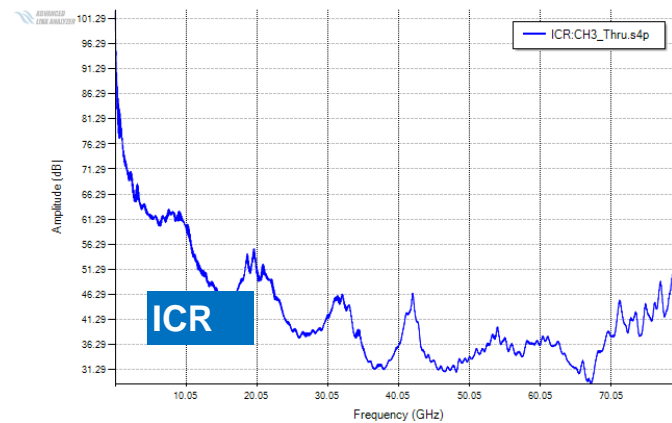
Channel Viewer: [14] CP: ILD



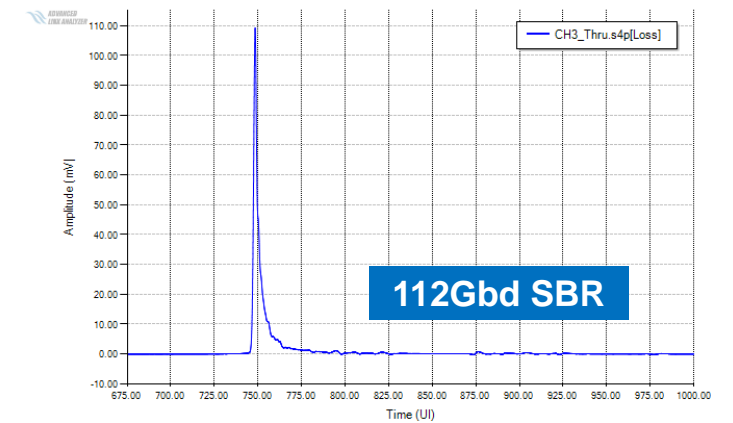
Channel Viewer: [15] CP: Return Loss



Channel Viewer: [16] CP: ICR



Channel Viewer: [17] SBR: Sdd21



See: [li_3df_01_220322.pdf](#)

Case B: 224 Gbps-PAM4 CR COM

Assumptions/Models/Parameters

- Summary
 - TX/RX die model: 3-segment LC model based on Intel 224Gbps PAM4 TC*
 - TX/RX package model: 2-segment TL model based on Intel test package & technology roadmap*
 - TX characteristics
 - Output amplitude ($A_v/A_{fe}/A_{ne}$): Same as 100GBASE-CR1
 - Rise/Fall Time (T_R): $0.31875 \cdot UI$ ($\sim 2.85\text{ps}$ @ 112Gbd, 3ps @ 106.25Gbd)
 - Jitter/Noise/Nonlinearity
 - A_{DD} , σ_{RJ} , $SNRTX$, RLM : Same as 100GBASE-CR1
 - EQ
 - 8 taps FIR: 6 pre-taps and 1 post-tap
 - RX characteristics
 - Noise filter BW (f_r): $0.5 \cdot \text{Baud Rate}$
 - Noise: η_{a_0} (TBD)
 - EQ: CTLE (scaled from 100GBASE-CR1), DFE (TBD)
 - DER: 10^{-4} (Same as 100GBASE-CR1)

Note: *: See [mli_3df_02a_220316](#)

Case B: 224Gbps-PAM4 CR COM Configuration

Table 93A-1 parameters			
Parameter	Setting	Units	Information
f_b	112	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.4e-4; 0.9e-4, 0.9e-4; 1.1e-4, 1.1e-4]	nF	[TX RX]
L_s	[0.13, 0.13; 0.15, 0.15; 0.14, 0.14]	nH	[TX RX]
C_b	[0.3e-4, 0.3e-4]	nF	[TX RX]
z_p select	[1 2]		[test cases to run]
z_p (TX)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (NEXT)	[12 29; 1.8 1.8]	mm	[test cases]
z_p (FEXT)	[12 31; 1.8 1.8]	mm	[test cases]
z_p (RX)	[12 29; 1.8 1.8]	mm	[test cases]
C_p	[0.4e-4 0.4e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	
A_fe	0.413	V	
A_ne	0.608	V	
AC_CM_RMS	0	V	[test cases]
L	4		
M	32		
filter and Eq			
f_r	0.5	*fb	
c(0)	0.5		min
c(-1)	[-0.4:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.2]		[min:step:max]
c(-3)	[-0.1:0.02:0.1]		[min:step:max]
c(-4)	[-0.1:0.02:0.1]		[min:step:max]
c(-5)	[-0.1:0.02:0.1]		[min:step:max]
c(-6)	[-0.1:0.02:0.1]		[min:step:max]
c(1)	[-0.2:0.02:0]		[min:step:max]
N_b	TBD	UI	
b_max(1)	TBD		
b_max(2..N_b)	TBD		
b_min(1)	TBD		
b_min(2..N_b)	TBD		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	44.8	GHz	
f_p1	44.8	GHz	
f_p2	112	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	0.7	GHz	

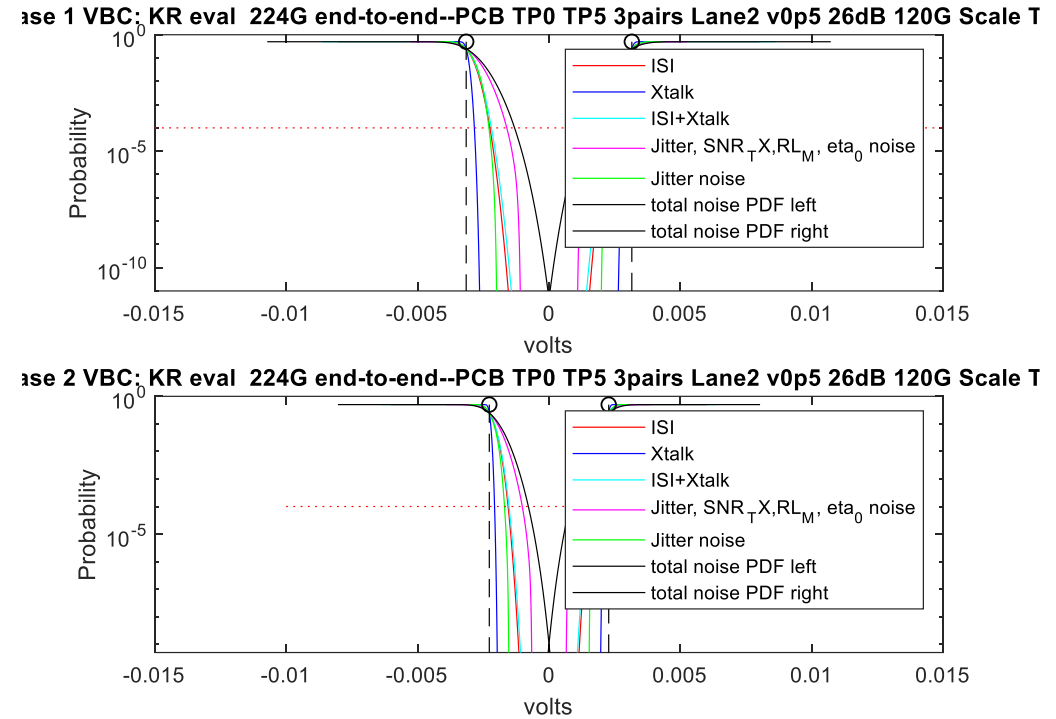
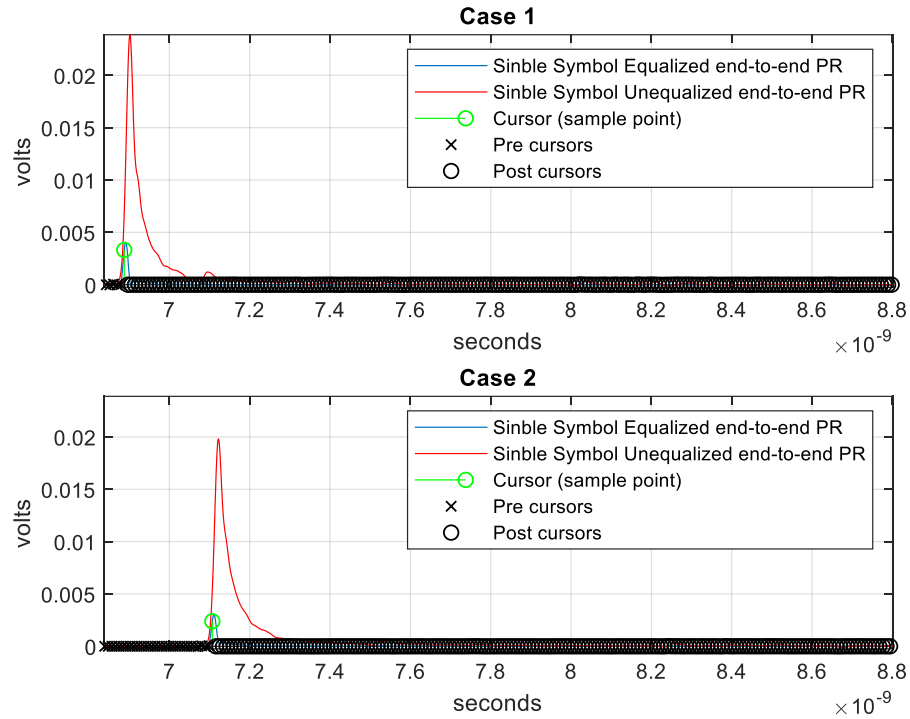
I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	1	logical
CSV_REPORT	1	logical
RESULT_DIR	\results\CEI200LR_(date)\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	LR_eval_	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	8	dB
DER_0	0.0001	
T_r	0.002845982	ns
FORCE_TR	1	logical
Local Search	2	
BREAD_CRUMBS	1	logical
SAVE_CONFIG2MAT	1	logical
PLOT_CM	0	
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	3500	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0]	[port1 port2]
TDR_W_TXPKG	0	
N_bx	21	UI
Tukey_Window	1	logical
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	TBD	V^2/GHz
SNR_TX	33	dB
R_LM	0.95	

Table 93A-3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.00089 0.000155]	
package_tl_tau	0.006141	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92-12 parameters		
Parameter Setting		
board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]	
board_tl_tau	5.790E-03	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	110.3	mm
z_bp (NEXT)	110.3	mm
z_bp (FEXT)	110.3	mm
z_bp (RX)	110.3	mm
C_0	[0.29e-4]	nF
C_1	[0.19e-4]	nF
Include PCB	0	logical
Floating Tap Control		
N_bg	TBD	0 1 2 or 3 groups
N_bf	TBD	taps per group
N_f	TBD	UI span for floating taps
bmaxg	TBD	max DFE value for floating taps
B_float_RSS_MAX	TBD	rss tail tap limit
N_tail_start	TBD	(UI) start of tail taps limit
ICN & FOM_ILD parameters		
f_v	0.742	*Fb
f_f	0.742	*Fb
f_n	0.742	*Fb
f_2	80.000	GHz
A_ft	0.600	V
A_nt	0.600	V
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V

Notable changes from 100GBASE-CR1

See [mli_3df_02a_220316](#) for die and PKG parameters

Case B: 224Gbps-PAM4 CR COM Analysis Results



- COM = 4.265dB w/ [12, 12]mm pkg (Case 1), 3.274dB w/ [31, 29]mm pkg (Case 2)

Summary and Next Steps

- 28 dB CR+/26 dB CR channels (BGA-to-BGA) supporting 1 meter cable are achievable with PAM4 modulation at 224 Gbps using COM, with the following realizable characteristics:
 - Reference die and package models extracted from the Intel TCs, test package, and roadmap
 - Linear scaling 100GBASE-CR1 to 200GBASE-CR1 by 2x for most parameters
 - To support 28 dB (CR+) with 224Gbps-PAM4, increase minimum TX amplitude to 1V, i.e. $A_v = 0.51625V$, from 0.8V, i.e. $A_v = 0.413V$, is needed
 - Higher TX swing corresponds to the higher TX power
 - Reduce RX noise filter BW, i.e., $f_r = 0.5$ from $f_r = 0.75$ of 100GBASE-CR1
 - Lower RX BW corresponds to the lower power
- Next Steps
 - Continue improving 1 meter CR channels
 - Determine the power optimized RX noise η_0 and DFE specific parameters.

Thank You!