224G Package and PCB Investigations and COM Reference Model

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OUTLINE

- 224G package design considerations
- Package technology enablement
- 224G package and PCB design practices
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- Proposed 224G Package T-Line Reference Model
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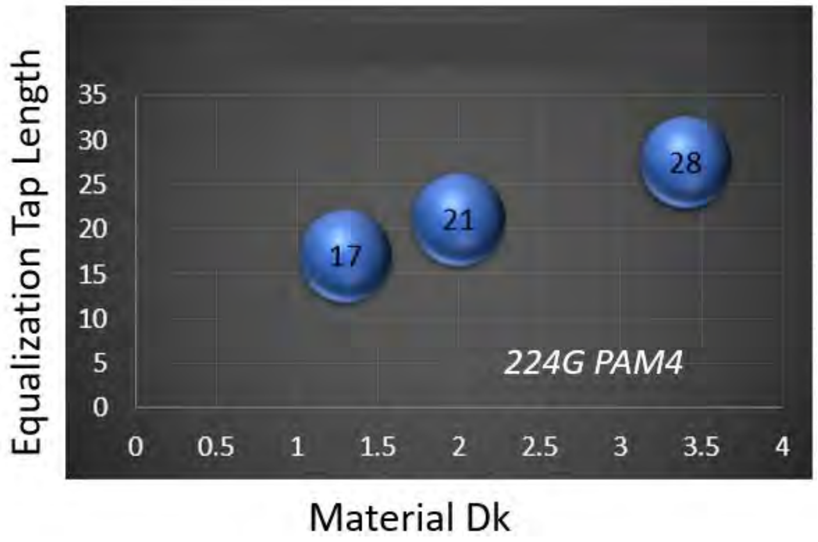
224G Package Design Considerations

- **Higher-order mode propagation and dispersion**
  - Small BGA ball pitch to eliminate the higher-order mode propagation
- **Plane resonance**
  - Adequate ground plane stitching to suppress the plane resonance
- **Transmission loss**
  - Skip-layer trace routing to mitigate the dielectric loss
- **Vertical transition and cross talk**
  - Optimized ball/PTH pattern/voiding and ball size for proper shielding and mitigation of discontinuities
- **PCB breakout adoption**
  - Smart BGA ball pattern for facilitating the board breakout

Package Technology Enablement

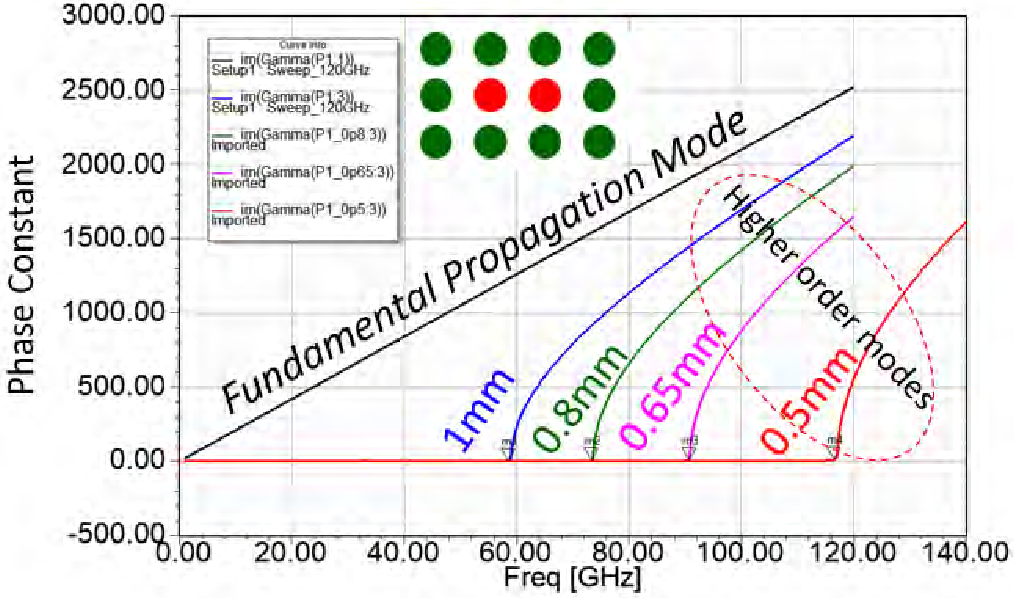
- **Low loss dielectric material**
  - Dielectric loss $\propto f$
- **Advanced copper surface treatment**
  - Metal loss $\propto \sqrt{f}$
- **Skip-layer technology**
  - $\text{Loss} \propto E^2 \; (E = {}^{V}/_{d})$ where d is the distance from signal to ground
- **Lower Dk dielectric material**
  - Less capacitive effects → More relaxed voiding requirement
  - Lower propagation delay ($\propto \sqrt{\varepsilon_r}$) → Less equalization tap length
  - Dk<2.0

0.12 dB/mm @ 56GHz

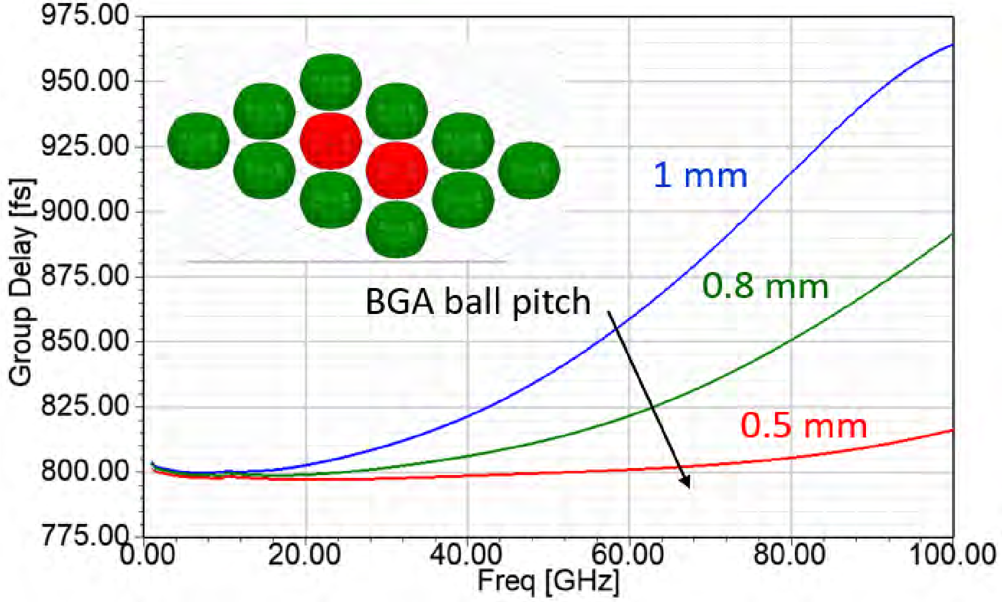


Package Ball Pitch Design: Higher-Order Mode and Dispersion

BGA



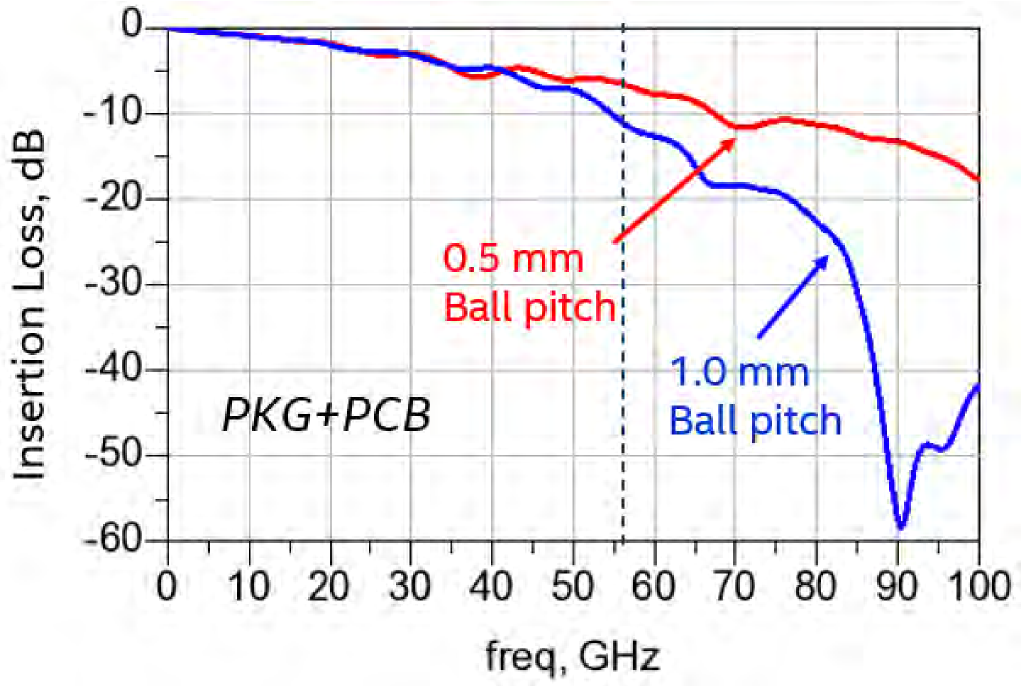
Cutoff frequency vs. BGA ball pitch



Normalized BGA group delay

Takeaway: The smaller the BGA ball pitch, the higher the cutoff frequency of higher-order modes; and the smaller the group delay variation hence the less dispersion (ISI).
1mm ball pitch cutoff frequency is ~ 58GHz, 0.8mm or smaller ball pitch is recommended for 224G PAM4.

Package Ball Pitch Design: Impact on PCB Transition Loss

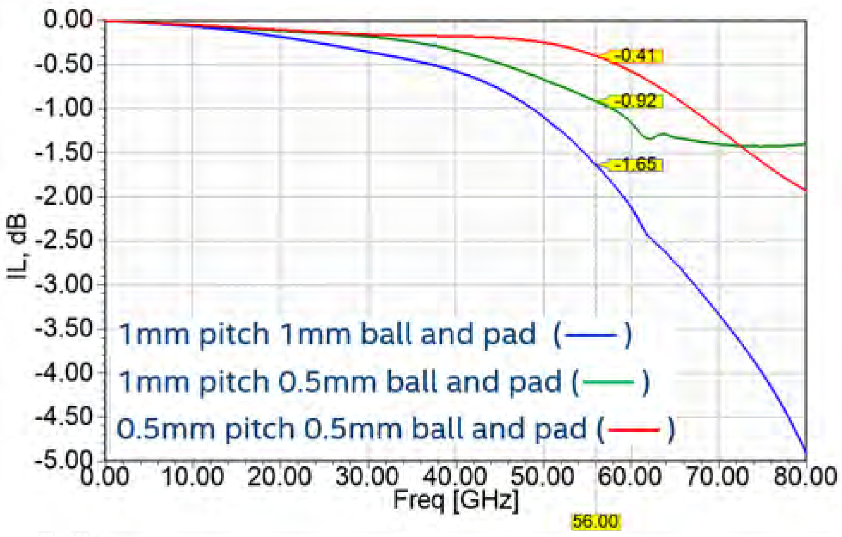


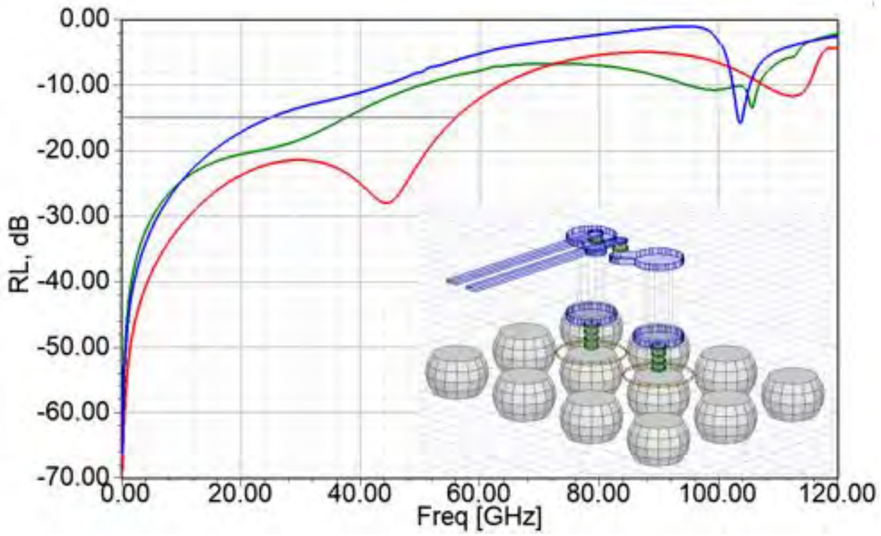
Package+PCB with 1mm vs. 0.5mm BGA ball pitch

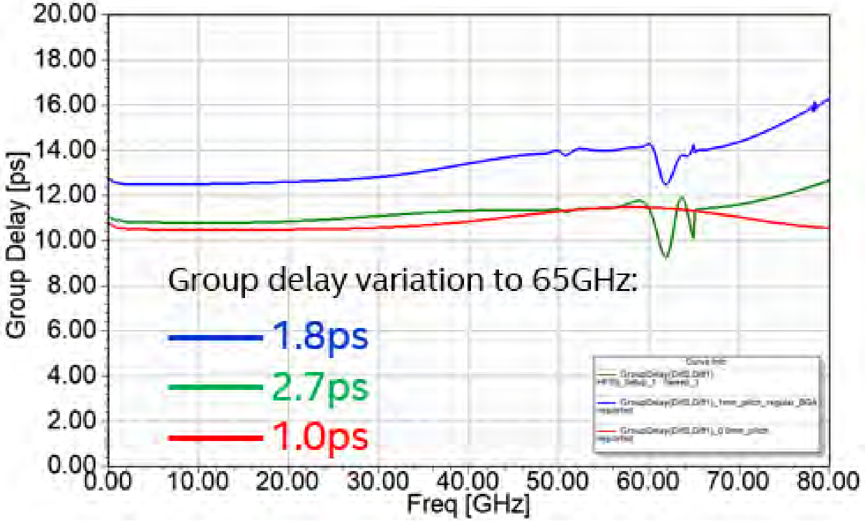
- PCB via-in-pad (VIPPO) pattern/pitch follows package BGA ball pattern/pitch
- More confined via configuration (from small package ball pitch) showed much smaller PCB transition loss (5 dB difference here) when using the same package ball pattern
- A properly selected ball pitch to suppress the higher-order mode propagation is the first step to designing a healthy 224G package

Package Ball Pitch and Ball Size Impact

- **Ball pitch – dispersion and loss**
- **Ball size – discontinuities and loss**
- **Comparison of**
  - o 1mm ball pitch + 1mm ball/pad size
  - o 1mm ball pitch + 0.5mm ball/pad size
  - o 0.5mm ball pitch + 0.5mm ball/pad size

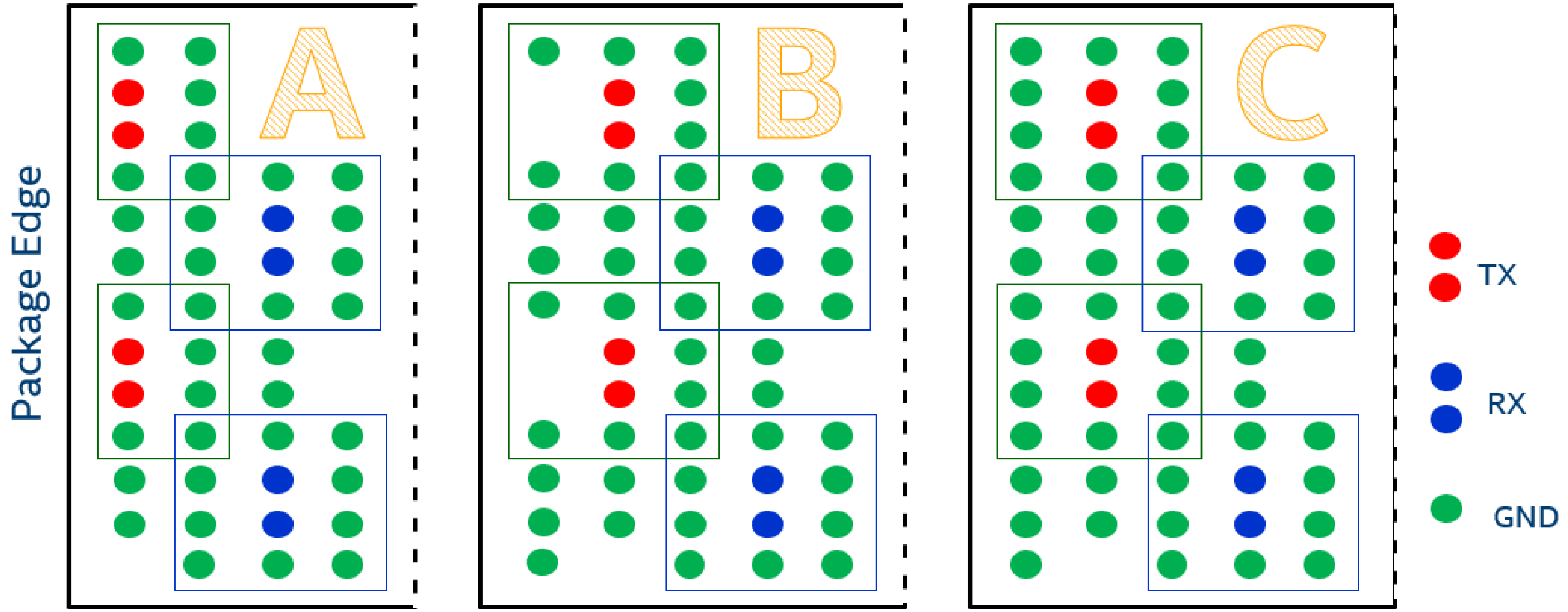






224G Package Ball Pattern Design

- **Case study of three BGA ball patterns**
  - Comparable return loss and insertion loss
  - 5-10 dB package cross talk improvement from A to C for TX



Package Localized Skip Layer Trace Design

- **Regular routing layer for**
  - GPIO/DDR
    - *Density and crosstalk control*
  - PDN
    - *Close ground reference*
- **Localized skip-layer routing for**
  - 224G Channels
    - *Loss control*

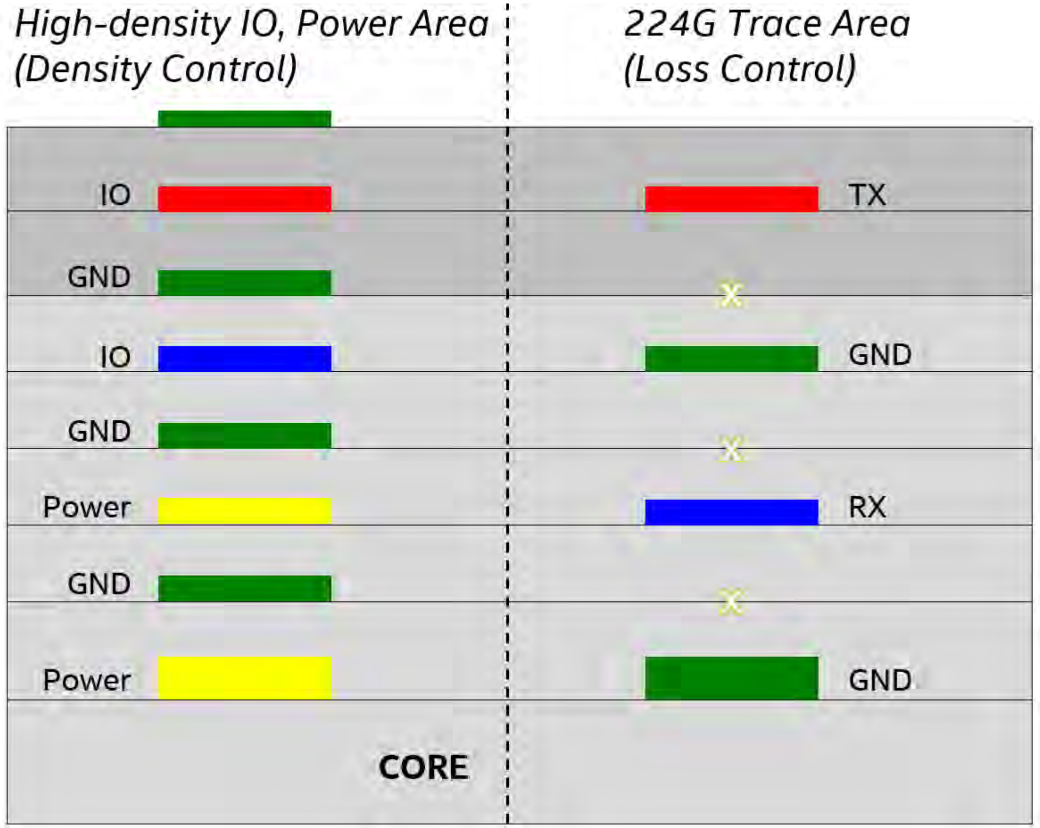
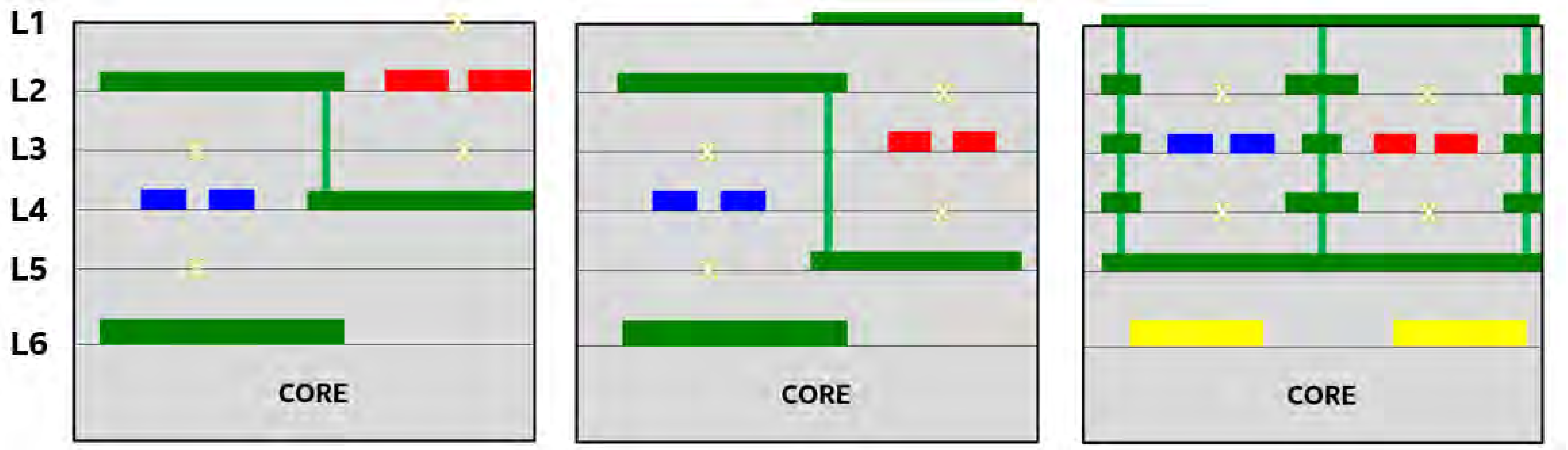


Illustration of a localized skip-layer configuration for 224G trace routing

Package Skip Layer Design: 12L Configurations



A

Embedded MSL
and STL

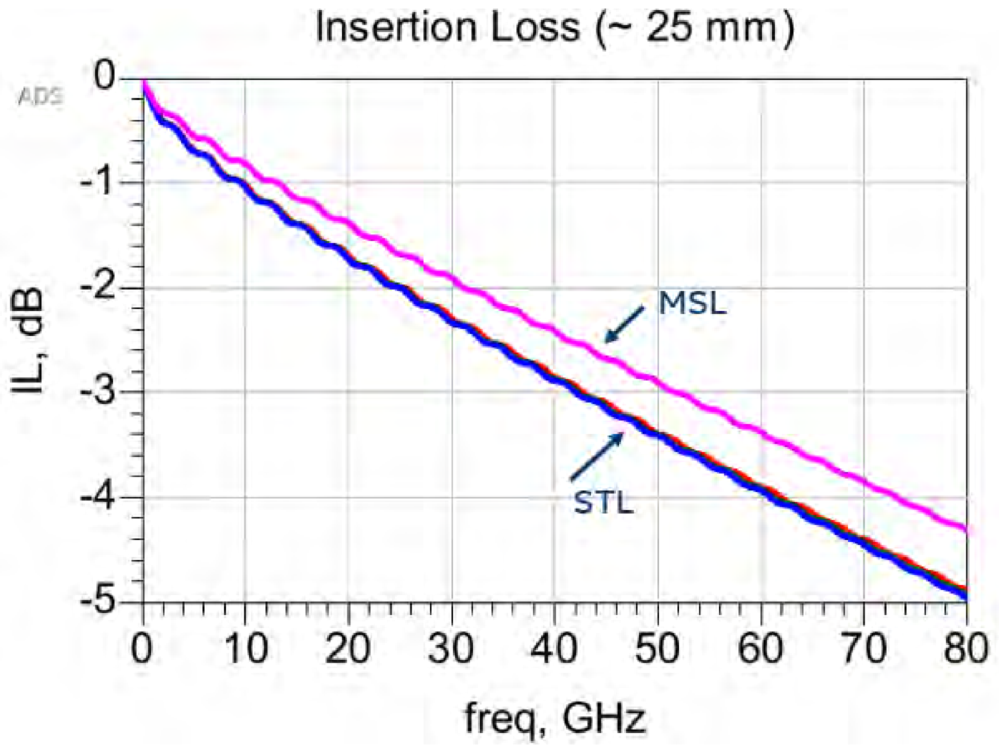
B

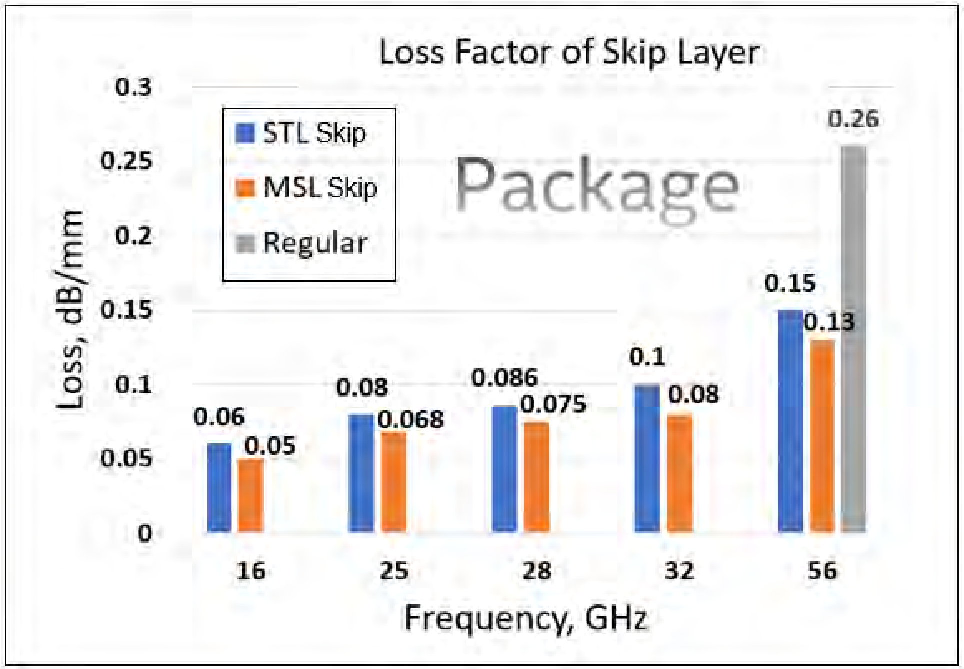
Shielded STL on
adjacent layers

C

Shielded STL on
same layers

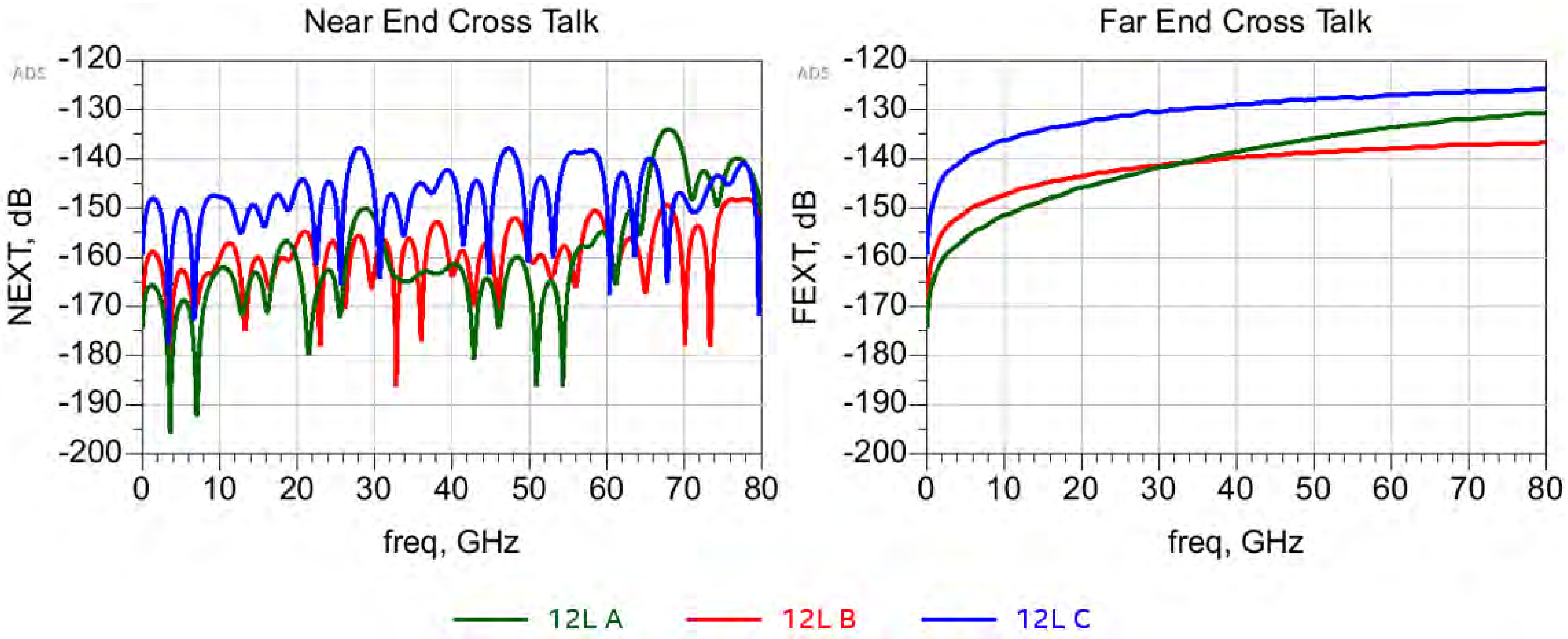
Package Skip Layer Trace Loss





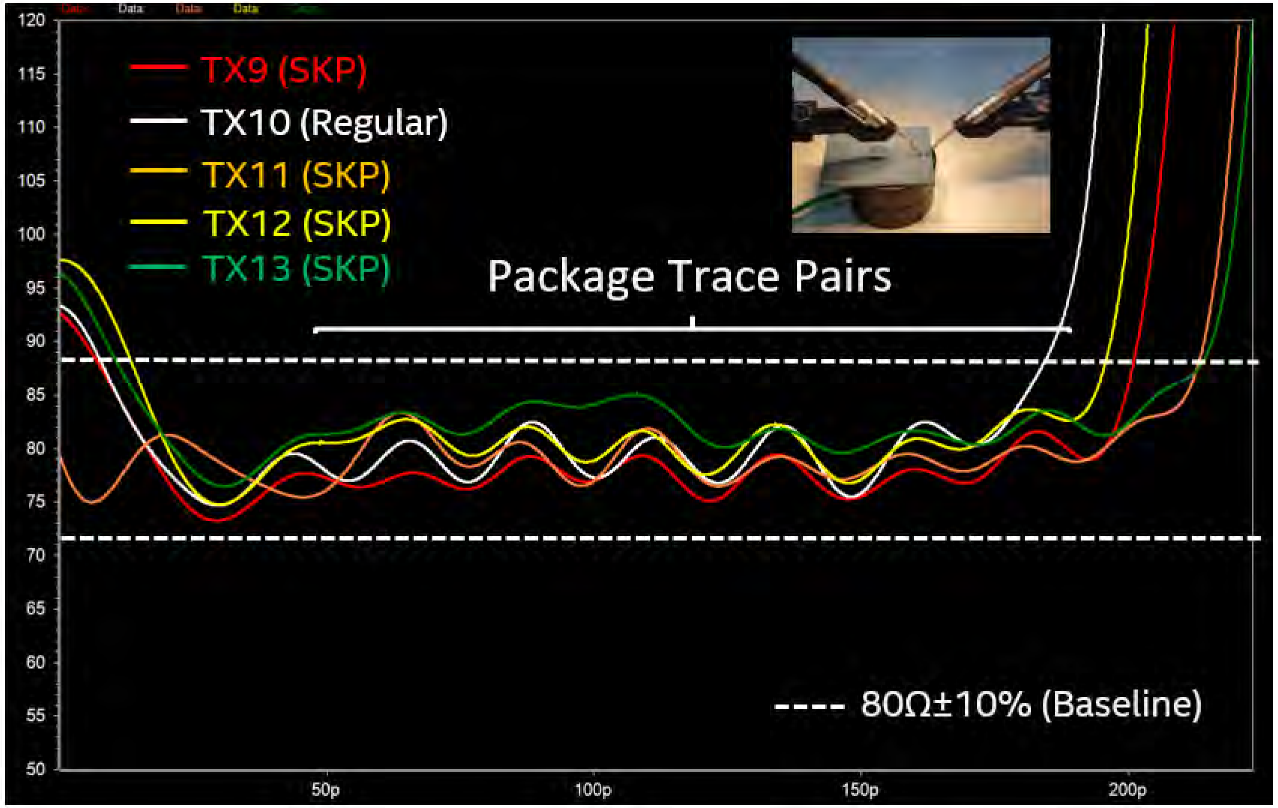
Notes: The trace loss was simulated based on current low loss material and copper surface treatment;
More advanced substrate material and copper surface treatment will further improve the package trace loss.

Package Skip Layer Trace Crosstalk



Takeaway: 25mm trace coupling is below -125dB to 56GHz following the suggested design guides.

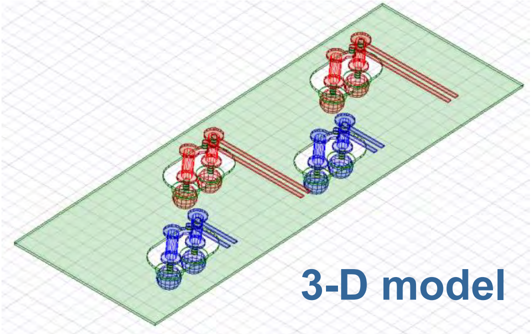
Package Trace Impedance Verification



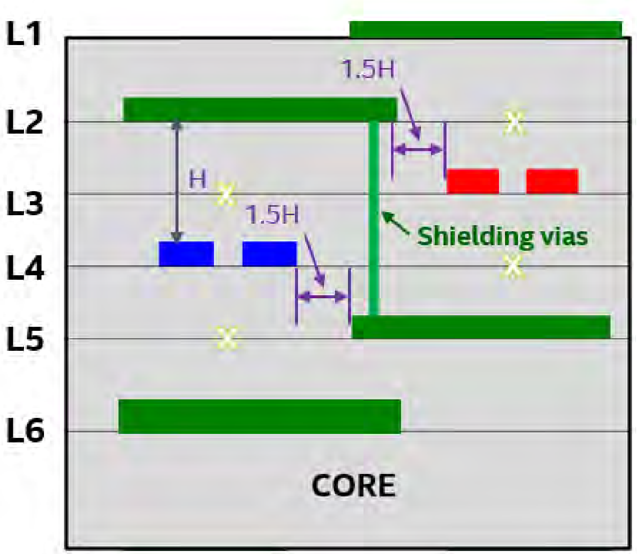
Notes: The TDR measurement verified the 80Ω differential impedance with ±10% tolerance for the skip-layer and the regular trace design;
No significant difference was seen between the skip-layer and the regular trace design from the TDR measurement.

224G Package Design Practice

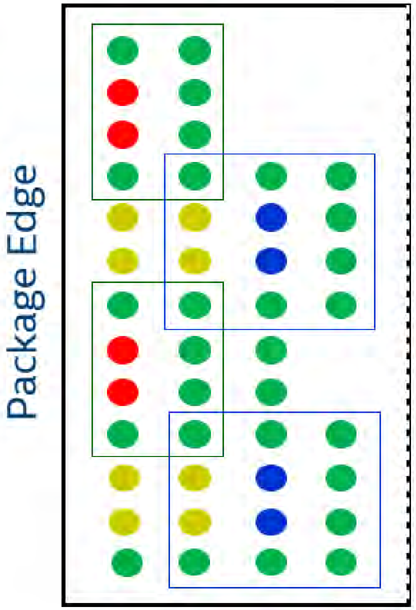
- **12L package with low loss material**
- **0.5mm ball pitch (ball pattern A)**
- **Skip-layer configuration B**
- **400 um core**
- **Trace-PTH-BGA optimization**
  - o Discontinuities
  - o Loss
  - o Crosstalk
  - o PCB breakout



3-D model



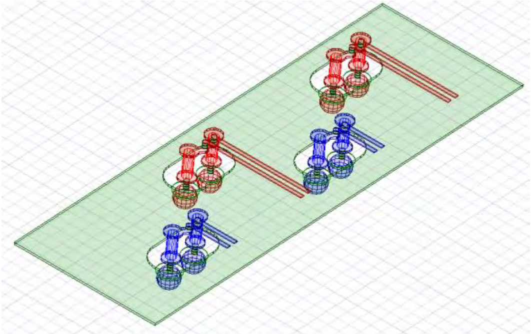
Skip-layer trace

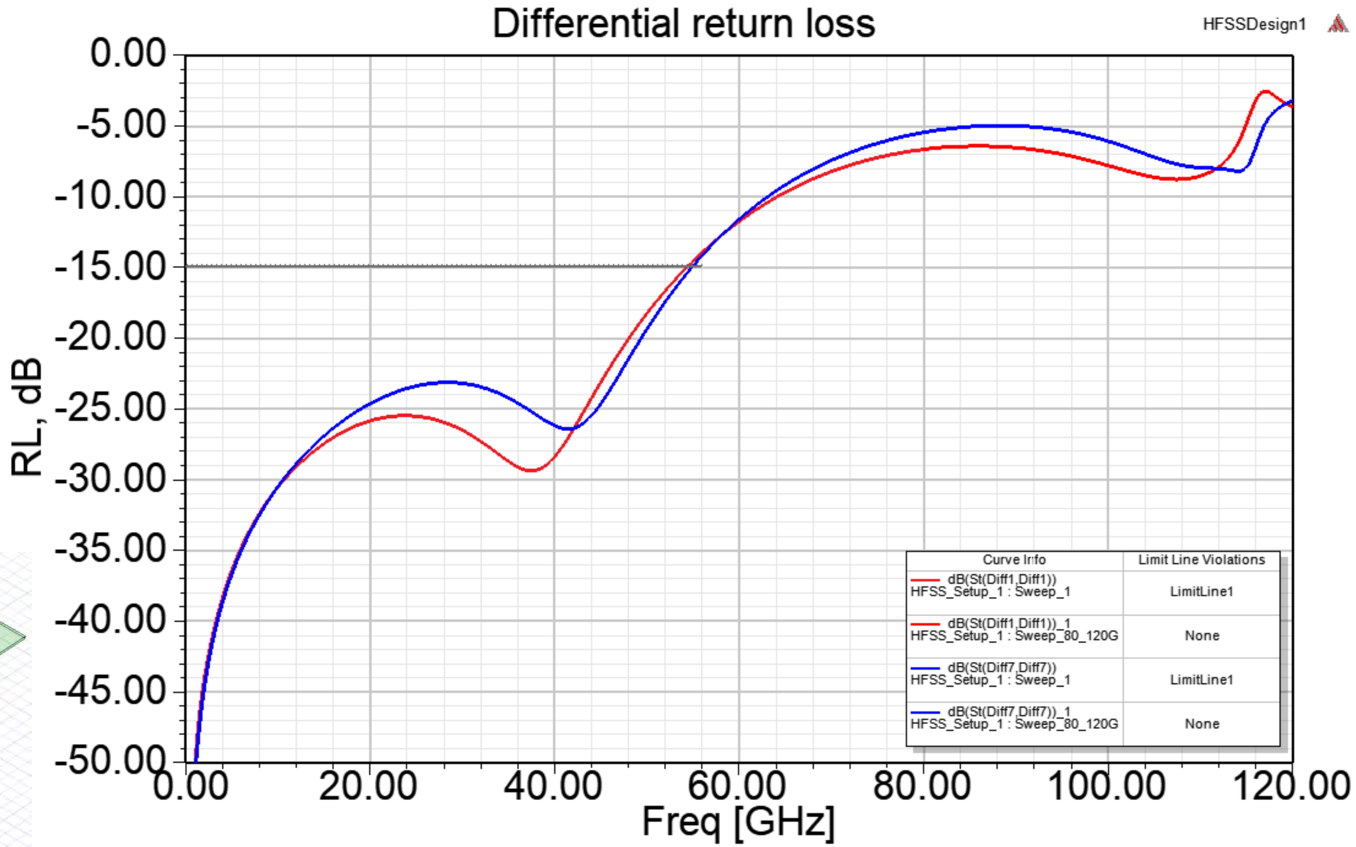


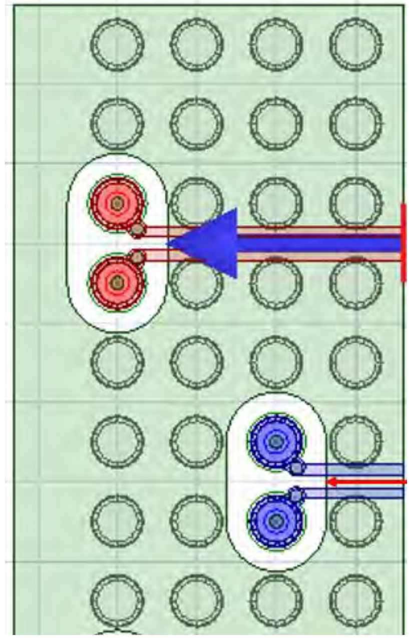
BGA ball pattern

Package Differential Return Loss

- **De-embed trace**
- **-15 dB to 56GHz**

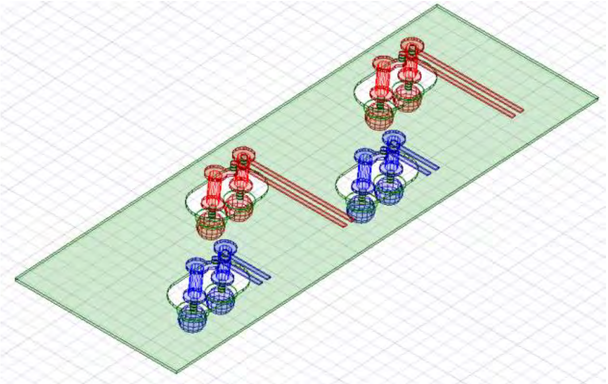


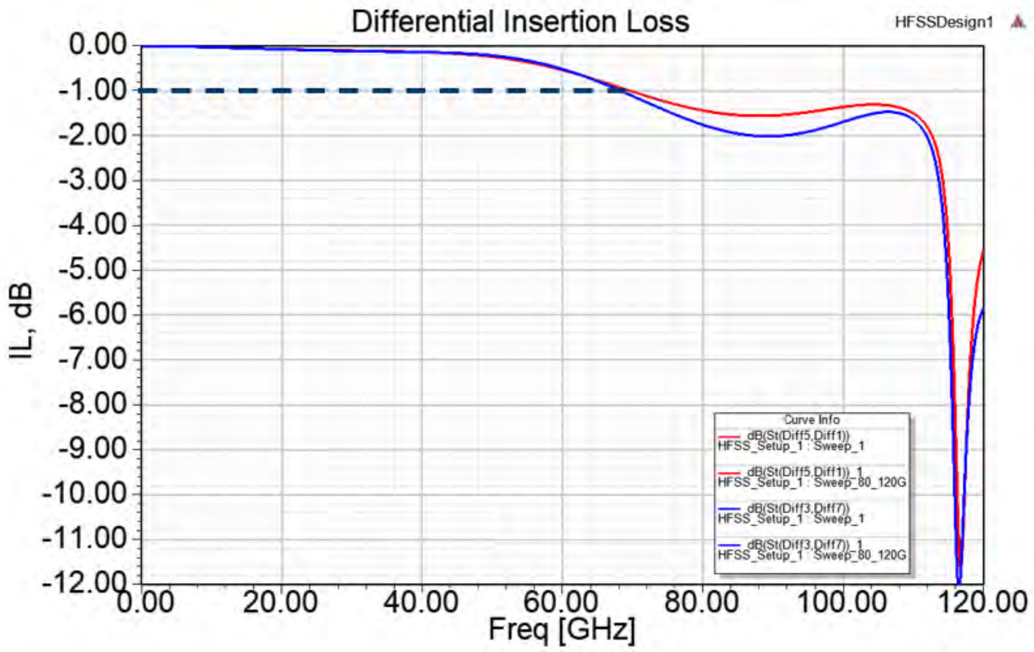


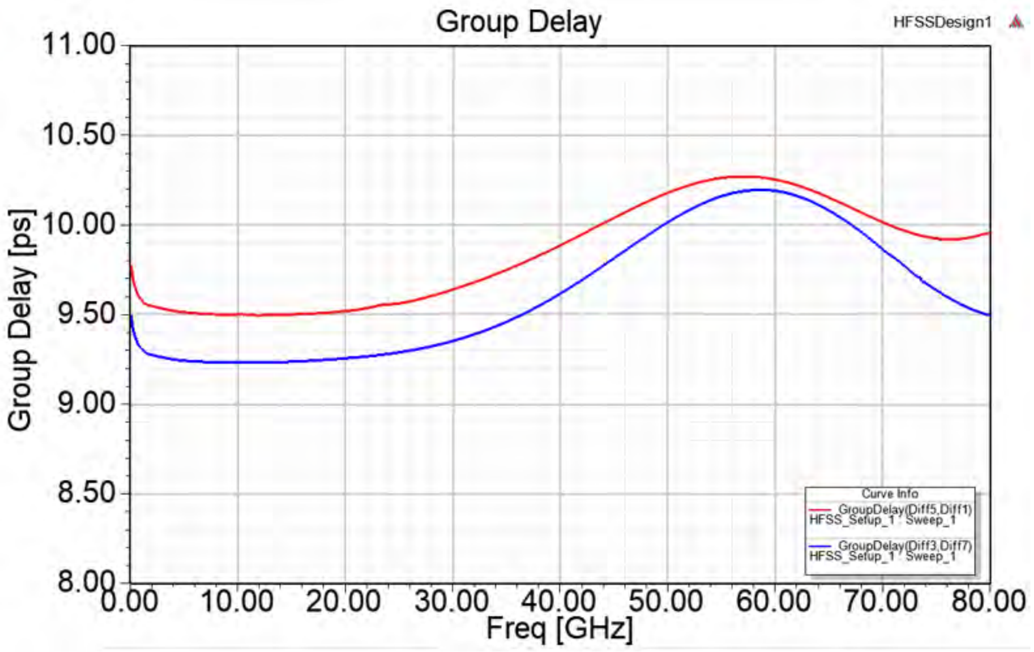


Package Differential Insertion Loss and Group Delay

- **1 dB BW: ~ 68GHz**
- **Group delay skew: < 1ps to 80GHz**

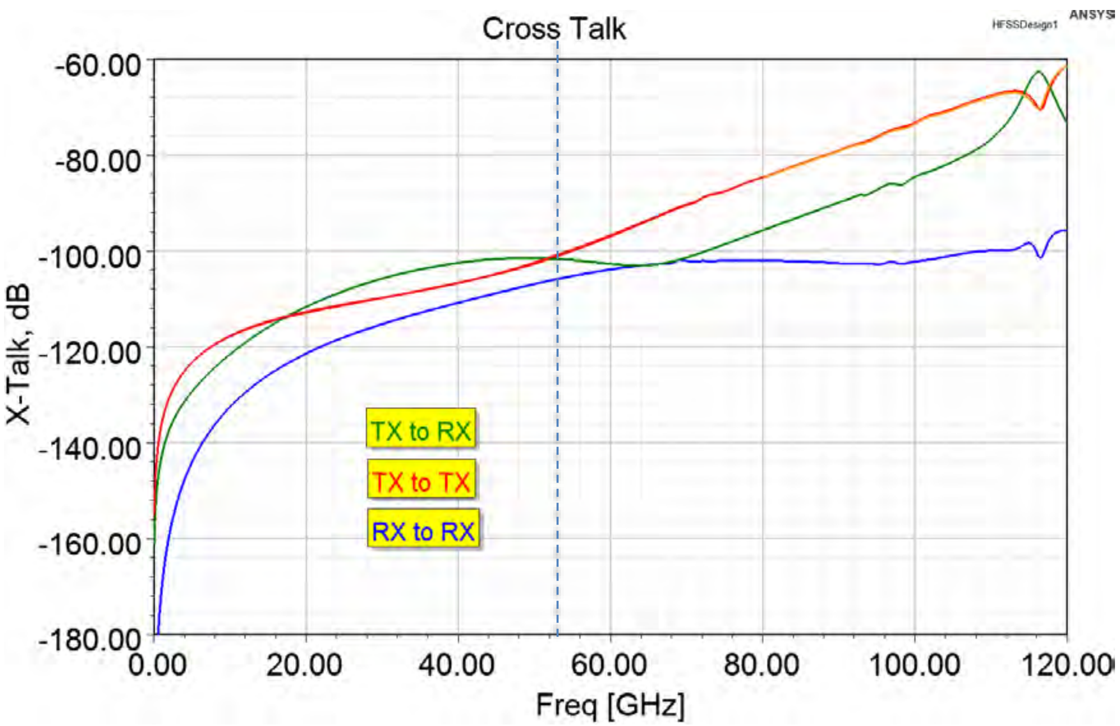


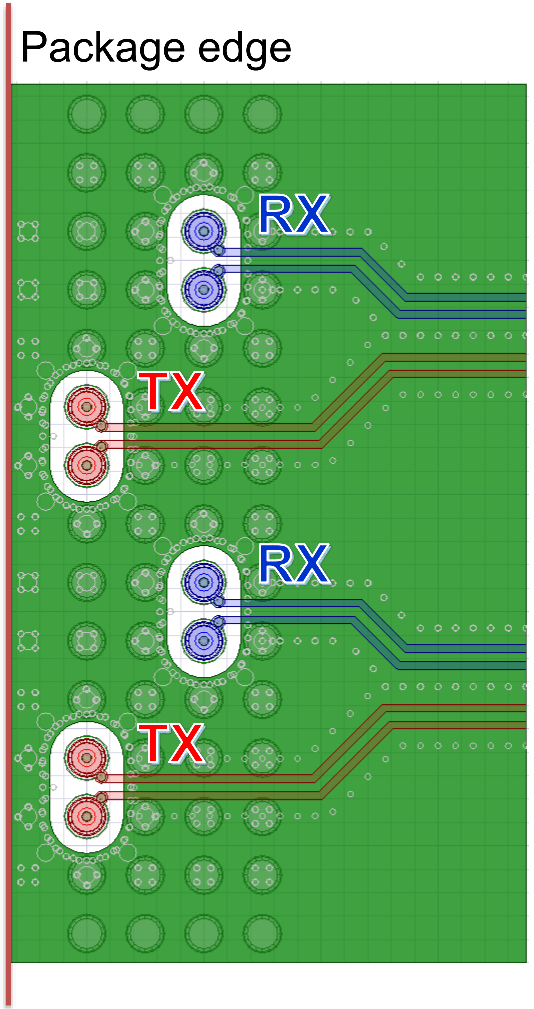




Package Differential Crosstalk

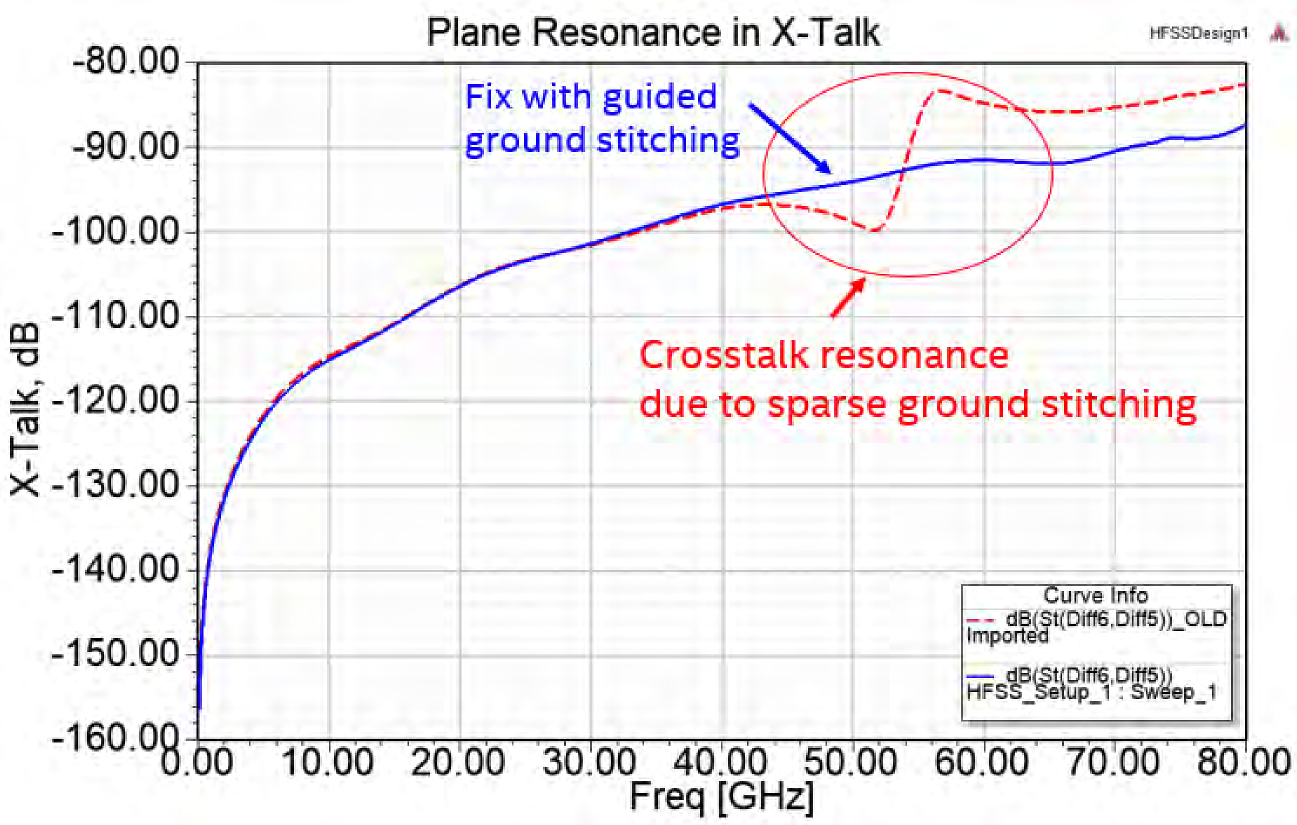
- Crosstalk below -98dB up to 56GHz
- Crosstalk to edge ball without full shielding increases dramatically with frequencies beyond 56GHz





Package Plane Resonance

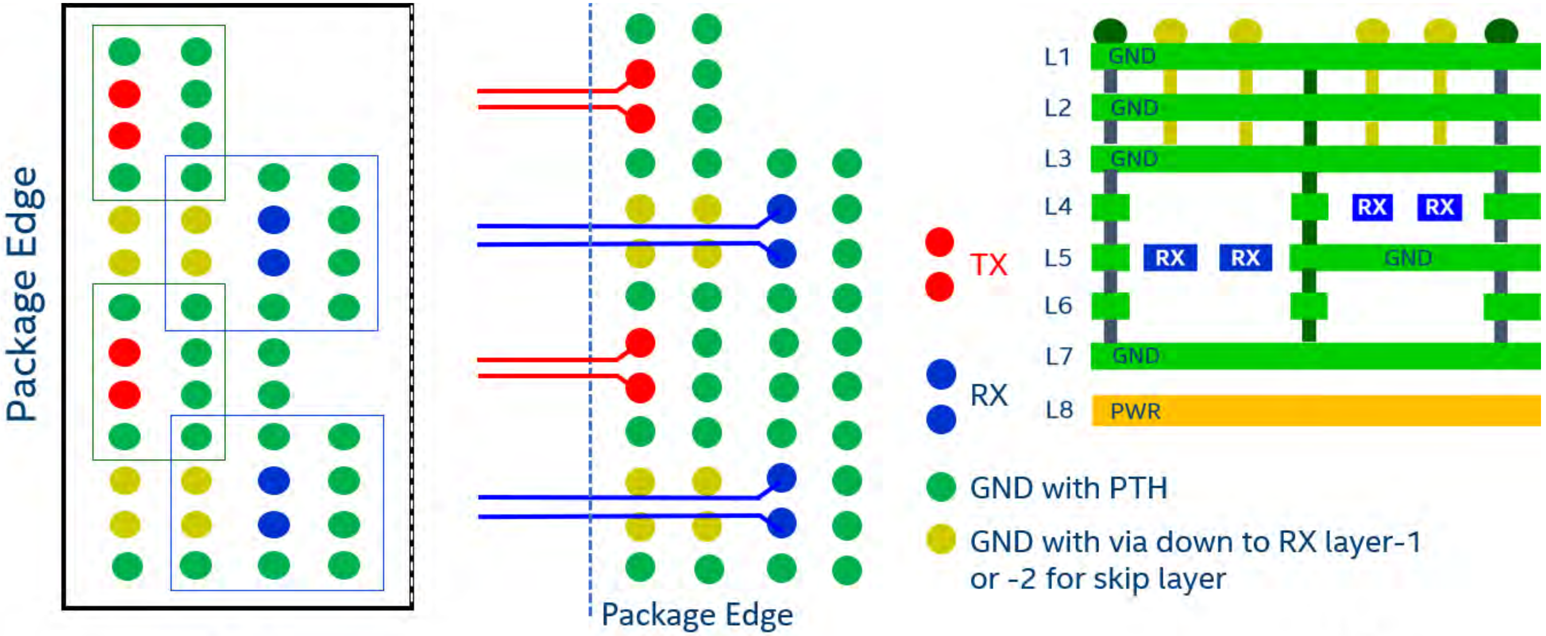
- **Ground plane stitching via guideline**
  - Via pitch < 1/10 wavelength along the TX/RX traces
  - Via pitch < ¼ wavelength everywhere else in the vicinity of 224G channel routing



PCB Design – BGA Ball Breakout

- Smart BGA ball pattern can ease the PCB breakout
- Properly separated ball pairs

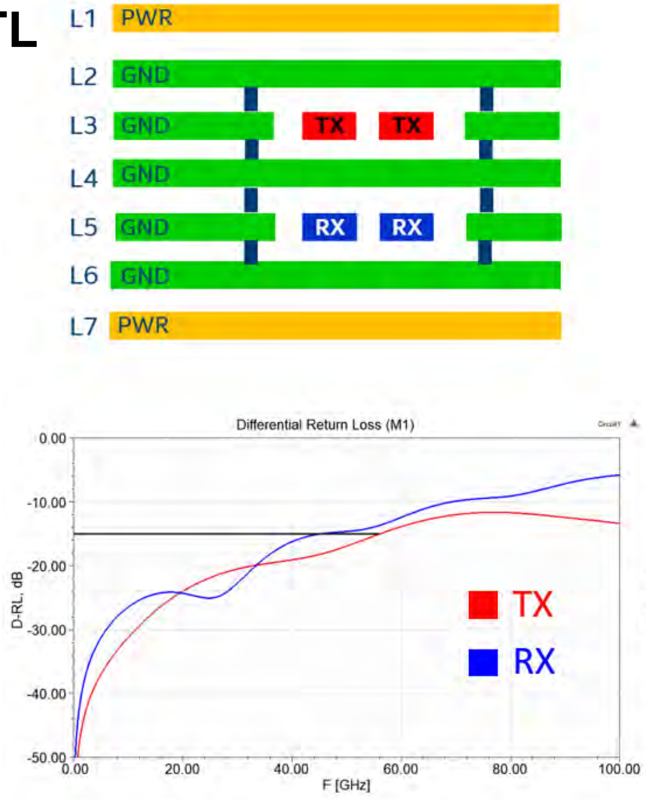
  can reduce trace to via coupling



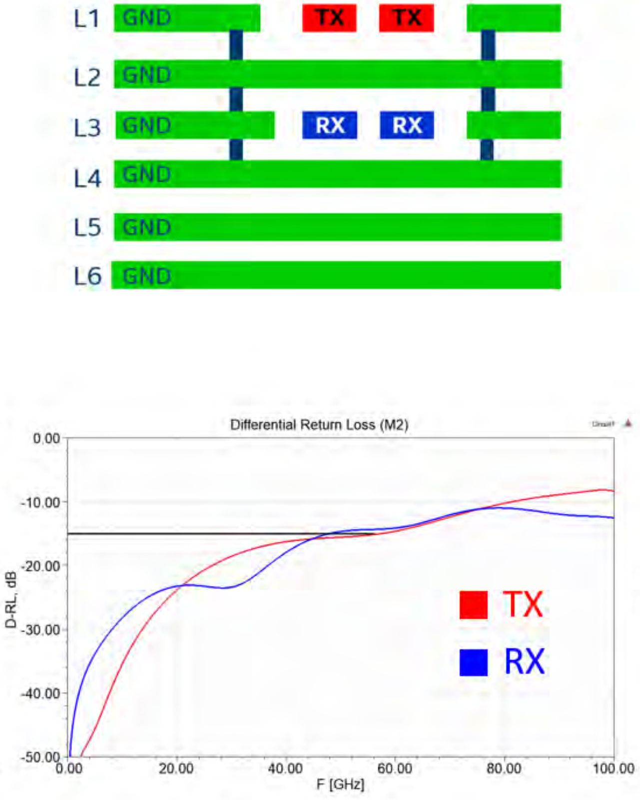
(a) (b) (c)

PCB Design – Trace Routing Configurations

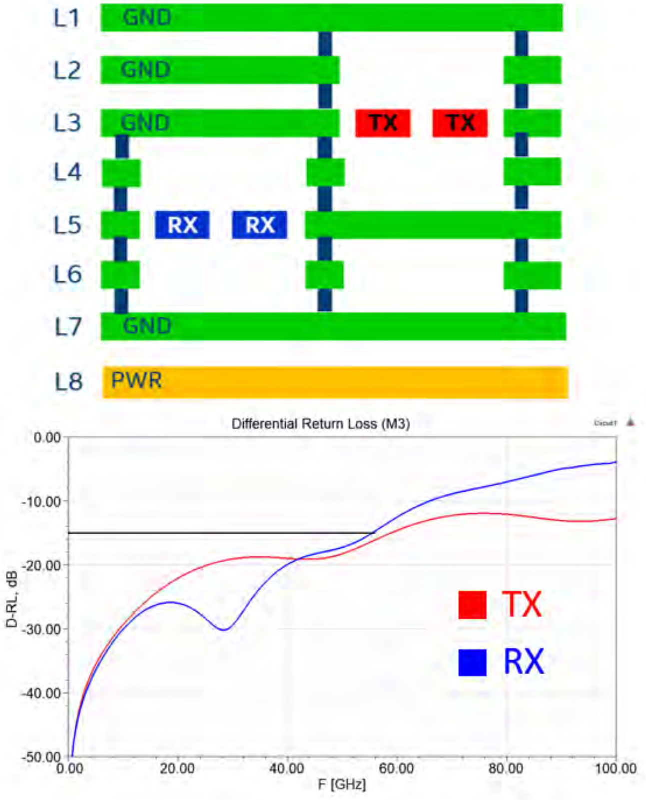
- **Regular STL**
- **Regular MSL + STL**
- **Skip-layer STL**



(a) Regular STL



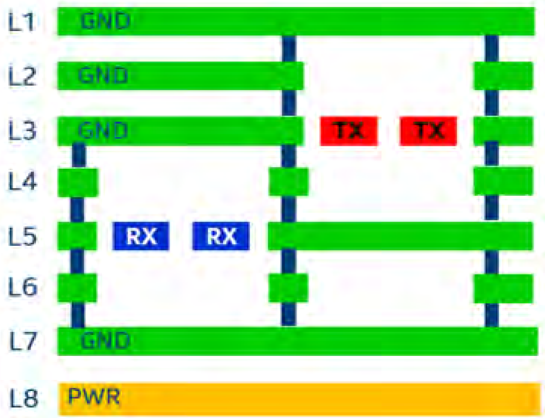
(b) Regular MSL

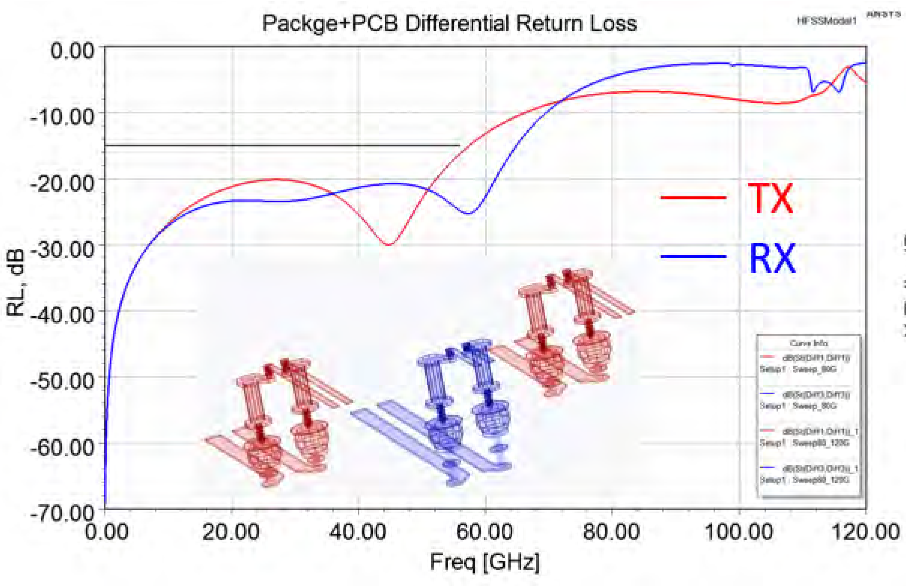


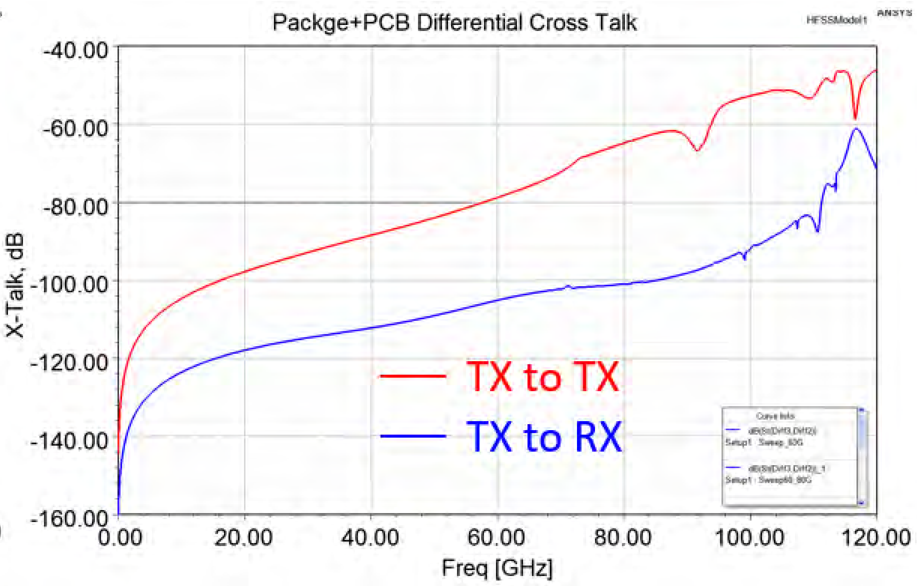
(c) Skip Layer STL

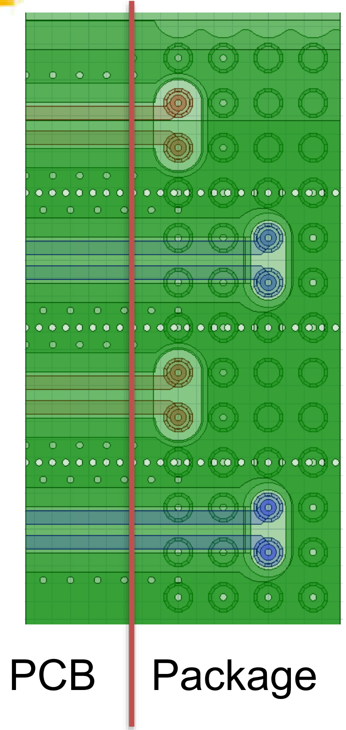
Package-PCB Co-modeling

- Package-PCB breakout return loss < -15 dB to 56GHz
- Edge ball/via coupling < -80 dB to 56GHz
- Inner ball/via coupling < -100 dB to 56GHz



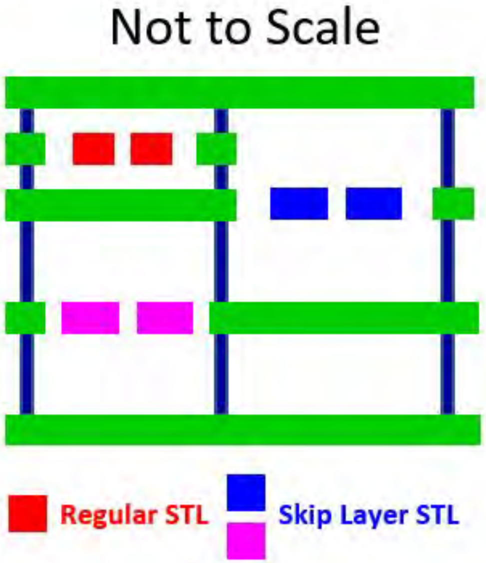


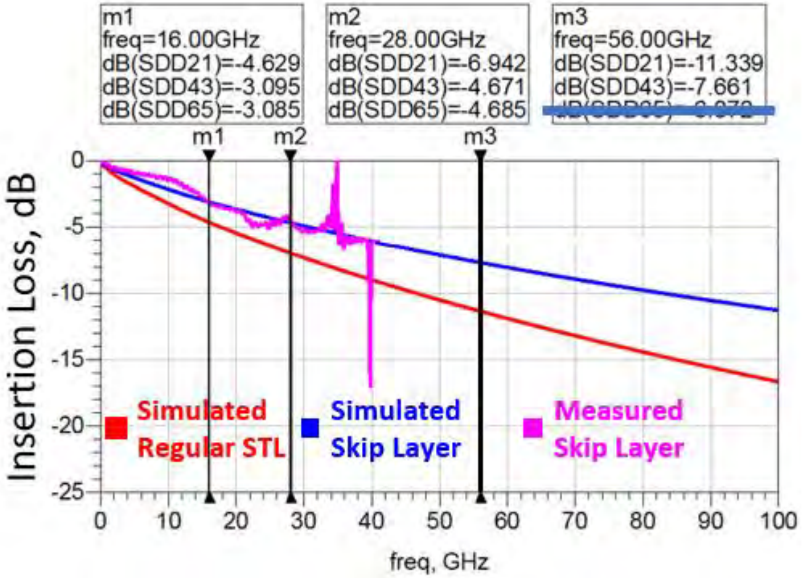




PCB Trace Loss Correlation

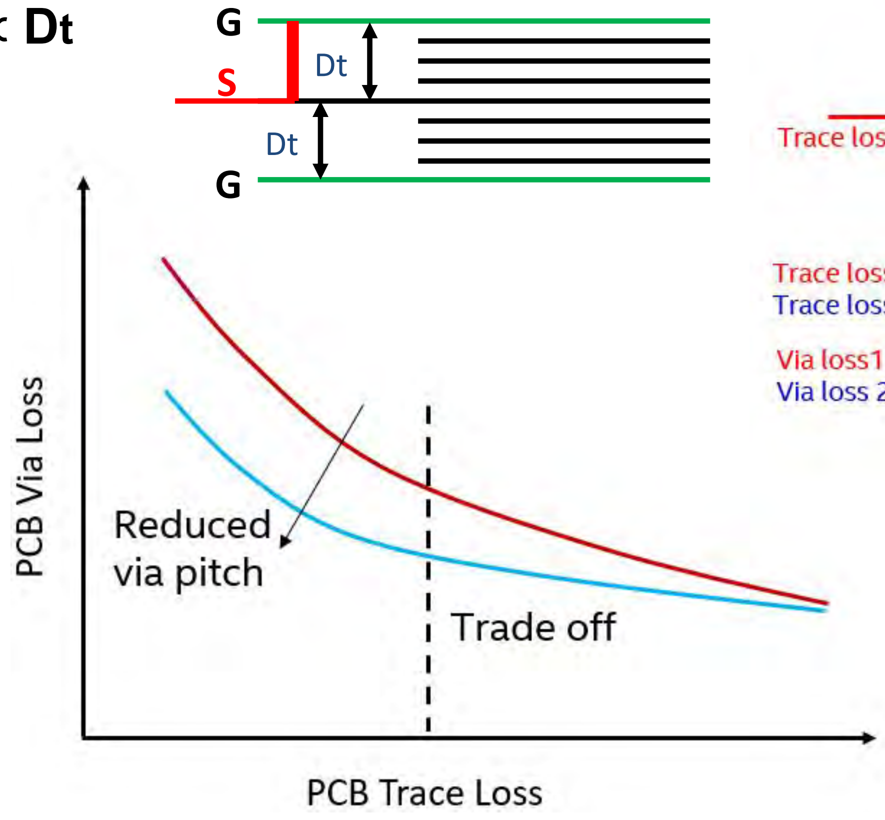
- **Standard PCIe AIC (Add-in-Card) stackup**
- **PCB material: M7N**
- **Trace loss at 56GHz**
  - o Regular STL: 2.8dB/inch
  - o Skip-layer STL: 1.9dB/inch

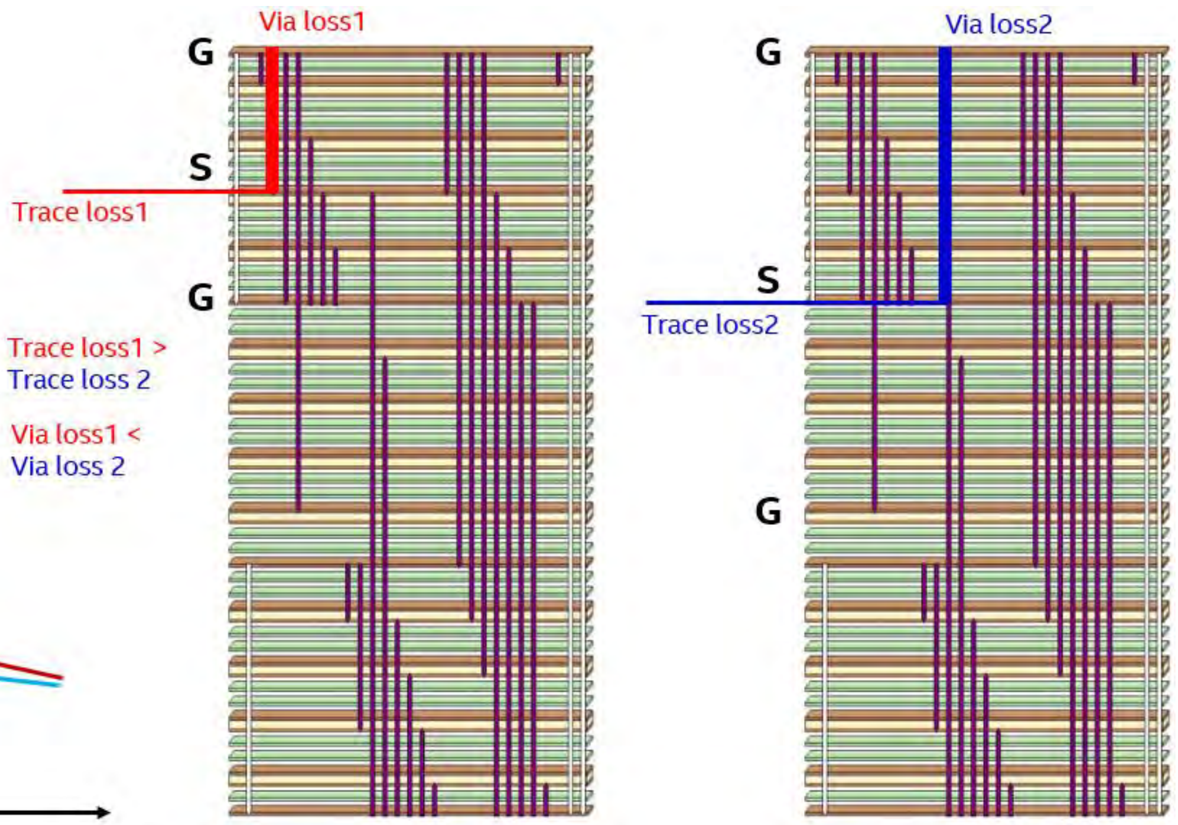




PCB Loss Improvement

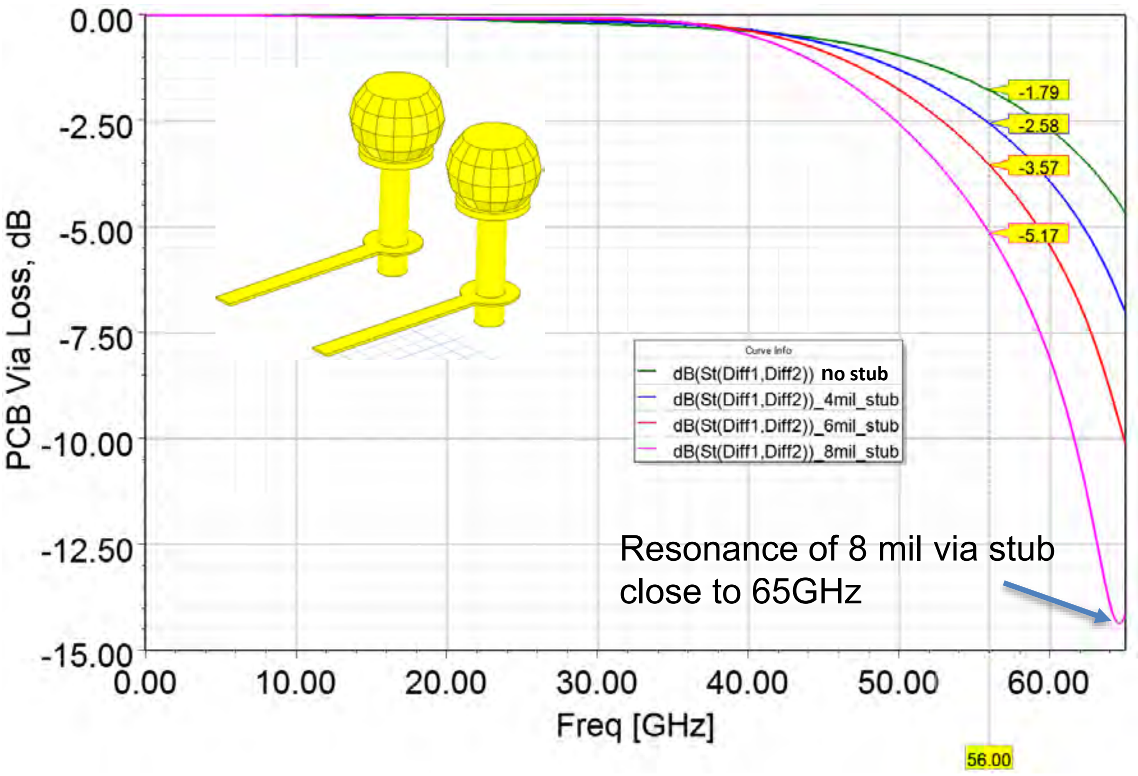
- **Skip-layer trace routing**
- **PCB trace loss ∝ 1/Dt**
- **PCB via loss ∝ Dt**
- **Trade-off of Dt**





PCB Via Stub Effects

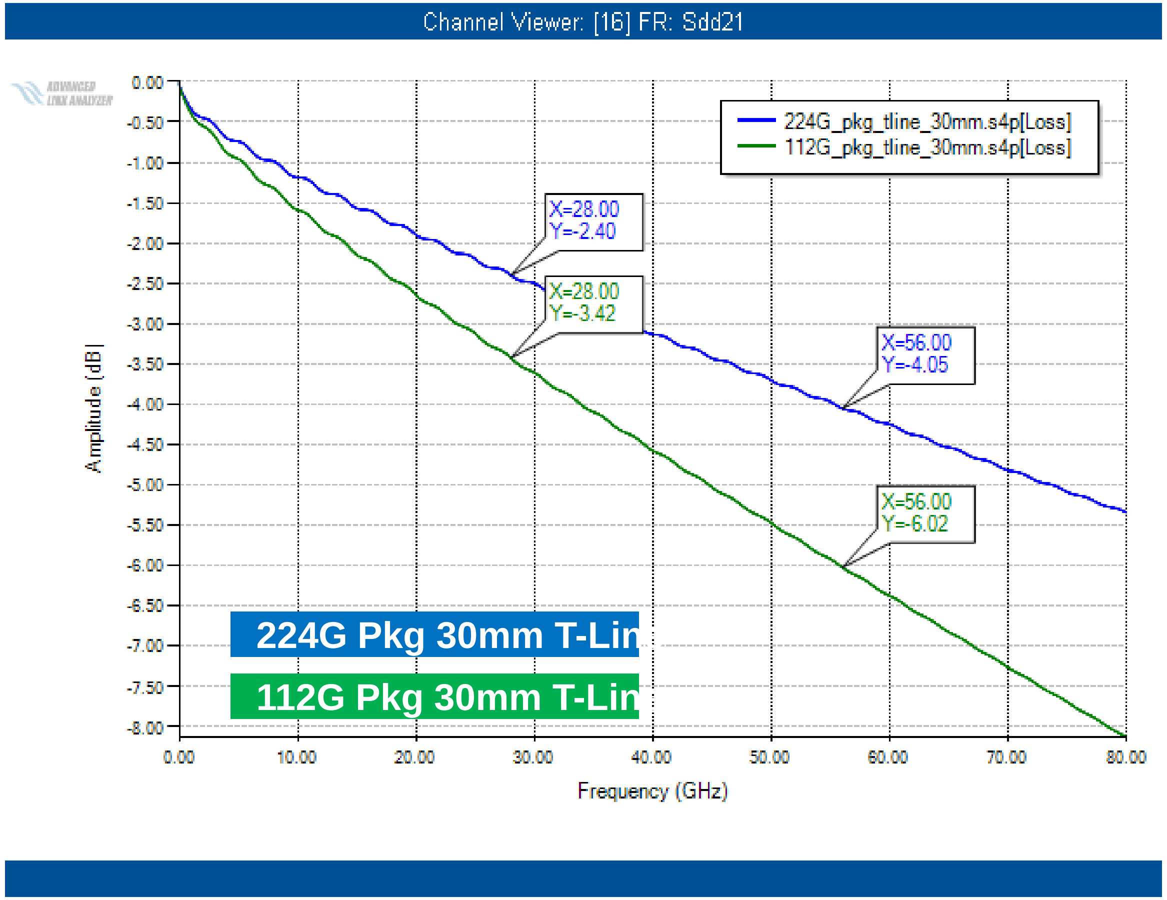
- PCB via loss increases with via stub length
- < 6 mil via stub length is recommended for 224G PAM4 design



PCB via loss with different via stub lengths

A Proposed Host Reference Package Model for 802.3df

Parameter	112G Package T-Line Model Parameters	Proposed 224G Package T-Line Model Parameters
Z_p	30 mm	30 mm
γ_0	0 /mm	**0 /mm**
τ	6.141e-3 ns/mm	**6.141e-3 ns/mm**
a_1	9.909e-4 ns$^{1/2}$/mm	**8.9e-4 ns$^{1/2}$/mm**
a_2	2.772e-4 ns/mm	**1.55e-4 ns/mm**
Z_c	87.5 Ω	**87.5 Ω**
R_o	50 Ω	50 Ω
C_p	87 fF	**40 fF**



224G PAM4 Package Design Summary

- **Desired next generation package trace loss target for interpretation flexibility: 0.1 dB/mm at Nyquist frequency**
  - Skip-layer trace routing is required for mitigating the transmission loss
  - Low loss material and advanced copper surface treatment are required
- **0.8mm ball pitch is recommended (0.65mm or smaller preferred)**
- **Smaller ball size can further reduce discontinuities and package loss**
- **BGA ball pattern needs to be PCB breakout friendly and fully shielded**
- **Ground stitching via pitch < 1/10 wavelength along TX/RX traces and < 1/4 wavelength everywhere else in the vicinity of the 224G channel routing are required**

224G PAM4 PCB Design Summary

- **Desired next generation PCB trace loss target for interpretation flexibility: 1 dB/inch at Nyquist frequency**
  - Skip-layer trace routing is required
  - Ultra low loss material is required
  - HVLP copper surface treatment is required
- **PCB via stub length < 8mil is required**
- **Well controlled process variation of Dk, Df and dielectric thickness is required**

References

[1] J. Jiang et al, “Designing 224G PAM4 High Performance FPGA Package and Board with Confidence”, *Designcon*, 2021.

Thank You!