Reference Die and Package Models for 802.3df Host

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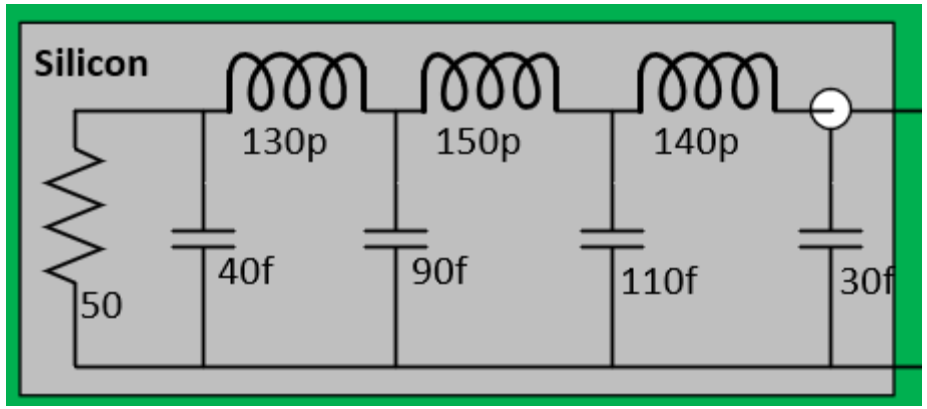
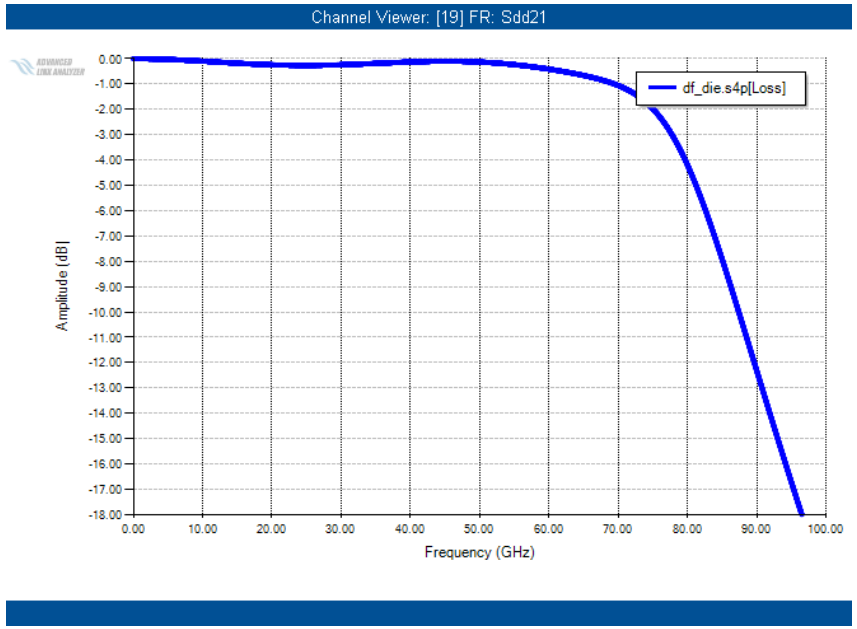
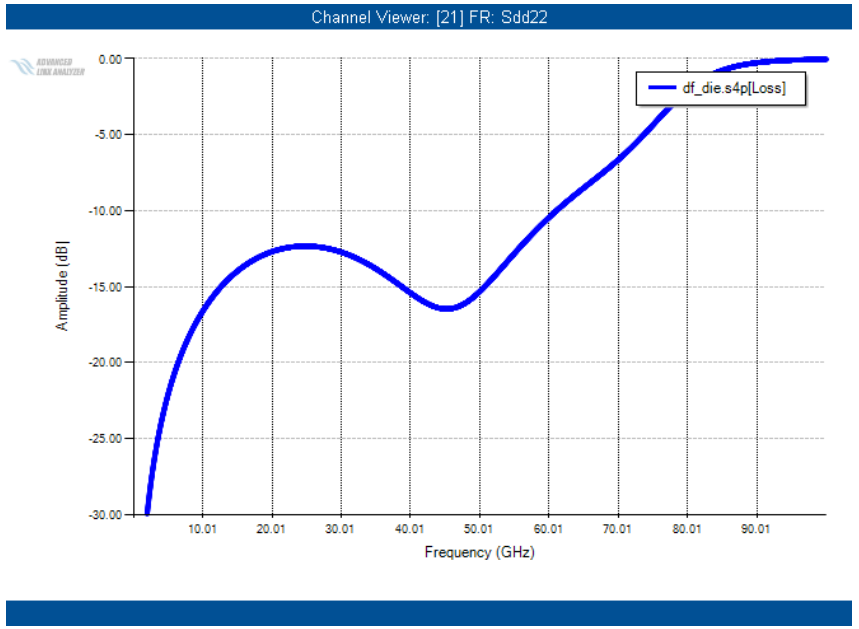
Method and Objectives

- This presentation intents to provide a 224 Gbps-PAM4 reference die model and parameters which are extracted from the Intel test chips [1], [2]
- This presentation intents to provide a 224 Gbps-PAM4 reference package model and parameters which are extracted from test packages and roadmap at 2024+[3], [4]
- Those reference die and package models are required to form the basis/foundation for 802.3df COM simulations and specification developments

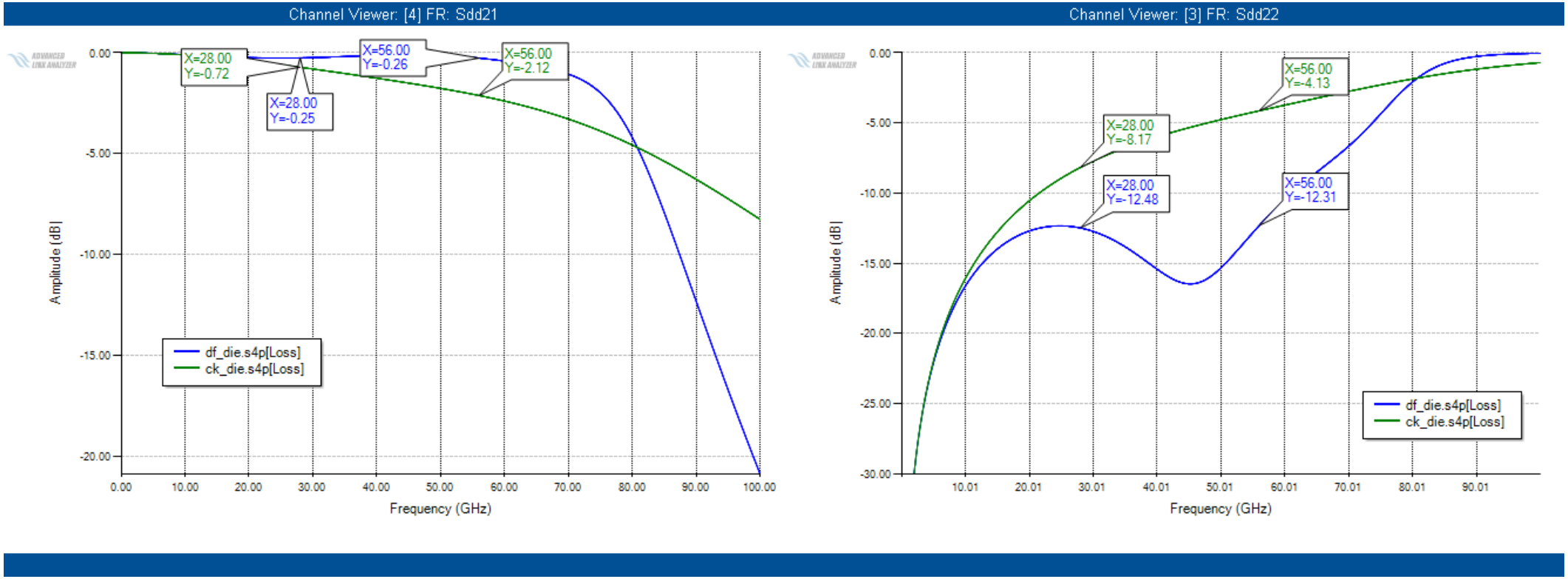
A Proposed Reference Die Model for 802.3df





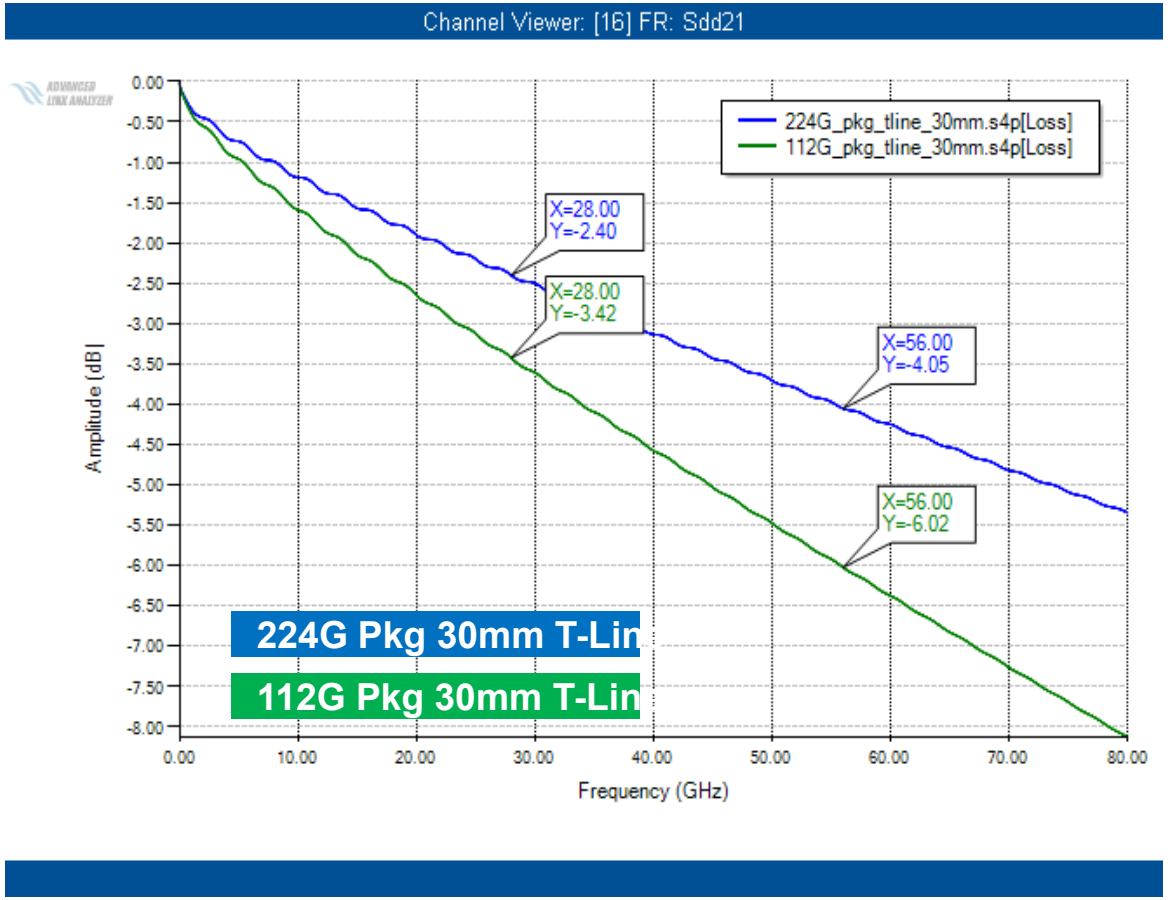


The Proposed Reference Host Die Model for 802.3df vs. that of 802.3ck



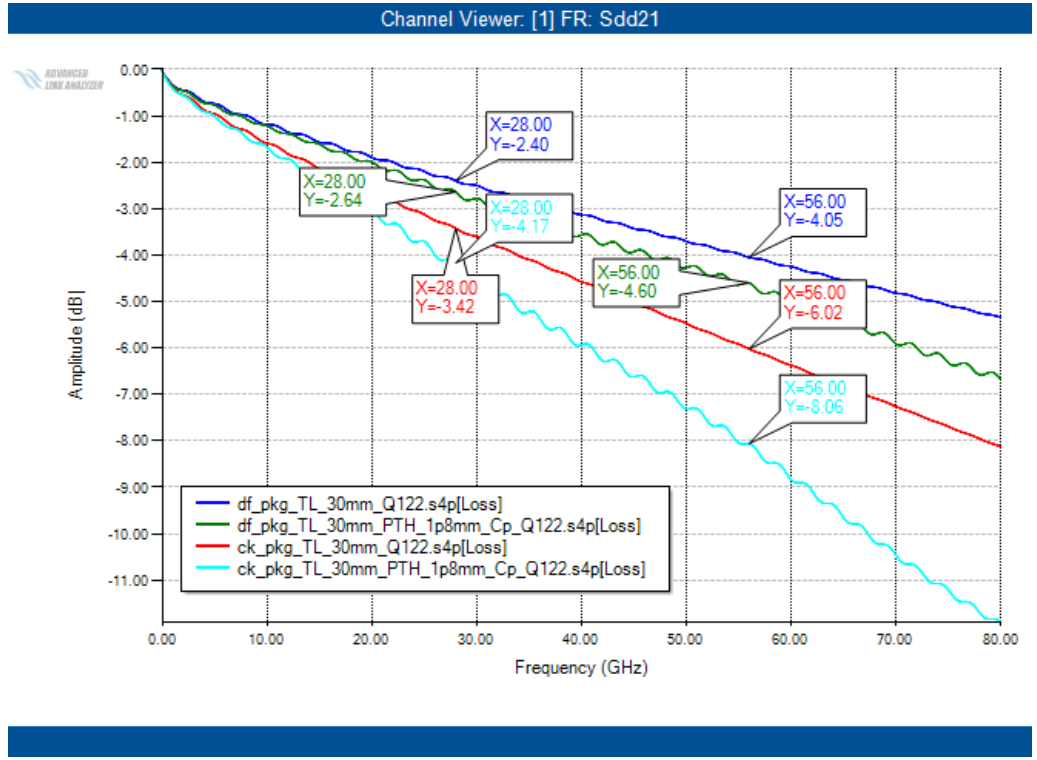
A Proposed Host Reference Package Model for 802.3df (1/2)

Parameter	112G Package T-Line Model Parameters	Proposed 224G Package T-Line Model Parameters
Z_p	30 mm	30 mm
γ_0	0 /mm	**0 /mm**
τ	6.141e-3 ns/mm	**6.141e-3 ns/mm**
a_1	9.909e-4 $ns^{1/2}$/mm	**8.9e-4 $ns^{1/2}$/mm**
a_2	2.772e-4 ns/mm	**1.55e-4 ns/mm**
Z_c	87.5 Ω	**87.5 Ω**
R_o	50 Ω	50 Ω
C_p	87 fF	**40 fF**



A Proposed Host Reference Package Model for 802.3df (2/2)

Parameter	112G Package T-Line Model Parameters	Proposed 224G Package T-Line Model Parameters
Z_p	30 mm	30 mm
γ_0	0 /mm	**0 /mm**
τ	6.141e-3 ns/mm	**6.141e-3 ns/mm**
a_1	9.909e-4 $ns^{1/2}$/mm	**8.9e-4 $ns^{1/2}$/mm**
a_2	2.772e-4 ns/mm	**1.55e-4 ns/mm**
Z_c	87.5 Ω	**87.5 Ω**
R_o	50 Ω	50 Ω
Cp	87 fF	**40 fF**



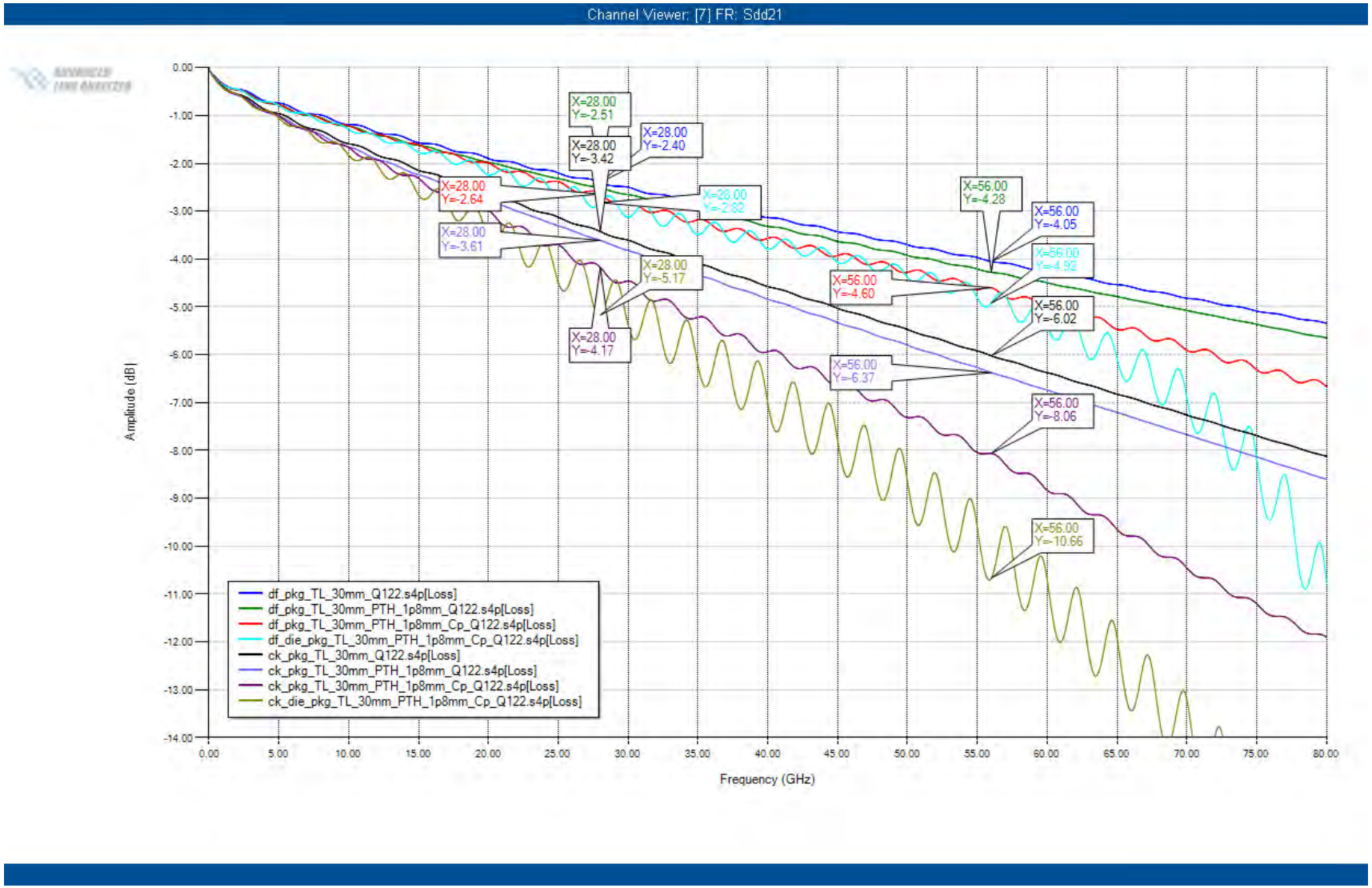
224G Pkg 30mm T-Lin

112G Pkg 30mm T-Lin

224G Pkg 30mm TL + 1.8mm PTH + Cp

112G Pkg 30mm TL + 1.8mm PTH + Cp

224G vs 112G Reference Package Model Comparison



224G Pkg 30mm T-Line

224G Pkg 30mm TL + 1.8mm PTH

224G Pkg 30mm TL + 1.8mm PTH + Cp

224G Die + Pkg 30mm TL + 1.8mm PTH + Cp

112G Pkg 30mm T-Line

112G Pkg 30mm TL + 1.8mm PTH

112G Pkg 30mm TL + 1.8mm PTH + Cp

112G Die + Pkg 30mm TL + 1.8mm PTH + Cp

References

[1] J. Kim et al, "A 224Gb/s DAC-Based PAM-4 Transmitter with 8-Tap FFE in 10nm CMOS", *ISSCC*, 2021.

[2] A. Khairi "A 1.4 pJ/b 224 Gb/s- PAM4 SERDES Receiver with 31 dB Loss Compensation ", *ISSCC*, 2022.

[3] J. Jiang et al, "Designing 224G PAM4 High Performance FPGA Package and Board with Confidence", *Designcon*, 2021.

[4] M. Li et al. "224G Package and PCB Investigations and COM Reference Model", *https://www.ieee802.org/3/df/public/22_03/li_3df_01_0322.pdf*.

Thank You!