PAMn vs Channel and FEC Investigations for 224 Gbps

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Intel

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Contents

I. 224 Gbps Modulation and Channel Characteristics

224 Gbps Modulation Scheme and Channel Characteristics

- Currently, PAM4 is used in 53 Gbps and 106 Gbps Ethernet and OIF-CEI-56G/112G
- Naturally, it is highly desired to continue using PAM4 in the 224 Gbps, considering
  - Backward compatibility
  - Electrical to optical compatibility
  - Testing methodology and equipment maturity and availability

PAM_L Modulation Considerations for 224Gbps

- To continue using PAM4 for 224Gbps implies
  - SERDES:
    - *2X symbol rate, 2X bandwidth (BW) for AFE, 2X reduction in jitter/noise spectrum density compared with 112 Gbps PAM4.*
      - Intel recent 224Gbps TC (2022) has demonstrated that those performance doubling can be achieved
  - Channel
    - *End-to-end channel (including package, break-out, PCB/cable, and connectors) performance needs to improve such that the IL at its Nyquist will be kept at the close vicinity of those for 112 Gbps.*
      - Good progresses had been made in the industry in achieving those goals.

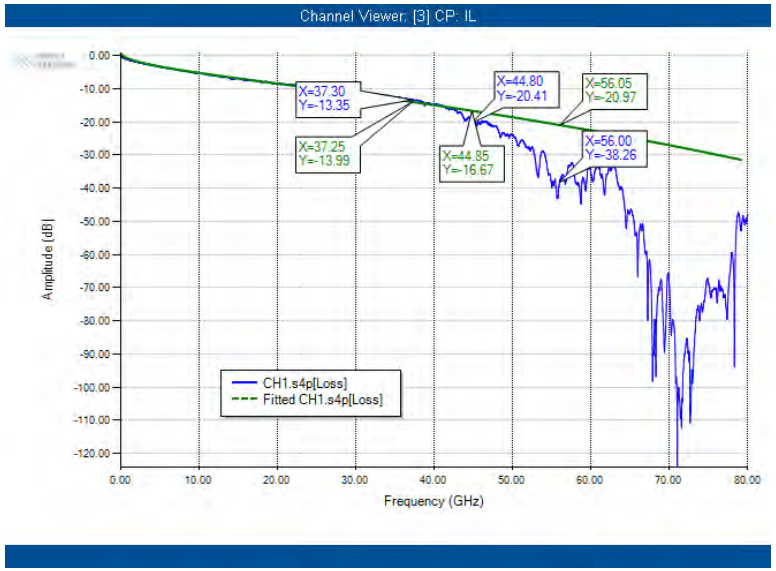
Comparisons of 224 Gbps PAM_L

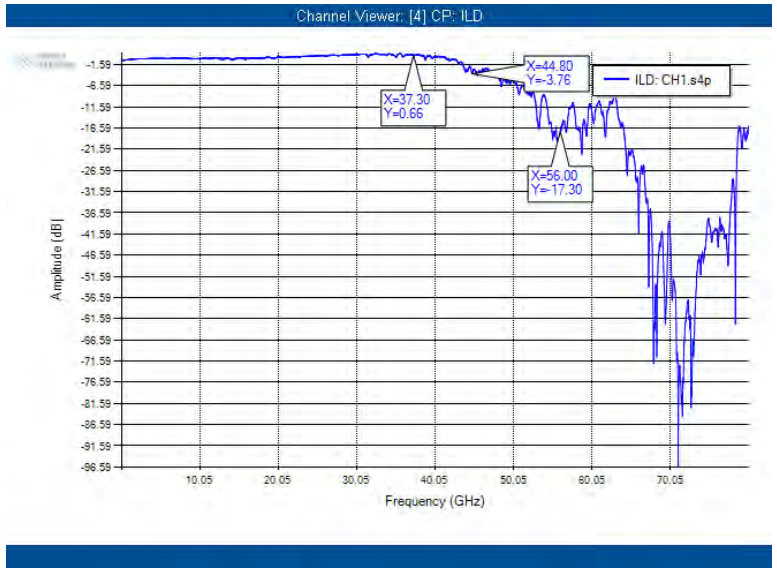
Data Ratem Gb/s	224	224	224	224	224	224
PAMn Levels	4	5	6	7	8	16
Bit per symbol	2.00	2.32	2.58	2.81	3.00	4.00
Symboe Rate (GS/s)	112.00	96.47	86.66	79.79	74.67	56.00
UI (ps)	8.93	10.37	11.54	12.53	13.39	17.86
Nyquist Freq	56.00	48.24	43.33	39.90	37.33	28.00
SNR Delta	0.00	-2.50	-4.44	-6.02	-7.36	-13.98

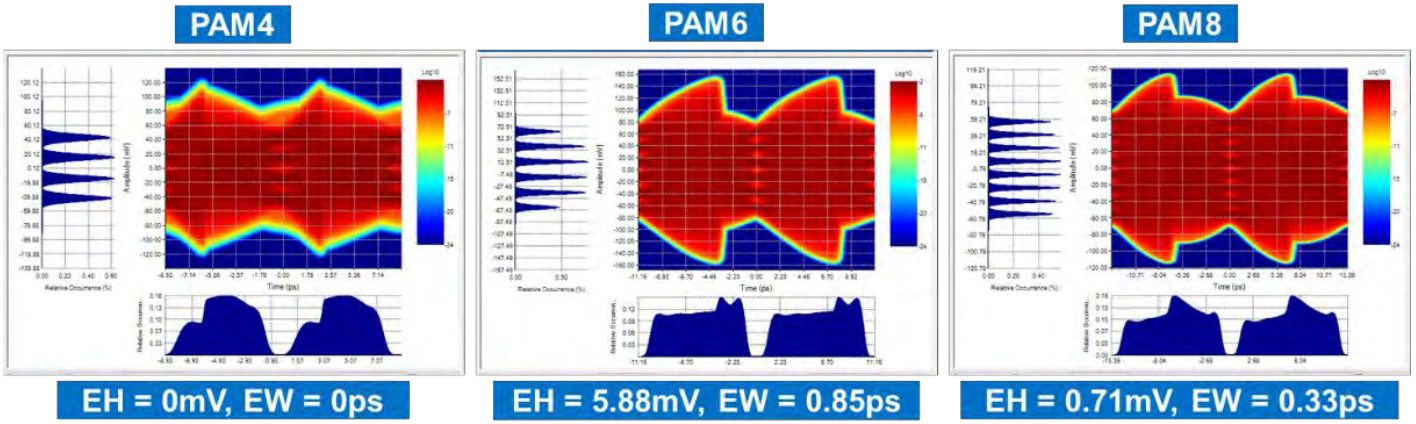
Simulation Die and Package Considerations

- Die model and characteristics are based on Intel 224Gbps test chips (e.g., [1], [2]).
- Package model and characteristics are aligned with industry RM and Intel package projection at 2024-2025 (e.g., [3]).

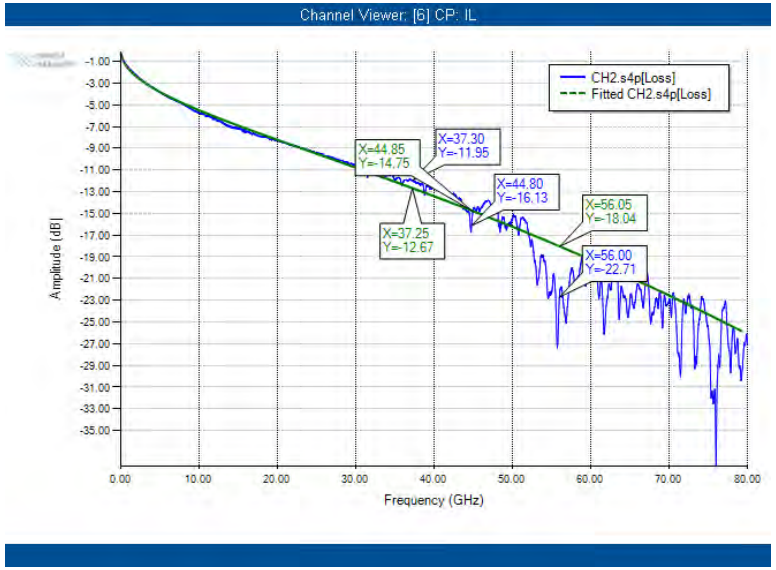
PAM_L and Channel Investigations – Channel #1

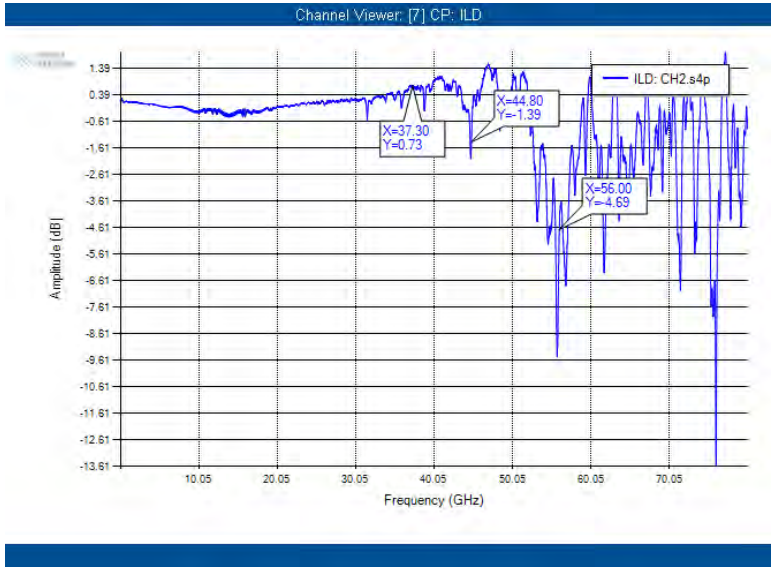


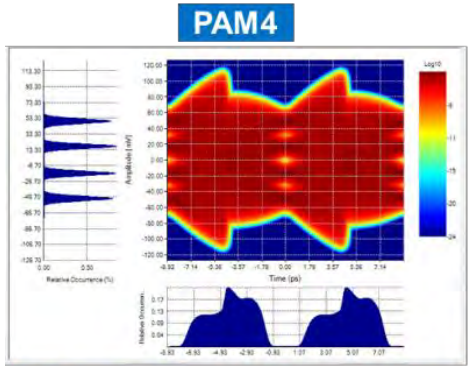




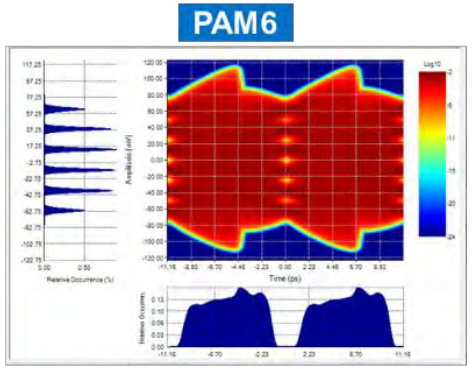
PAM_L and Channel Investigations – Channel #2



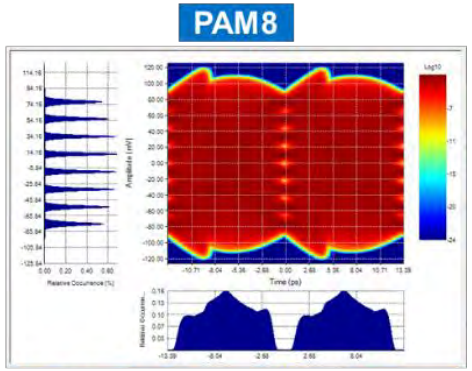




EH = 12.85mV, EW = 1.54ps

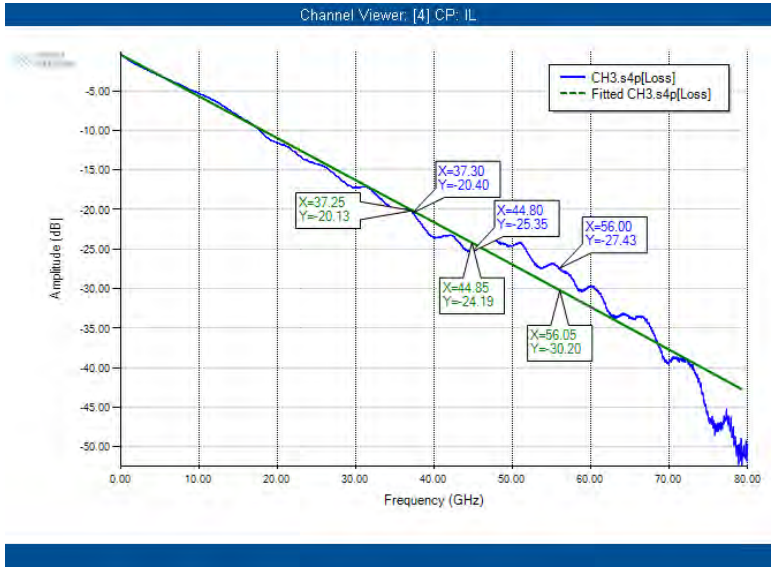


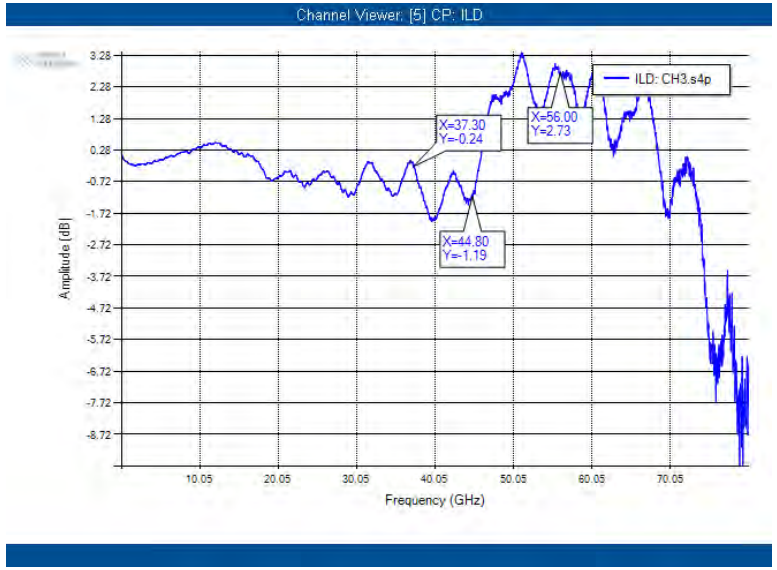
EH = 9.58mV, EW = 1.66ps

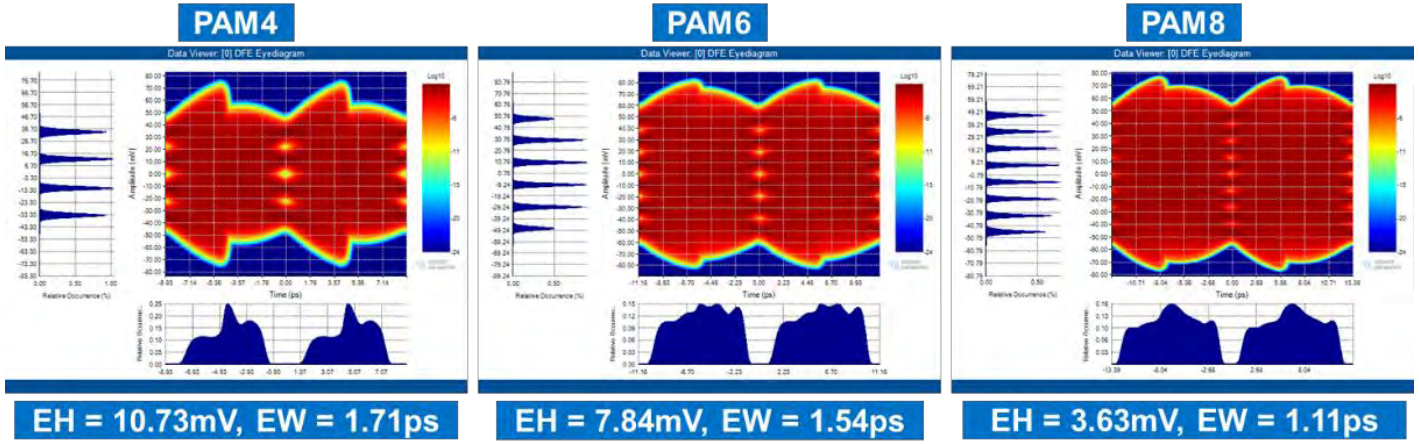


EH = 7.37mV, EW = 1.23ps

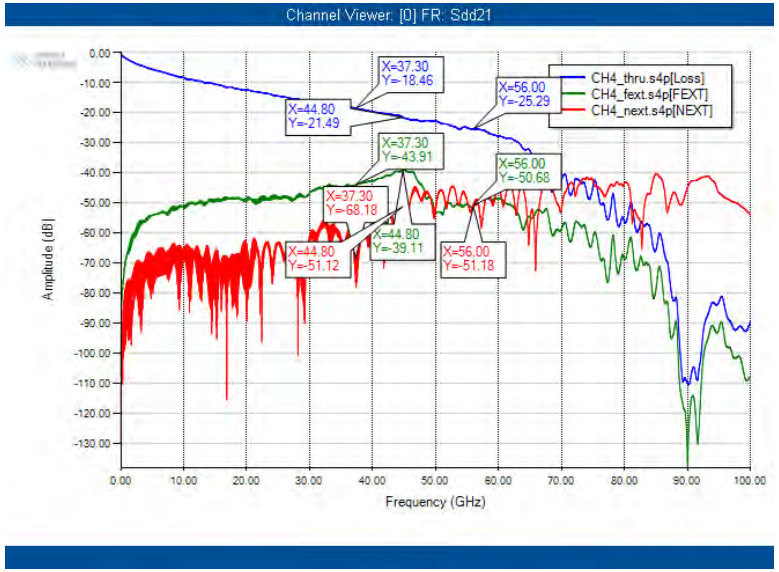
PAM_L and Channel Investigations – Channel #3

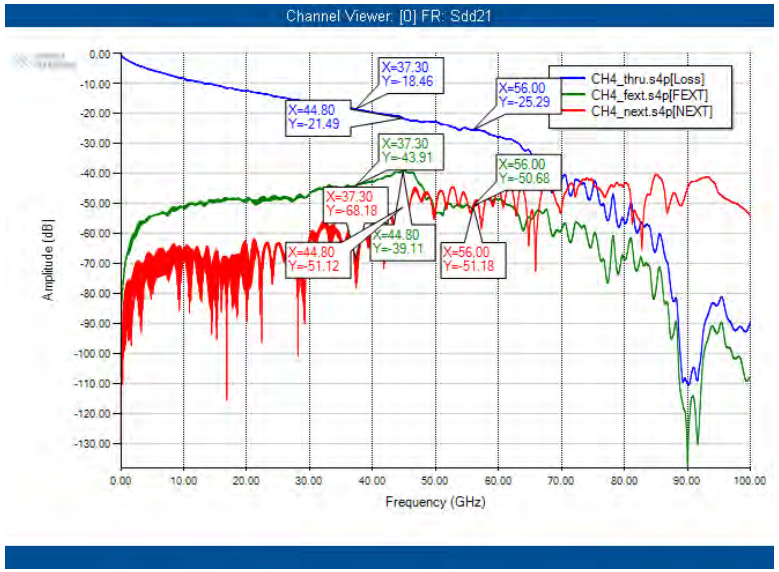




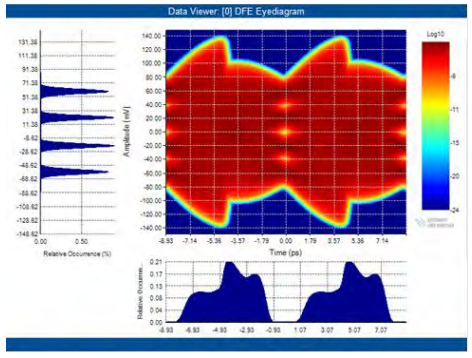


PAM_L and Channel Investigations – Channel #4 [4]



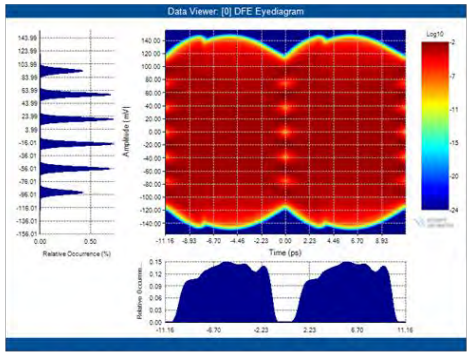


PAM4



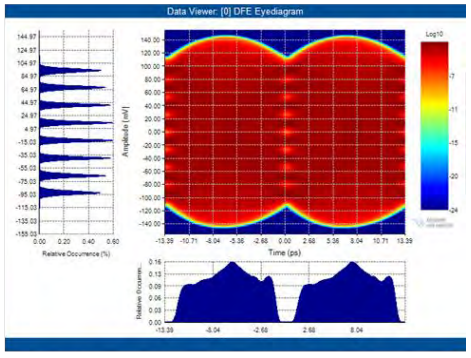
EH = 15.37mV, EW = 1.34ps

PAM6



EH = 13.09mV, EW = 1.35ps

PAM8



EH = 6.96mV, EW = 1.13ps

PAM_L and Channel Investigations -- Summary

Channel	PAM4		PAM6		PAM8	
	IL/ILD/ICN @56GHz	EH/EW @10^{-4}	IL/ILD/ICN @44.8GHz	EH/EW @10^{-4}	IL/ILD/ICN @37.3GHz	EH/EW @10^{-4}
CH #1	38dB/17dB/0mV	0mV/0ps	20dB/4dB/0mV	5.88mV/0.85ps	13dB/1dB/0mV	0.71mV/0.33ps
CH #2	23dB/7dB/0mV	12.85mV/1.54ps	16dB/1dB/0mV	9.58mV/1.66ps	12dB/1dB/0mV	7.37mV/1.23ps
CH #3	27dB/3dB/0mV	10.73mV/1.71ps	24dB/1dB/0mV	7.84mV/1.54ps	20/0dB/0mV	3.63mV/1.11ps
CH #4	25dB/1dB/1.09mV	15.37mV/1.34ps	22dB/1dB/0.99mV	13.09mV/1.35ps	19dB/1dB/0.93mV	6.96mV/1.13ps

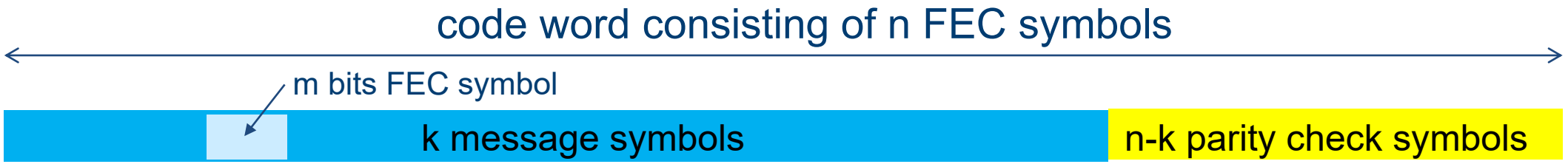
Conclusions

- It is clear that the optimal modulation critically depends on the channel performance and characteristics.
- Simulations have shown that with reasonable channel IL (i.e.,~30dB IL, and ≤3dB ILD, at the PAM4 Nyquist), and a transceiver design (die and package) that works well at PAM4 rate, PAM4 would out-perform PAM_L, where L > 4.

II. 224 Gbps Modulation and FEC

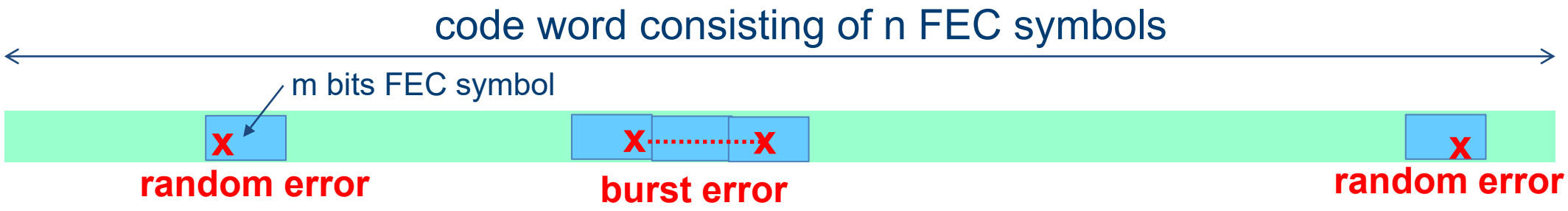
Reed-Solomon FEC: RS(n,k,t) over GF(2^m)

- **Structure**
  - FEC code word consists of n FEC symbols
    - *n = (k message symbols) + (n-k) parity symbols*
  - Each FEC symbol consists of m bits
- **Error Correction Capability**
  - Can correct up to t = (n-k)/2 FEC symbol errors



PAM_L Random Error and Burst Error on FEC

- **Random Error of Modulation Symbol**
  - Each error likely causes one FEC symbol error
    - Probability of random error is of our concern
- **Burst Error of Modulation Symbol**
  - One burst error can cause multiple FEC symbol errors
    - Probability of burst error and its length is of our concern
      - e.g. 6-UI long burst errors cause 2 FEC symbol errors with PAM4, but may cause 3 FEC symbol errors with PAM6

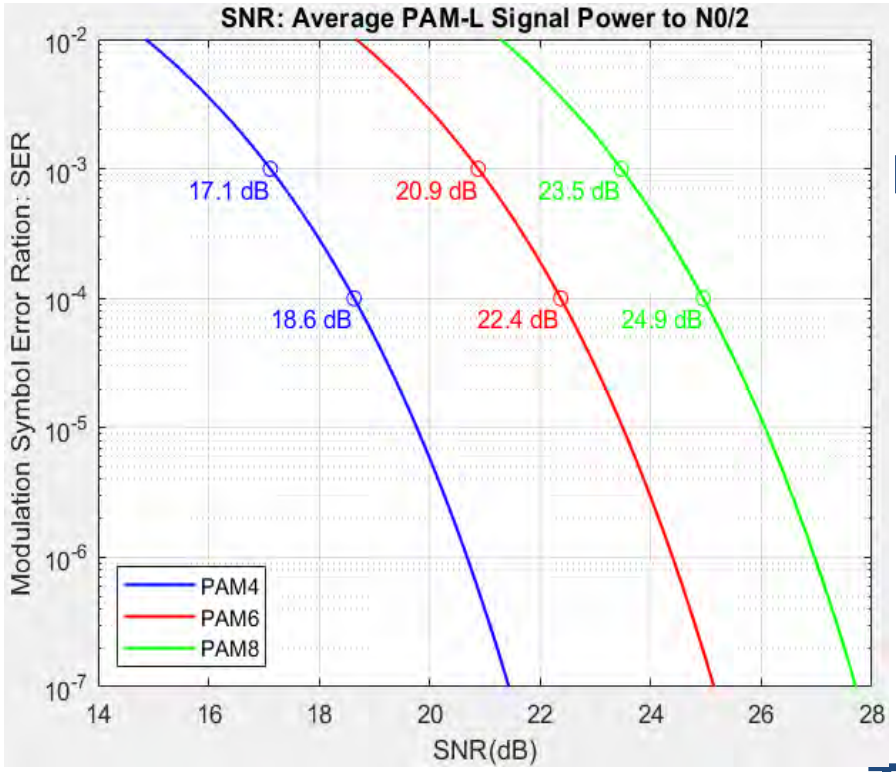


RS(n,k,t) over GF(2^m) with PAM_L

- **Each PAM_L modulation symbol (1 UI) carries $\log_2(L)$ bits**
  - PAM_L UIs required to send each FEC symbol summarized in the table below
    - *PAM_2 (NRZ) uses 10 UIs, PAM_4 uses 5 UIs, …*
  - FEC with higher order PAM_L would suffer more from burst error
    - *As discussed in the previous slide and the table below*

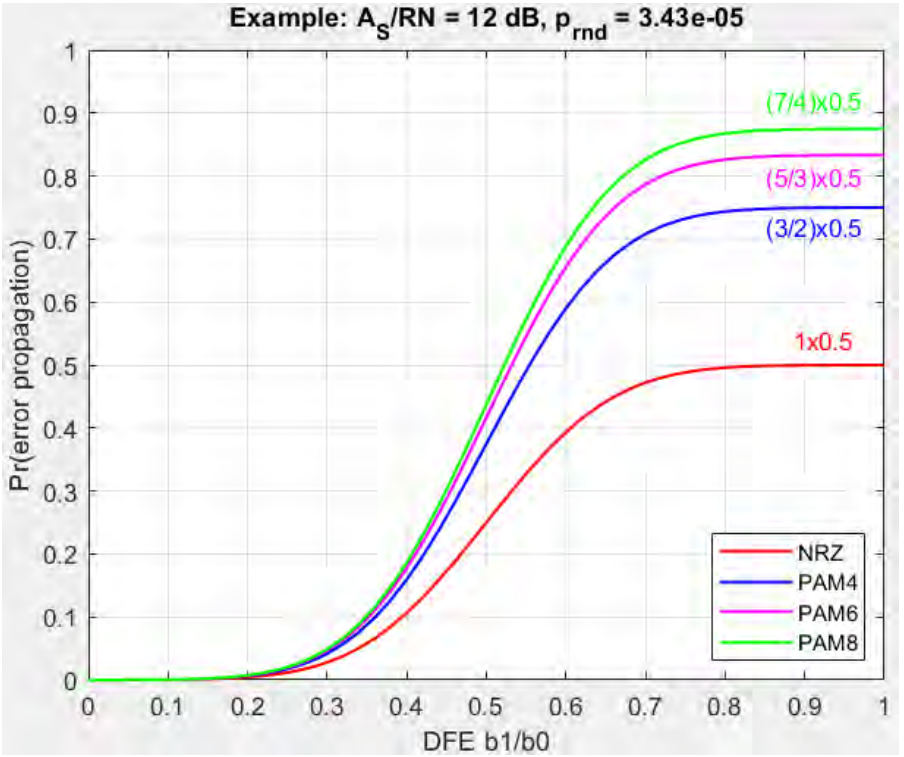
PAM_L	$\log_2(L)$	Mod_Symb/FEC_Symb
2	1	10
4	2	5
6	2.58 ≈ 2.5	4
8	3	3.33 ≈ 4

Error Probabilities and FEC Performance



Random Error Probability

Burst Error Probability



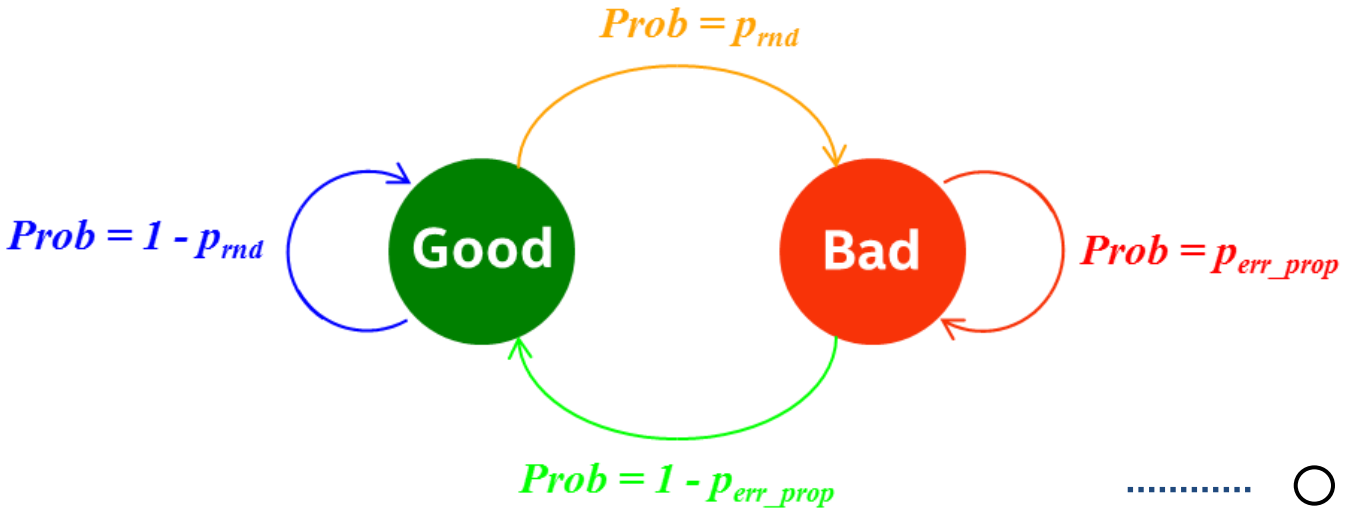
Two-State Error Model

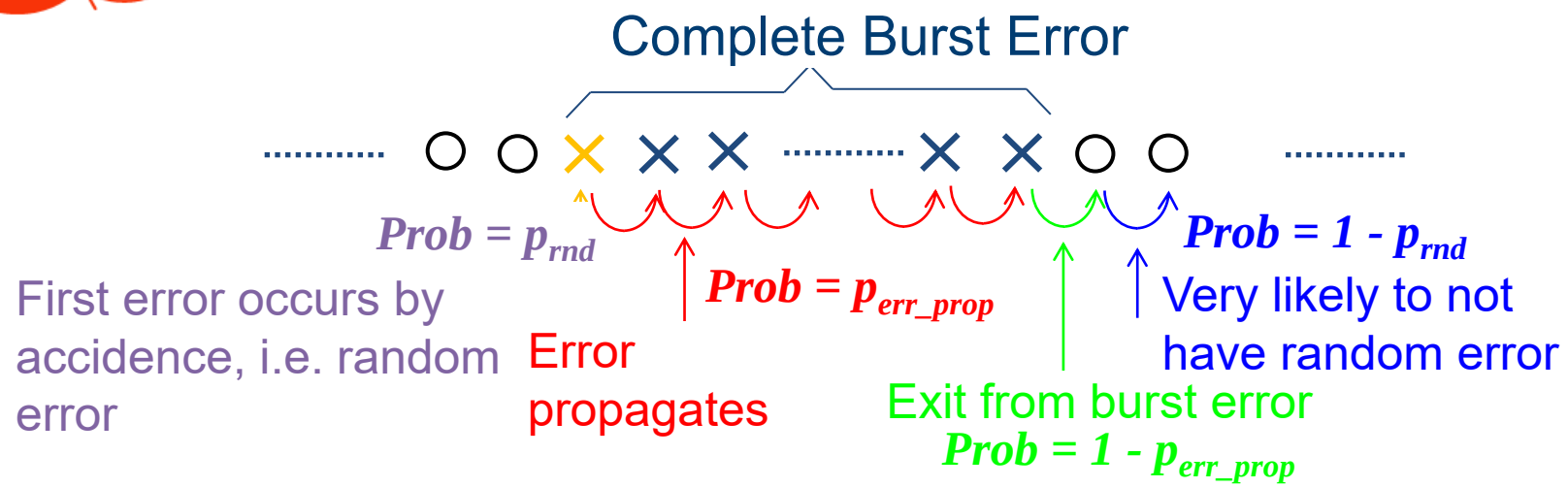
FEC Performance Model
(pre-FEC BER vs. post-FEC FER)

discussed in the following slides

Two-State Error Model

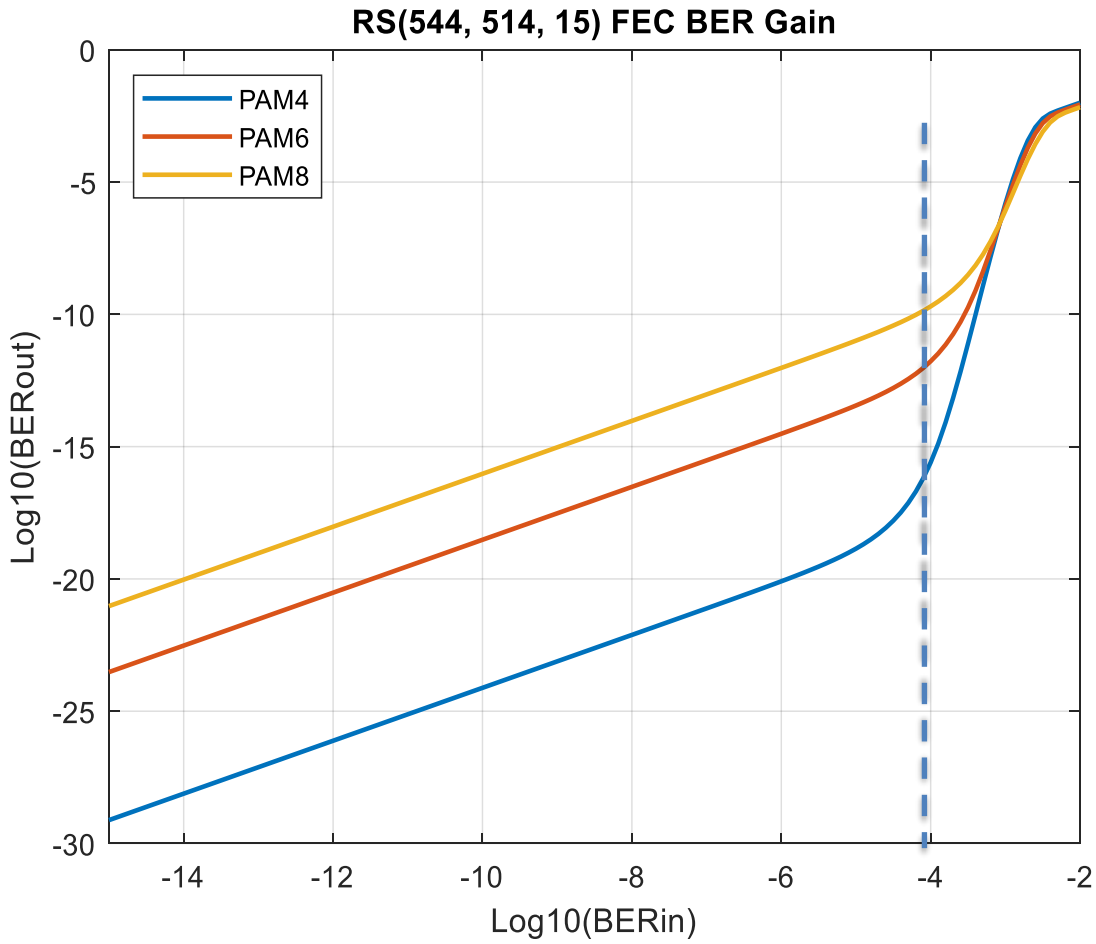
- **Simple and Frequently Used Error Model**
  - Burst error triggered by random error, and cased by error propagation





Example KP FEC Performance vs. PAM-4/6/8

- FEC performance model
  - Obtained by combining FEC structure and two-state error model
- If max pre-FEC BER is 10^{-4}
  - PAM4 can achieve post-FEC BER < 10^{-15}
  - PAM6 and PAM8 would require stronger FEC to achieve post-FEC BER < 10^{-15}

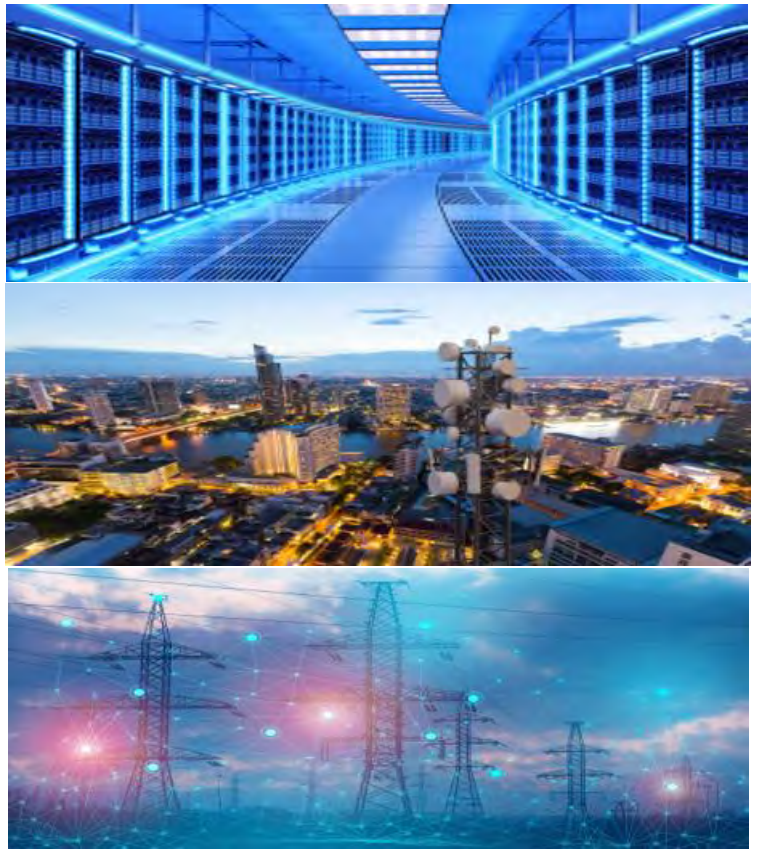


III. 224 Gbps Transceiver Development and Characteristics

Intel 224 Gbps-PAM4-LR Transceiver Highlights ([1],[2])

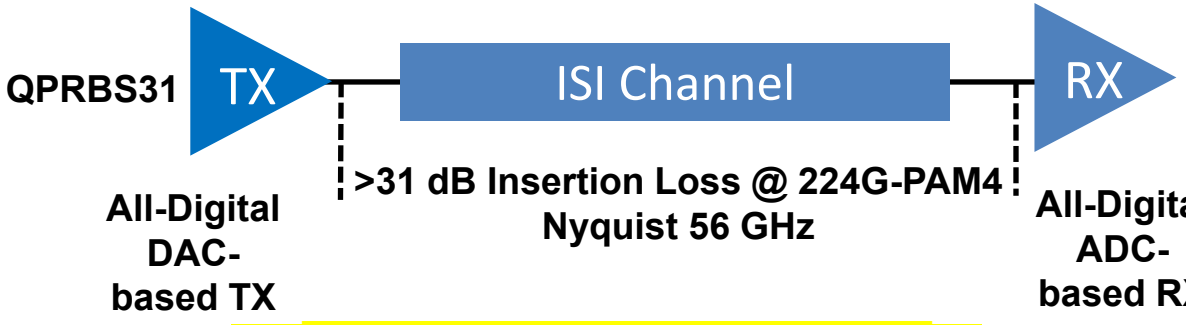
- **~2X** TX/RX data path bandwidth and sampling rate increase
- **~ 2X** jitter and noise reduction
- **~2X** power reduction per bit

compared with 112 Gbps-PAM4 generation

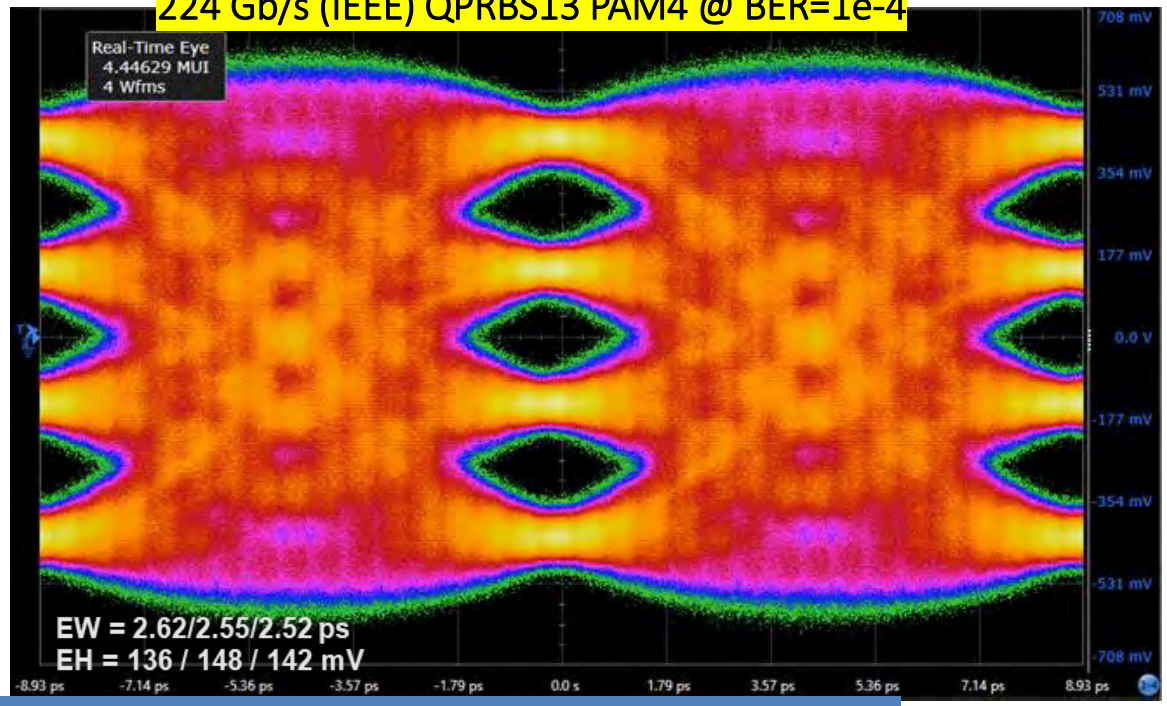


224 Gbps-PAM4-LR Transceiver Test Chip

- Solid full-link transmitter and receiver performance demonstrated on the test chip
  - For TX measurement, eye diagram measured on an oscilloscope
  - For RX BER measurement, TX on one test chip transmits to RX on another test chip through a > 31 dB channel

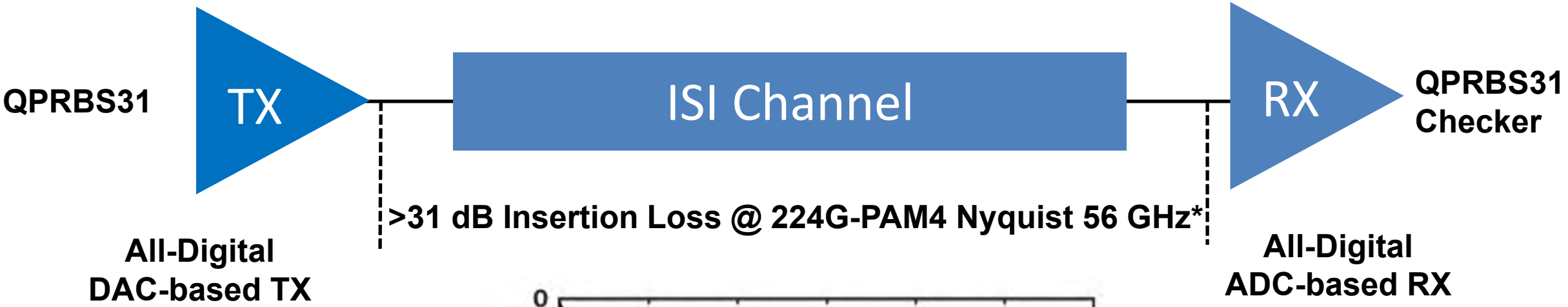


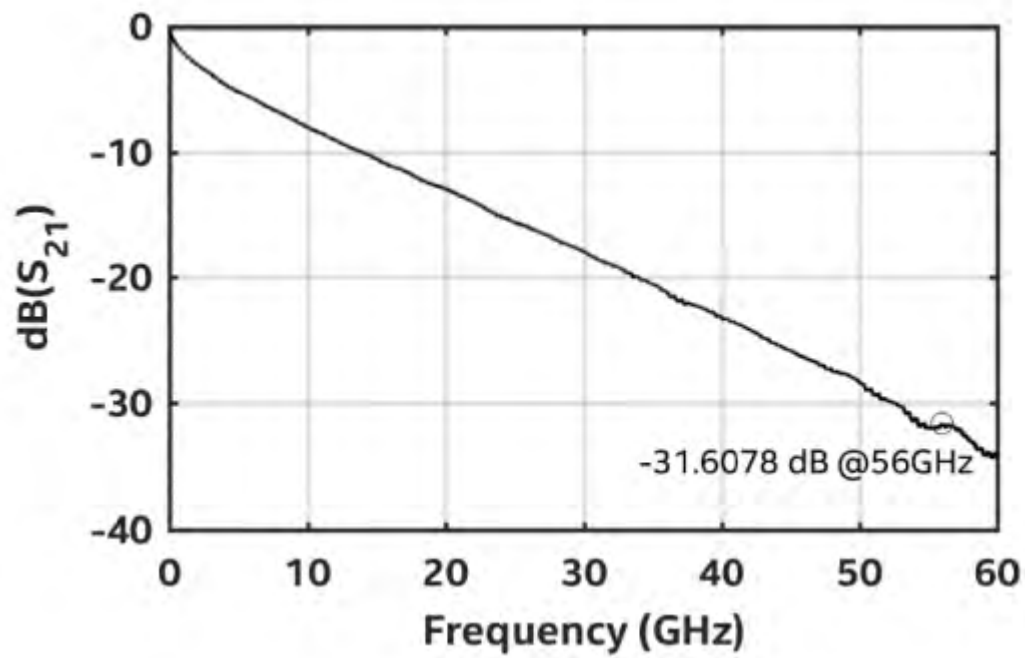
224 Gb/s (IEEE) QPRBS13 PAM4 @ BER=1e-4



World's first 224 Gbps-PAM4-LR Transceiver Test Chip

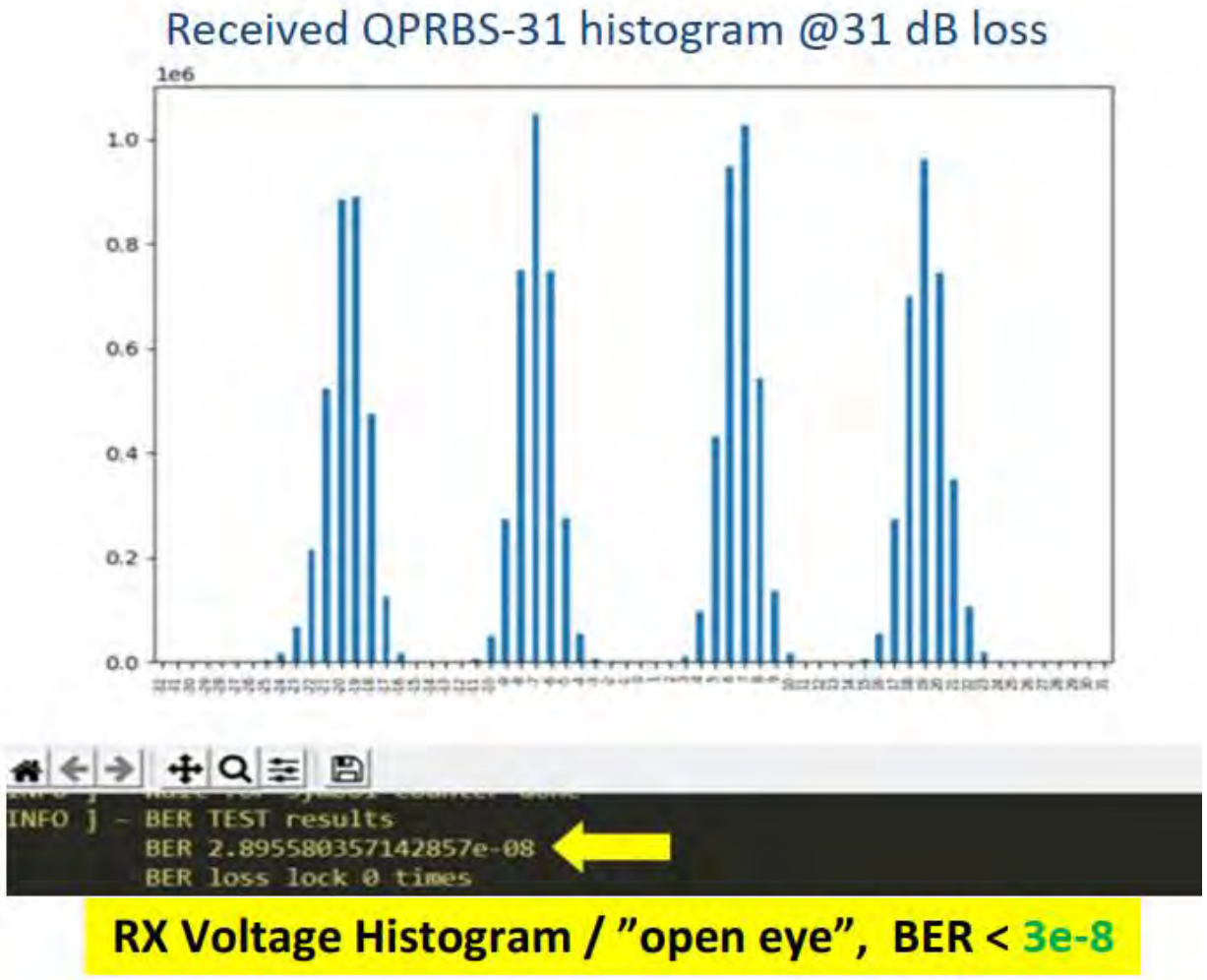
224 Gbps Test Channel





* Measured bump to bump

PAM4 224 Gbps Full System Measurement Results (> 31 dB Insertion Loss @ Nyquist 56 GHz)



IV. Summary and Conclusions

- Our investigations and considerations of backward, optical modulation, FEC compatibility, and broad market potential, suggest that PAM4 remains to be the optimal/common modulation for various reaches, C2M (VSR), C2C (MR), and CR (LR), for 224 Gbps electrical I/Os, where BGA-to-BGA channel IL is ~30 dB or less at PAM4 Nyquist.

References:

[1] J. Kim et al, “A 224Gb/s DAC-Based PAM-4 Transmitter with 8-Tap FFE in 10nm CMOS”, *ISSCC*, 2021.

[2] A. Khairi “A 1.4 pJ/b 224 Gb/s- PAM4 SERDES Receiver with 31 dB Loss Compensation“, *ISSCC*, 2022.

[3] J. Jiang et al, “Designing 224G PAM4 High Performance FPGA Package and Board with Confidence”, *Designcon*, 2021.

[4] 1 meter TP1-TP4 CR Channel from OSFP (hosted by Amphenol).

Thank You!