An Investigation of a Direct Attach Copper Cable (DAC) Assembly Channel Simulation

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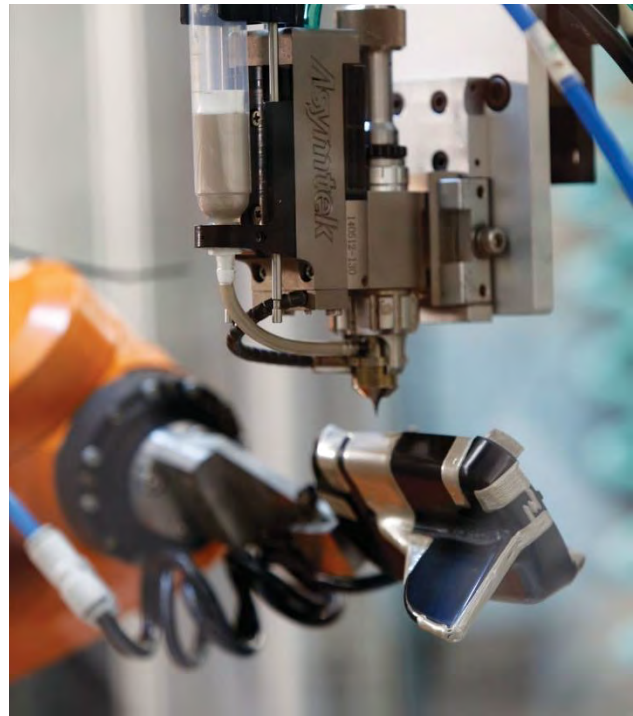
3/22/22
EVERY CONNECTION COUNTS



Overview

A preliminary investigation of a passive copper cable assembly concept channel is presented to help guide P802.3df architecture discussions. Development work is on-going, and updates are expected.

Further detail, refinement and optionality is anticipated in future contributions

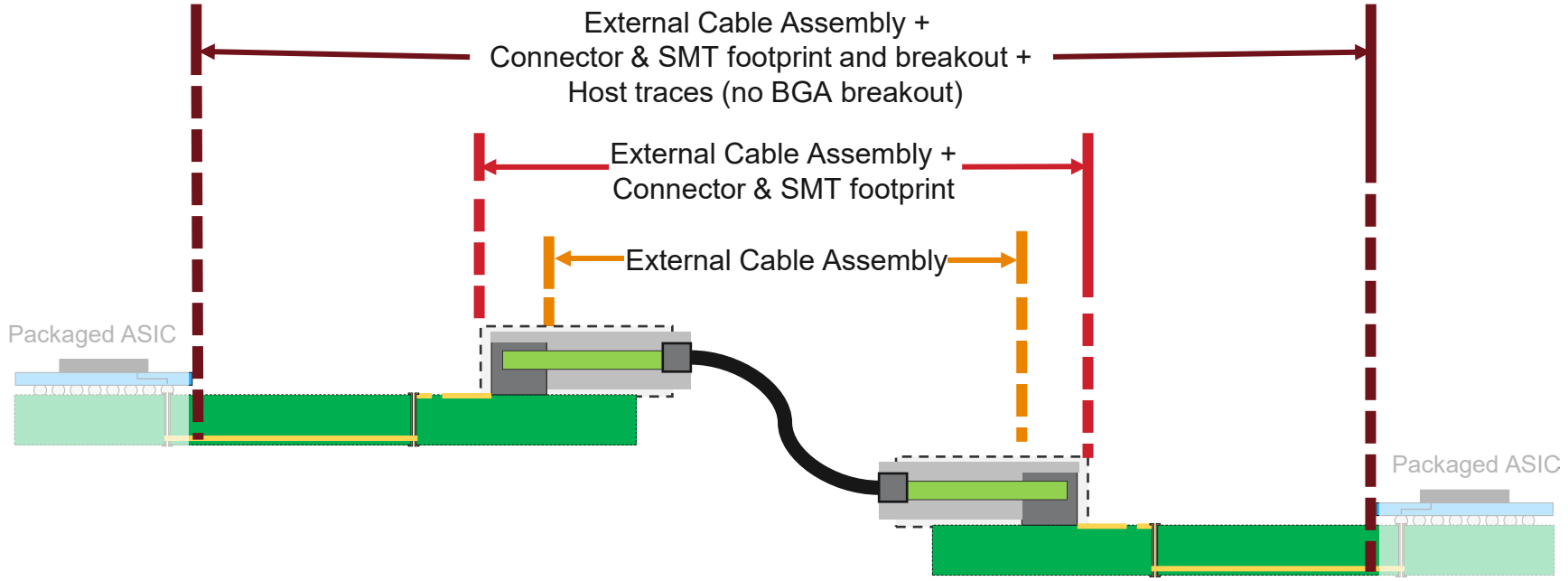
This is not intended to be a final position on a copper cable assembly channel performance

The intent of this presentation is to provide directional input at this early stage of the project

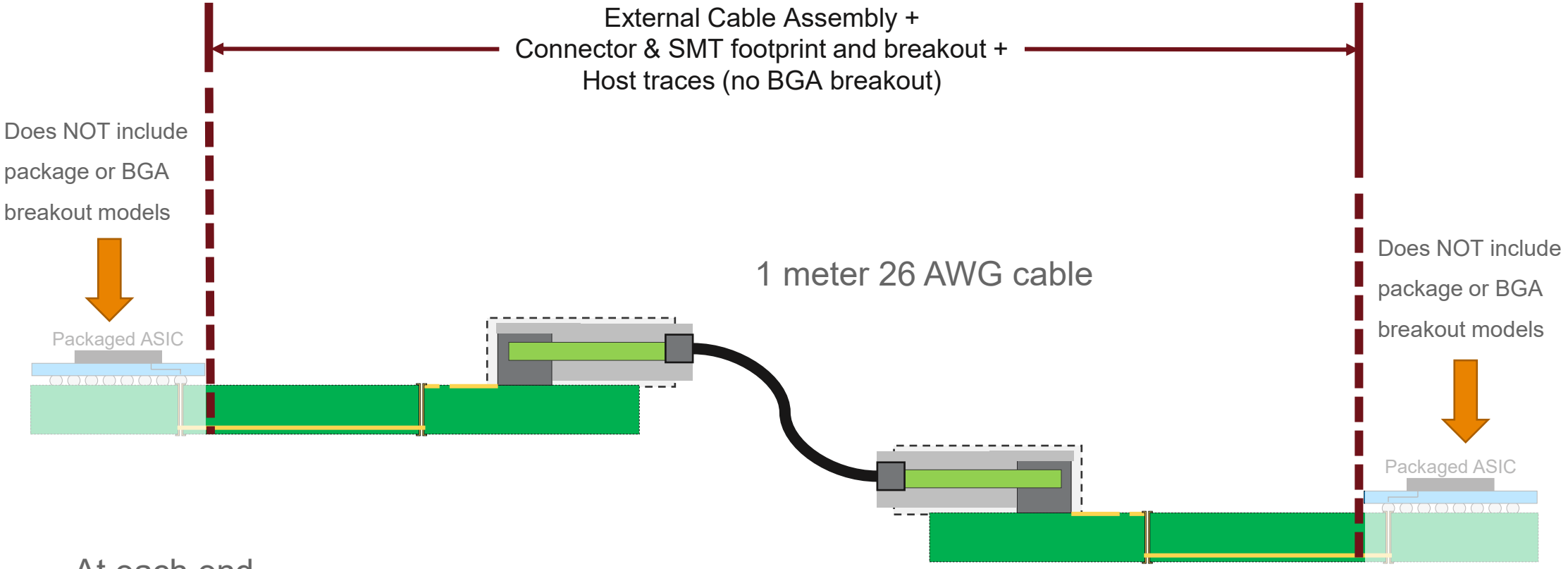
Additional development is in process on connector, bulk cable, wire termination and cable assembly PCB designs

Description

- Simulation for 200G concept connector and cable assembly with host loss
- No silicon package
- No BGA escape. Recommend that BGA escape simulations are contributed for comparative channel evaluations
- Current view of passive cable assembly performance
- What this presentation is NOT:
  - Modulation proposal
  - Host architecture proposal options, i.e. traces vs. cabled host to “near ASIC” vs. co-package copper
  - Asymmetric architectures (managed deployment)



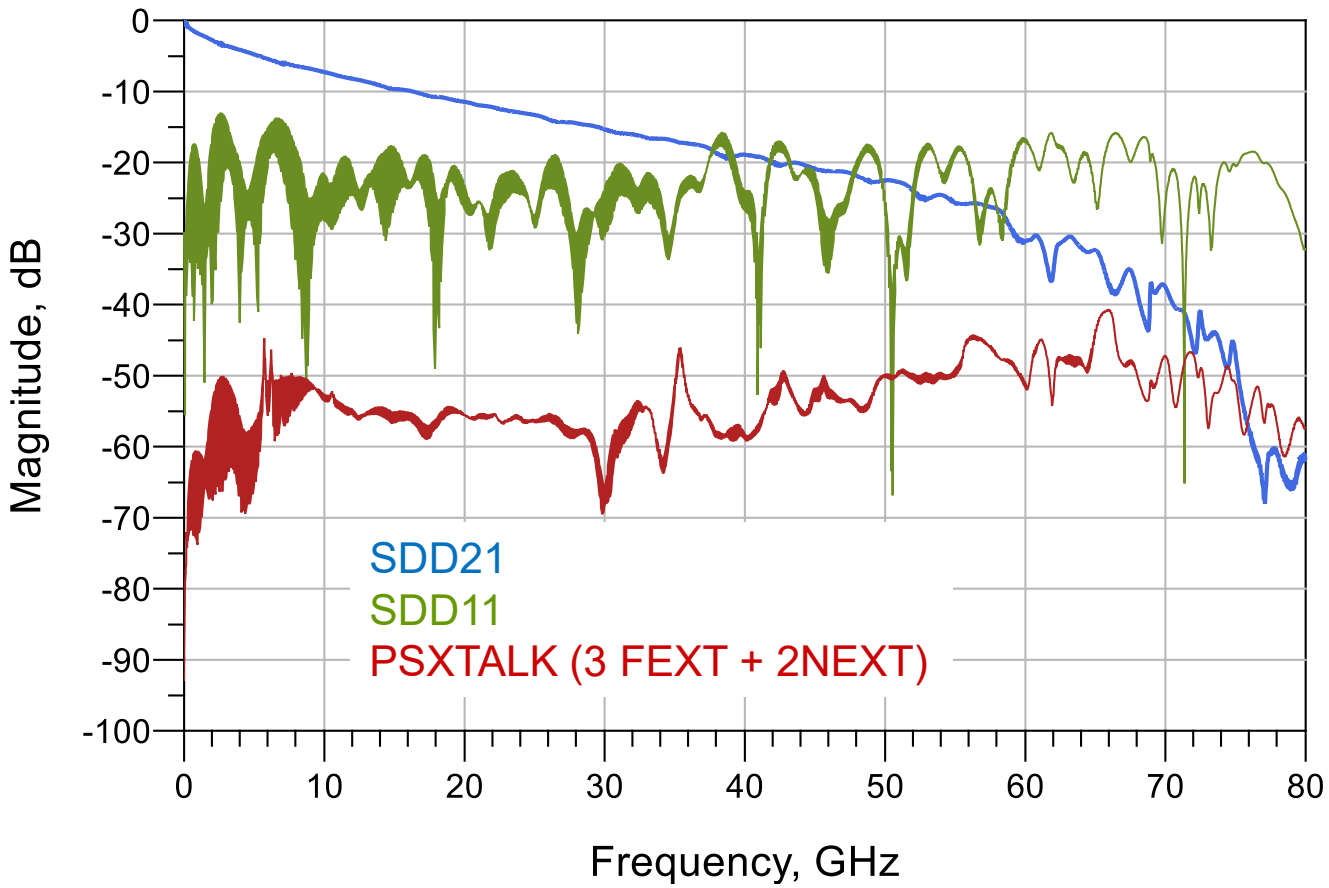
System Topology



At each end,

- OSFP 200G Connector
- Host SMT Footprint
- Host Transition Vias and Conn Breakout
- Host Trace Loss = 5dB @ 53.125 Ghz
- NO BGA BREAKOUT

Channel Performance (No BGA breakout included)



Parameters	@ 42.5 GHz PAM-6	@ 53.125 GHz PAM-4
Insertion Loss	20.36	25.17
Return Loss	17.58	17.81
Power Sum Crosstalk	50.76	50.93

Test Case	Channel IL @ 53.125GHz	Channel + PKG IL @ 53.125GHz	COM	ERL
1	25.17	30.27	4.7	17.81
2	25.17	31.8	4.54	17.81
3	25.17	35.63	3.58	17.81
4	25.17	37.68	3.05	17.81

Note that ERL/COM results do not capture impact of BGA breakout

Upper → G S S G L L L L G S S G S S G
Lower → G S S G L L L L G S S G S S G

G: ground contact
S: high speed contact
L: low speed contact
□ : Victim pair

Script: COM_370BetaL
Config File on Slide 6

COM Config File

This is just a starting point config file used for this study. It is not a proposal or recommendation.

Table 93A-1 parameters			2
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ; 0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[.12 .15 .14; .12 .15 .14]	nH	[TX RX]
C_b	[.3e-4 .3e-4]	nF	[TX RX]
z_p select	[1 2 3 4]		[test cases to run]
z_p (TX)	[11 15 26 31; 1.0 1.0 1.0 1.0]	mm	[test cases]
z_p (NEXT)	[9 15 24 29; 1.0 1.0 1.0 1.0]	mm	[test cases]
z_p (FEXT)	[11 15 26 31; 1.0 1.0 1.0 1.0]	mm	[test cases]
z_p (RX)	[9 15 24 29; 1.0 1.0 1.0 1.0]	mm	[test cases]
C_p	[0.4e-4 0.4e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[50 50]	Ohm	[TX RX]
A_v	0.413	V	
A_fe	0.413	V	
A_ne	0.608	V	
L	4		
M	32		
filter and Eq			
f_r	0.5	*fb	
c(0)	0.55		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.2]		[min:step:max]
c(-3)	[-0.1:0.02: 0]		[min:step:max]
c(1)	[-0.1:0.02:0]		[min:step:max]
N_b	12	UI	
b_max(1)	0.9		
b_max(2..N_b)	0.3		
b_min(1)	-0.85		
b_min(2..N_b)	-0.3		
g_DC	[-20:1:0]	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-8:1:0]		[min:step:max]
f_HP_PZ	1.0625	GHz	

I/O control		
DIAGNOSTICS	1	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	1	logical
RESULT_DIR	.\results\200G_kR_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	R200_eval	
COM_CONTRIBUTION	0	logical
Operational		
COM Pass threshold	3	dB
ERL Pass threshold	10.5	dB
DER_0	7.00E-04	
T_r	2.50E-03	ns
FORCE_TR	1	logical
Local Search	2	
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	logical
TR_TDR	0.01	ns
N	6000	
beta_x	0	
rho_x	0.618	
fixture delay time	[0 0]	[port1 port2]
TDR_W_TXPKG	0	
N_bx	36	UI
Z_t	50	ohm
Receiver testing		
RX_CALIBRATION	0	logical
Sigma BBN step	5.00E-03	V
Noise, jitter		
sigma_RJ	0.01	UI
A_DD	0.02	UI
eta_0	2.10E-09	V^2/GHz
SNR_TX	34	dB
R_LM	0.95	

Table 93A–3 parameters		
Parameter	Setting	Units
package_tl_gamma0_a1_a2	[0 0.0009909 0.0002772]	
package_tl_tau	6.14E-03	ns/mm
package_Z_c	[87.5 87.5 ; 92.5 92.5]	Ohm
Table 92–12 parameters		
Parameter	**Setting**	
board_tl_gamma0_a1_a2	[0 6.44084e-4 3.6036e-05]	1.5 dbpi at 56G
board_tl_tau	0.00579	ns/mm
board_Z_c	100	Ohm
z_bp (TX)	50	mm
z_bp (NEXT)	50	mm
z_bp (FEXT)	50	mm
z_bp (RX)	50	mm
C_0	[0.2e-4]	nF
C_1	[0.1e-4]	nF
Include PCB	0	**logical**
Floating Tap Control		
N_bg	4	0 1 2 or 3 groups
N_bf	6	taps per group
N_f	80	UI span for floating taps
bmaxg	0.2	max DFE value for floating taps
B_float_RSS_MAX	0.2	rss tail tap limit
N_tail_start	25	(UI) start of tail taps limit
ICN parameters		
f_v	0.890	*Fb
f_f	5*4	*Fb
f_n	5*4	*Fb
f_2	53.125	GHz
A_ft	0.600	V
A_nt	**0.600**	V
Dynamic TXFFE	1	
FloatingDFE_Development	1	

Summary

- Simulation results have been provided for a 200G channel consisting of:
  - 1m DAC 200G concept cable assembly
  - OSFP 200G concept connector (x 2)
  - Host connector footprint and via (x 2)
  - 5 dB of host loss @53.125 Ghz (x 2)
- Not a final position on performance, on-going work, additional optional implementations anticipated
- No position has been taken on modulation scheme for CR applications
- Intent is to provide guidance input for 802.3df architecture discussions