Proposed 800G LR4 Baseline with PAM4 IMDD

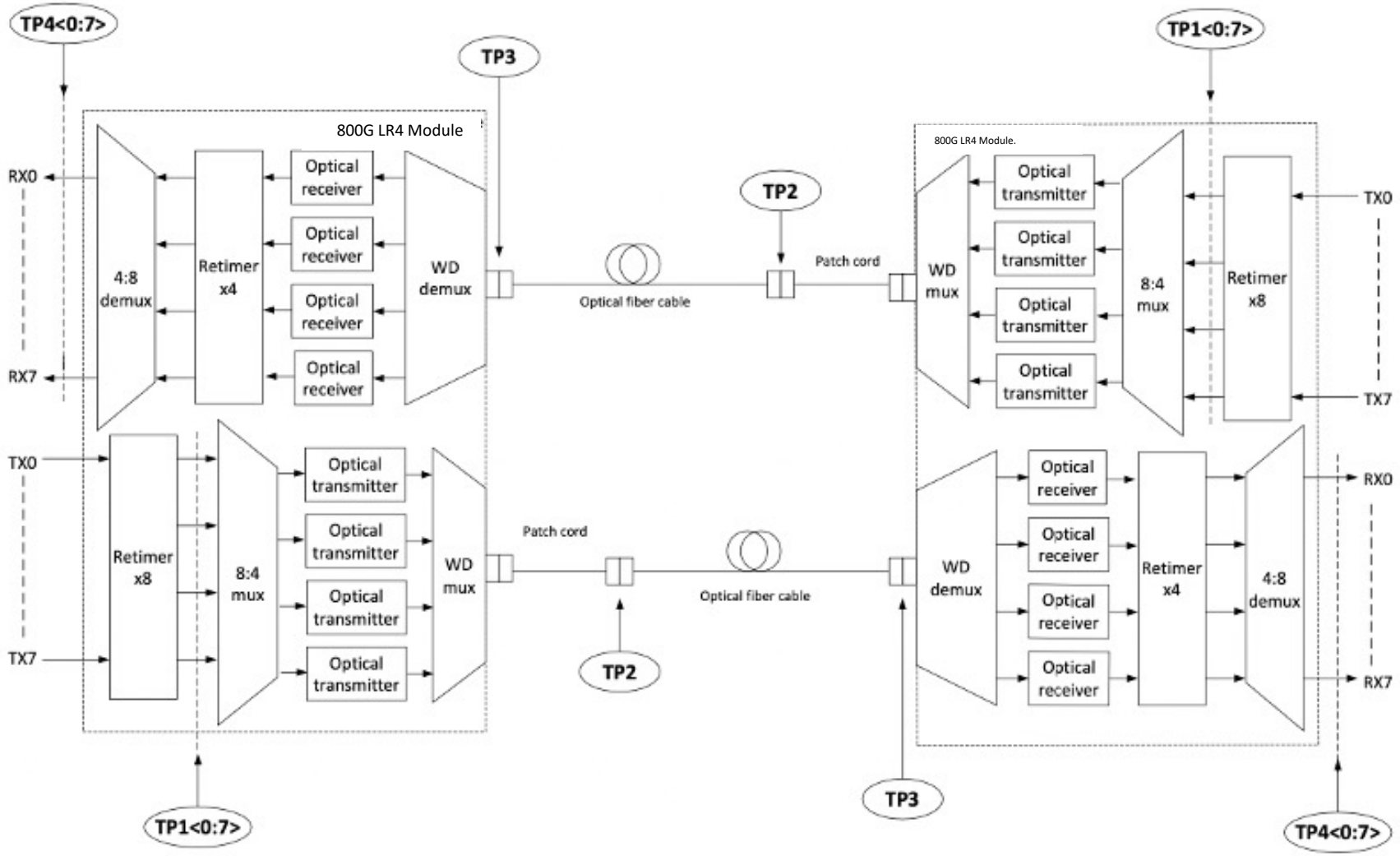
Rang-Chen (Ryan) Yu, SiFotonics
Frank Chang, Source Photonics

March 29, 2022
IEEE P802.3df

Supporters

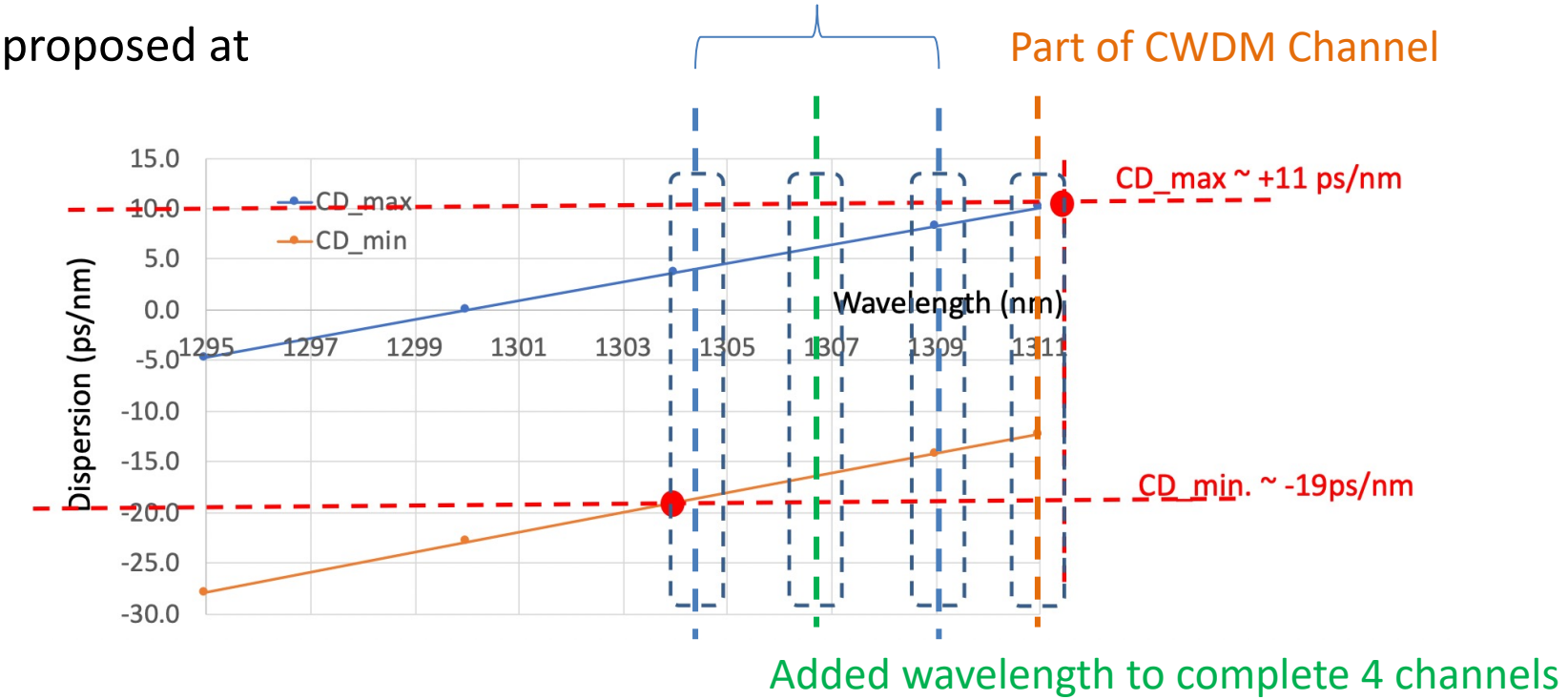
- Chongjin Xie, Alibaba
- Ed Uldrichs, Intel
- Eric Bernier, Huawei
- Guangquan Wang, China Unicom
- Han Li, China Mobile
- Hao Liu, China Telecom
- Guangcan Mi, Huawei
- Jianwei Mu, HiSense
- Jinghui Li, TFC
- Kohichi Tamura, CIG
- Natarajan Ramachandran, Broadcom
- Phil Sun, Credo
- Roberto Rodes, II-VI
- Shikui Shen, China Unicom
- Vasudevan Parthasarathy, Broadcom
- Vipul Bhatt, II-VI
- Xi Wang, Marvel
- Xiang Liu, Huawei
- Xue Wang, H3C
- Zhan Su, ZTE

800G LR4 Transceiver Block Diagram



800G LR4 Proposal Discussions

- Technical Feasibility of 800G LR4 with PAM4 IMDD discussed with a B400G Study group contribution [yu_b400g_01b_210819.pdf]
- 800G LR4 Technical feasibility Proposed
  - Channel wavelength plan proposed at
    - L0=1304.58nm
    - L1=1306.85nm
    - L2=1309.14 nm
    - L3=1311.43nm
  - CD tolerance levels
    - Max. +11ps/nm
    - Min. -19ps/nm



- FWM penalty had been raised as a consideration
- In this contribution, we proposed a baseline for 800G LR4 with adjusted Tx and Rx specifications

FWM Penalty Discussions

From John Johnson (johnson_3ca_1_0716)

FWM frequency:

$$f_{ijk} = f_i + f_j - f_k$$

FWM power:

$$P_{ijk} = \left(\frac{D_{ijk}}{3}\gamma L\right)^2 P_i P_j P_k e^{-\alpha L}\eta \text{ , where } \gamma = \frac{2\pi n_2}{\lambda A_e}$$

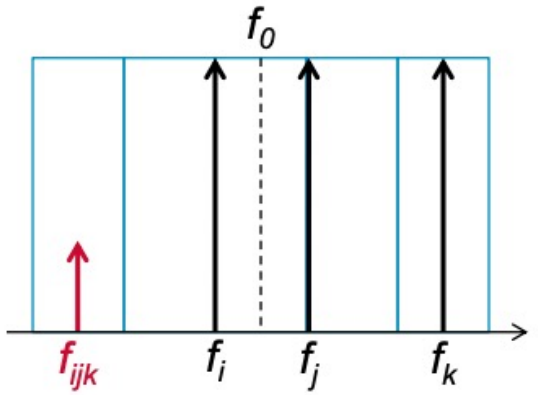
FWM efficiency:

$$\eta = \frac{\alpha^2}{\alpha^2 + \Delta\beta^2}\left(1 + \frac{4e^{-\alpha L}\sin^2(\Delta\beta L/2)}{(1 - e^{-\alpha L})^2}\right)$$

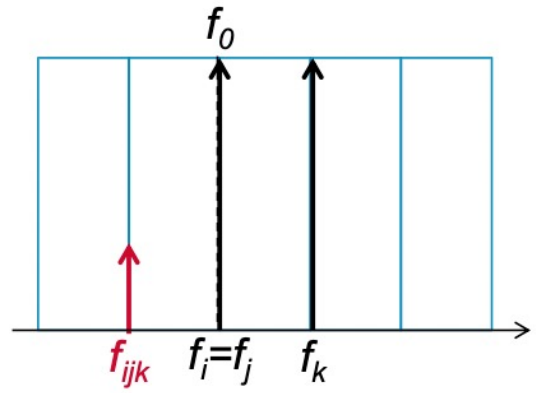
Phase matching condition:

$$\Delta\beta = \beta_i + \beta_j - \beta_k - \beta_{ijk}$$

$$\Delta\beta \approx \frac{2\pi\lambda^2}{c}(f_i - f_k)(f_j - f_k)\left[D(\lambda) - \frac{\lambda^2}{c}\left(\frac{f_i + f_j}{2} - f_{ijk}\right)\frac{dD}{d\lambda}\right]$$



- Dijk = 6 for non-degenerate mixing (3 distinct inputs)
- FWM conversion efficiency is maximum for phase-matched condition, $\Delta\beta = 0$, with f0, is centered between two of the input frequencies.



- Dijk =3forpartially-degenerate mixing (2 distinct inputs)
- FWM conversion efficiency is maximum for phase-matched condition, $\Delta\beta = 0$, with f0 = fi or fk.

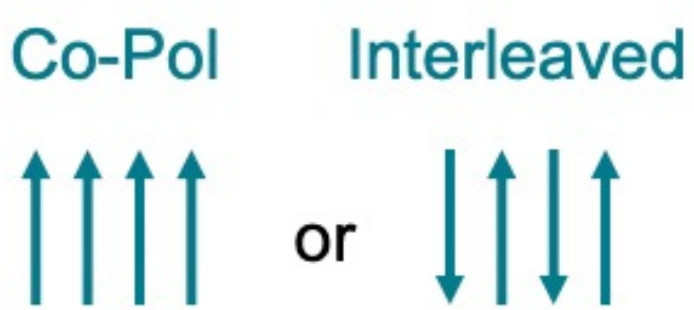
For all input powers = P, the FWM power

$$\frac{P_{ijk}}{P} = \left(\frac{D_{ijk}\gamma L}{3}\right)^2 P^2$$

FWM Penalty and Power Threshold Discussions

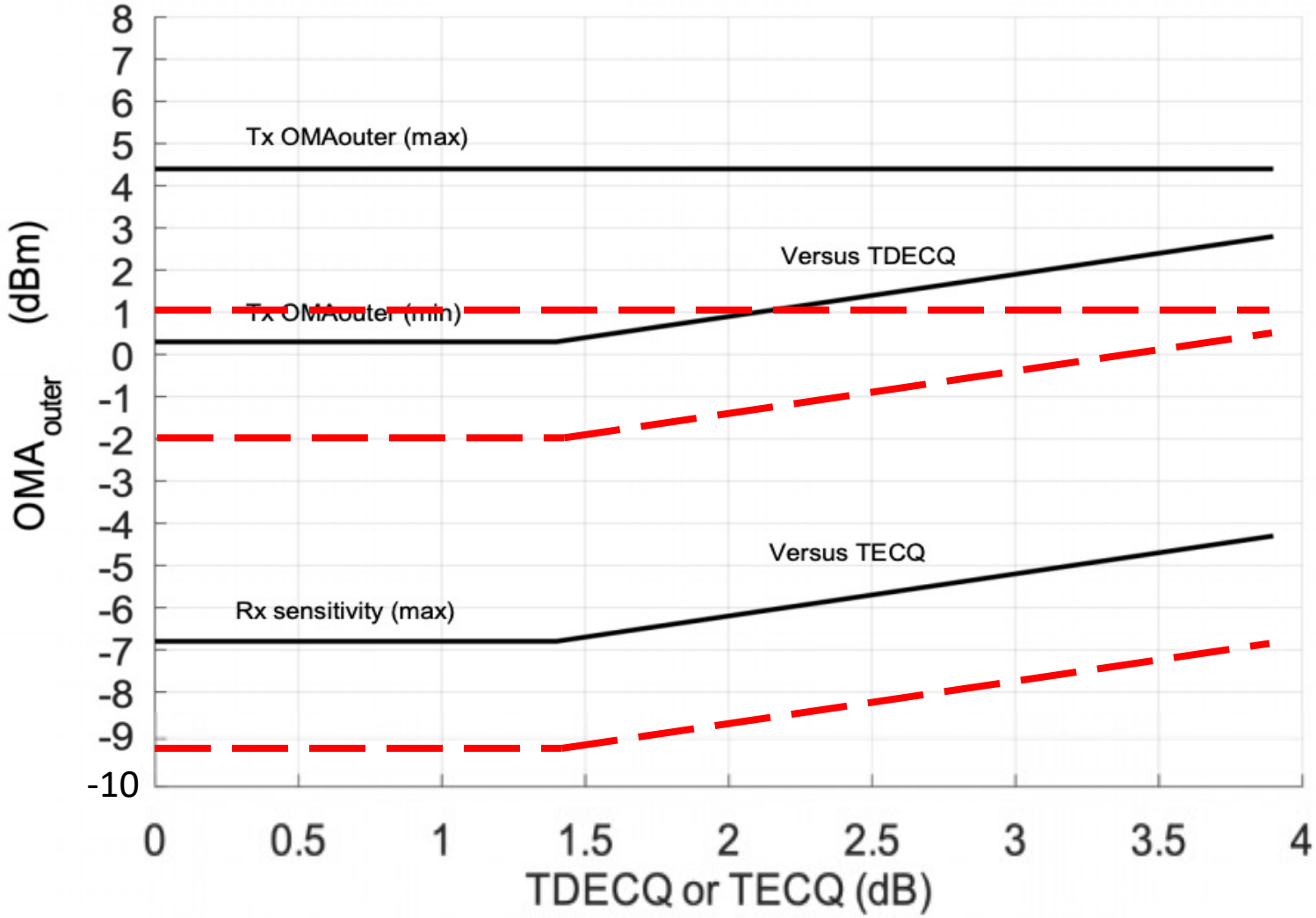
From John Johnson (John Johnson, “FWM Analysis 400G-ER4-30: Polarization Effect”, 100G Lambda MSA and Private communications)

- FWM “efficiency” requires channel polarization alignment
- Co-propagating channels over 10km without PMD, Channel power (OMA) threshold ~ -1.0 dBm to achieve FWM penalty <1dB
- Fiber PMD tends to scramble co-polarization, and reduce penalty to less than 1dB
- With polarization interleaving, equivalent channel power can be ~ 2.3dB higher, without PMD
- With fiber PMD, the FWM mitigation with polarization interleaving is somewhat reduced.



Proposed 800G LR4 Baseline Proposal

- Propose reduced Tx_OMA power_max with polarization to mitigate against FWM penalty
- Adjust receiver sensitivity accordingly to meet LR4 link budget

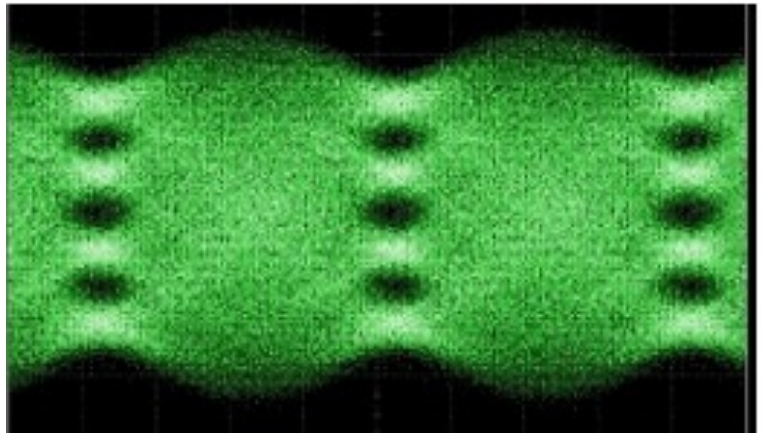


- Tx_OMAouter_max: + 1.0 dBm
- Tx_OMAouter_min:
  - -2.0dBm with TECQ < 1.4dB
  - -3.4dBm+TECQ with TDECQ>1.4dB
- Rx_sens_max:
  - -9.1dBm with TECQ < 1.4dB
  - -10.5dBm+TECQ with TECQ/TDECQ>1.4dB

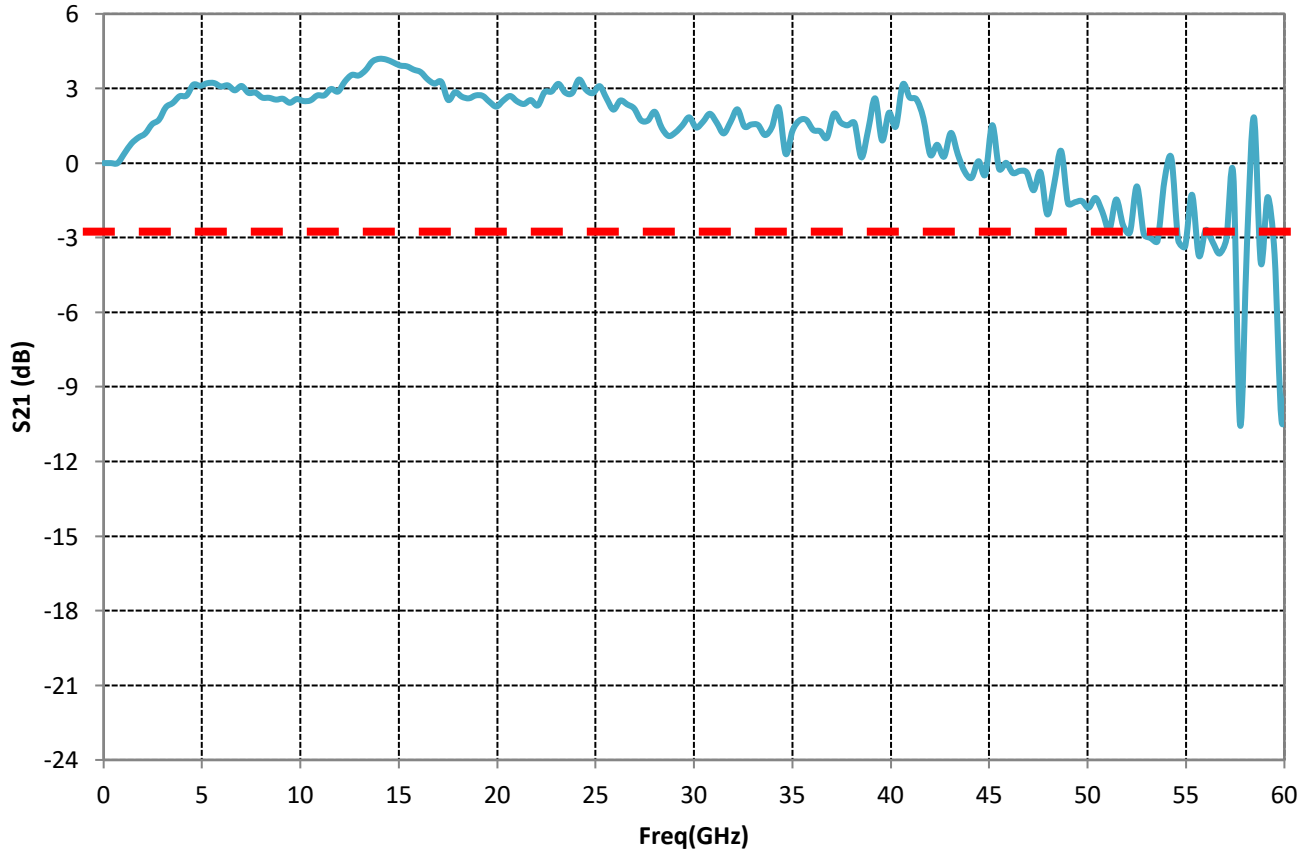
Feasibility of 100Gbaud PAM4 Transmitter

Silicon Photonics MZ Modulator with SiGe BiCMOS Driver (SiFotonics)

PAM4 Modulation Eye Diagram



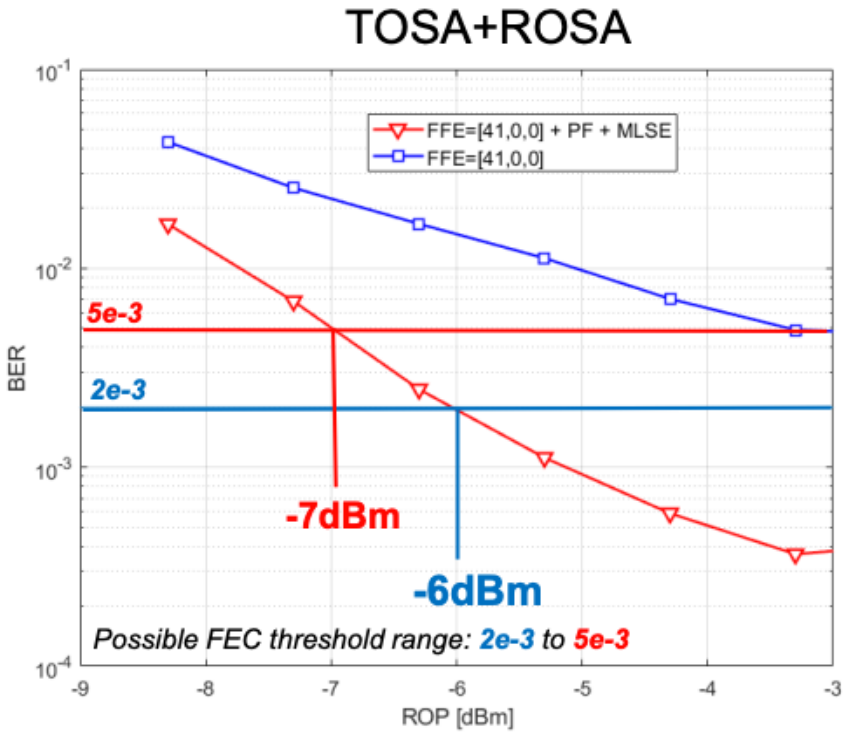
S21 Measurement of MZM and SiGe BiCMOS Driver combination



PIN Receiver Sensitivity Discussion

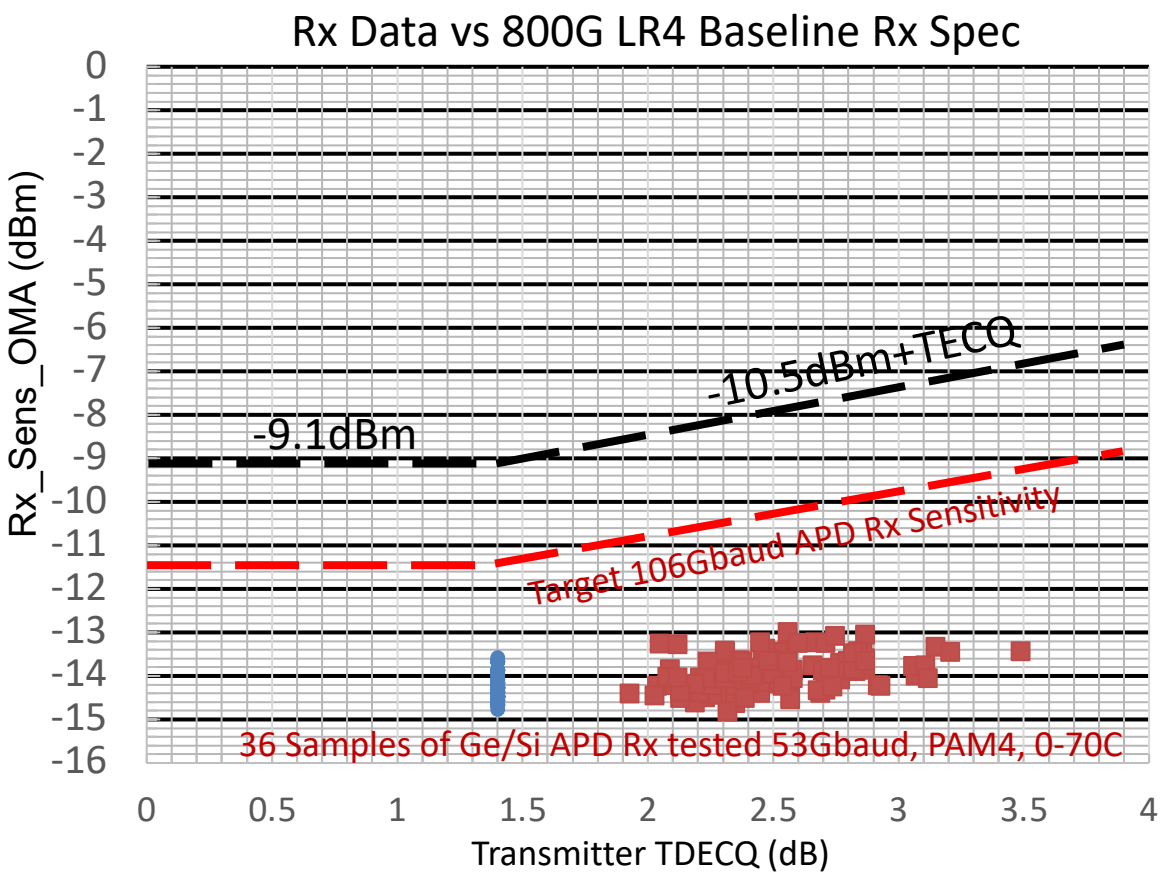
- Refer to M. Kuschnerov, "On the technical feasibility of optical 200 Gb/s PAM4", 802.3df, Feb'22, -8 to -9dbm sensitivity can be achieved with proper DSP capabilities

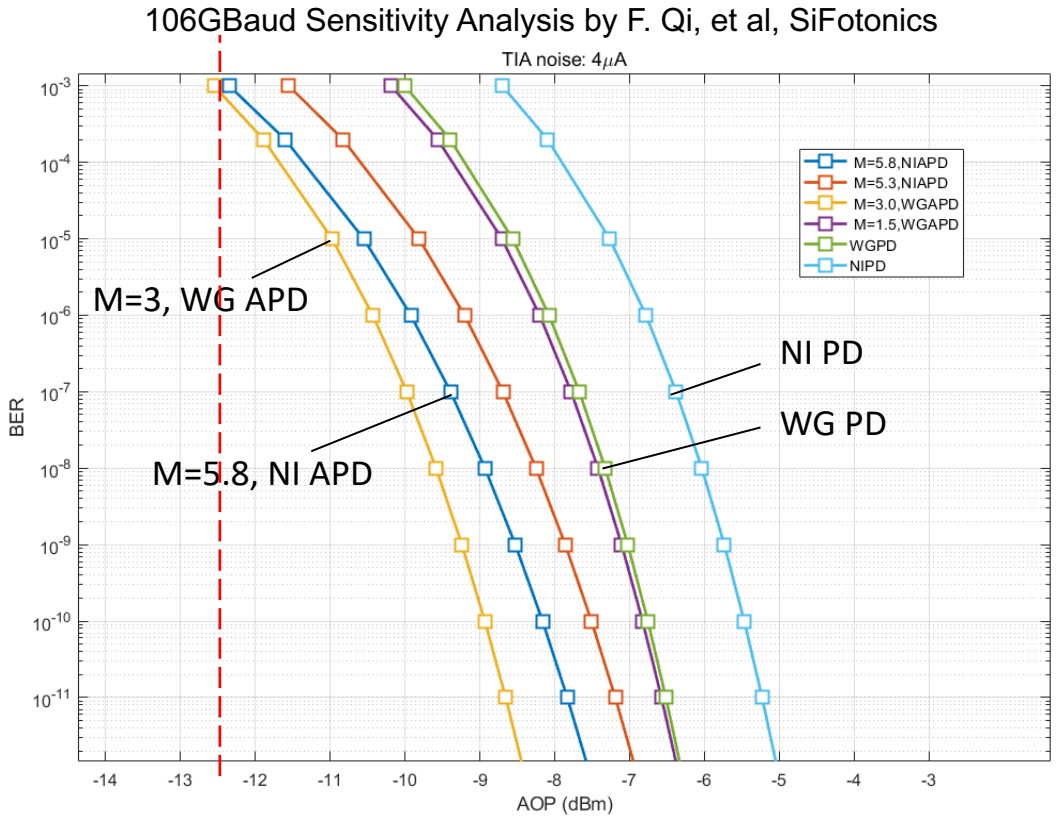
- These tests only used DAC1 as a reference
- Rx sensitivity:
  - -6dBm @ 2e-3 (Δ-1.5dB vs. PDFA)
  - -7.0dBm @ 5e-3 (Δ-2dB vs. PDFA)
- Using a DAC similar to DAC2, an improvement could be expected (>2dB) for an estimated Rx sensitivity of about -8dBm to -9dBm depending on the FEC



Receiver Sensitivity Improvement with APD Receiver

- Ge/Si APD had been in volume production over the last 5 years, with cum. Shipments > 1M Units for 25G+ data rate
- 8” Si wafer CMOS compatible technology enabling competitive alternative to traditional III-V APD, with improved Bandwidth-gain product
- Optimized Ge/Si APD expected 100GBaud PAM4 sensitivity ~ -12.5 dbm @BER 1E-3





Transmitter Spec. Proposal (Preliminary)

Description	800G LR4 Transmitter	Unit
PAM4 Signaling rate, (range)	106.25 ± 100 ppm	GBd
Wavelength (range)	L0=1304.06 to 1305.1 L1=1306.33 to 1307.38 L2=1308.61 to 1309.66 L3=1310.9 to 1311.96	nm
Side-mode suppression ratio (SMSR), (min)	30	dB
Total average launch power (max)	8.0	dBm
Channel Polarization at Launch (TP3)	Interleaved with adjacent channels	
Average launch power, (max) each lane	1.7	dBm
Average launch power,[a] (min), each lane	-5.0	dBm
Outer Optical Modulation Amplitude (OMA_{outer}), (max), each lane	1.0	dBm
Outer Optical Modulation Amplitude (OMA_{outer}),[b] (min), each lane For TDECQ<1.4dB For 1.4dB<TDECQ< TDECQ (max)	-2.0 -3.4+TDECQ	dBm
Difference in launch power between any two lanes (OMAouter) max	3	dB
Transmitter and dispersion penalty eye closure for PAM4 (TDECQ), (max)	3.9	dB
TECQ (Max)	3.9	
|TDECQ – TECQ | (max)	2.5	
Average launch power of OFF transmitter, (max)	-16	dBm
Extinction ratio (min)	3.5	dB
Transmitter over/under-shoot (max) Transmitter peak-to-peak power (max)	25	%
Transmitter peak-to-peak power (max)	5.2	dBm
Optical return loss tolerance (max)	15.6	dB
Transmitter reflectance[c] (max)	-26	dB
Transmitter transition time (max)	8.5	ps
$RIN_{15.6}$ OMA (max) for LR, RINxx.x OMA (max) for MR	-136	dB/Hz

Receiver Spec. Proposal (Preliminary)

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PAM4 Signaling rate, (range)	106.25 ± 100 ppm	GBd
Wavelength (range)	L0=1304.06 to 1305.1 L1=1306.33 to 1307.38 L2=1308.61 to 1309.66 L3=1310.9 to 1311.96	nm
Damage threshold, (min)[a]	TBD	dBm
Average receive power, (max), each lane	TBD	dBm
Average receive power,[b] (min), each lane	TBD	dBm
Receive power, (OMA_{outer}) (max), each lane	-2	dBm
Difference in receive power between any two lanes (OMAouter) (Max)	3	dB
Receiver reflectance (max)	-26	dB
Receiver sensitivity (OMA_{outer}),[c] (max), each lane For TDECQ<1.4dB For 1.4dB<TDECQ< TDECQ (max)	 -9.1 -10.5+TECQ	dBm
Stressed receiver sensitivity (OMA_{outer}),[d] (max) each lane	-6.6	dBm
Condition of stressed receiver sensitivity Test:		
Stressed eye closure for PAM4 (SECQ)	3.9	dB
OMAouter of each aggressor lane	-2.7	dBm

Comparison of Proposals

	This Proposal	Uneven Channel Proposal (Vipul et al)
Channel Plan	L0=1304.58nm L1=1306.85nm L2=1309.14 nm L3=1311.43nm	L0=1300.0nm L1=1303.4nm L2=1310.2nm L3=1324.1nm
Dispersion range	-19 to +11ps/nm	-22 to +22ps/nm
Tx_OMA_min.	-2.0dbm	+1.3dbm
Tx_OMA_max	+1dbm	
Tx Modulator Chirp Control	Not required	May Need to be tightly controlled
Rx_OMA_sensitivity_max (TECQ<1.4dB)	-9.1dbm	-5.8dbm
DSP Leverage	Share with 800G DR4/FR4	Can share with 800G DR4/FR4, if strong equalization implemented
Achieved Pfwm/Ps	<-30dB	<-30dB

Summary

- 800G LR4 with PAM4 IMDD baseline proposed
  - Channel frequency plan with 400GHz channel spacing near zero dispersion window of O-band
    - L0=1304.58nm
    - L1=1306.85nm
    - L2=1309.14 nm
    - L3=1311.43nm
  - Reduced transmitter power to mitigate FWM impairment
  - Adjust receiver sensitivity to meet 10km reach link budget
  - Proposed APD receiver as a viable option to support this target link budget
- Further refinement of specification expected with more detail study
  - e.g., if DSP is with stronger supporting higher CD level, the channel spacing can be relaxed to 800GHz, and Tx_OMA_power and Rx sensitivity may be adjusted up

Thank You!