Considering advanced signal processing for assessing electrical channel performance

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Introduction

- We are beginning to create specifications for an array of electrical and optical interfaces support ~200 Gb/s data rates per lane.
- This new generation of links are proving to be even more challenging to support than for 100 Gb/s.
- To address this challenging signaling rate, contributions have proposed various improvements to all aspects of the link including lower loss package, improved package escape, cabled routing from chip to faceplate, etc.
- Even with these improved assumptions we are still falling short of link budgets that work for the reaches we want to support.
- This contribution proposes that we explore how to incorporate the effects of MSLE in the channel operating margin (COM).

New standards projects targeting 200 Gb/s per lane

- At IEEE 802.3df project the following interfaces with 200 Gb/s per lane are being defined:
  - Direct-attach copper cable: 1.6TBASE-CR8, 800GBASE-CR4, 400GBASE-CR2, 200GBASE-CR1
  - C2M/C2C: 1.6TAUI-8, 800GAUI-4, 400GAUI-2, 200GAUI-1
  - 500 m parallel SMF: 1.6TBASE-DR8, 800GBASE-DR4, 400GBASE-DR2, 200GBASE-DR1
  - 2 km parallel SMF: 1.6TBASE-DR8-2, 800GBASE-DR4-2, 400GBASE-DR2-2, 200GBASE-DR1-2
  - 2 km duplex SMF: 800GBASE-FR4
  - 10 km duplex SMF: 800GBASE-LR4 (maybe; debating four lanes IMDD PAM4 vs single lane coherent)
- At OIF the following interface specifications with 200 Gb/s per lane are being defined:
  - CEI-224G-XSR-PAM4
  - CEI-224G-VSR-PAM4
  - CEI-224G-MR-PAM4
  - CEI-224G-LR-PAM4
- This contribution explores improvements to the specification methodology for the longer-reach electrical interfaces.

Use of higher gain FEC

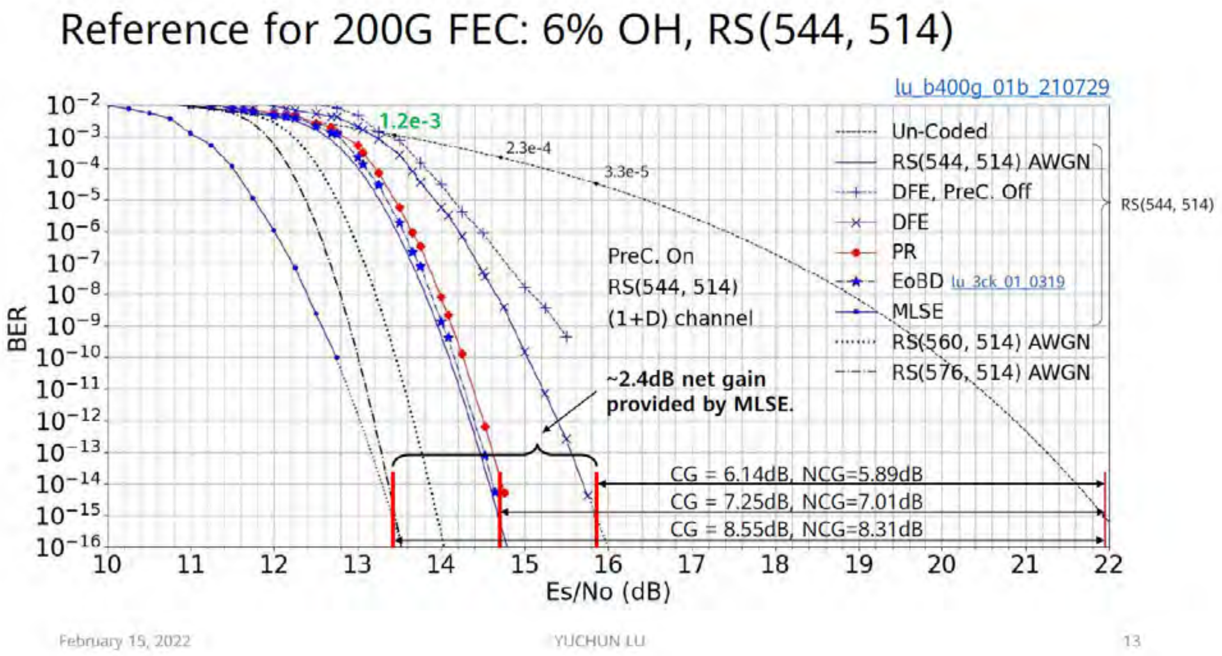
- In order to create more budget, higher gain FEC has been considered, however…
  - In order to get a decent increment in coding gain the encoded bit rate must be increased to support the increased coding overhead.
  - For high-loss or band-limited channels, the penalty due to the rate increase negates the coding gain improvement.
  - The higher FEC complexity increases the link latency.
  - The increased rate increases the power consumed at each active element in the link between the FEC encoder and decoder.
    - Increasing FEC gain is possible without increasing the bit rate, but with a significant increase in latency and complexity.
  - It would be beneficial to reuse the currently defined RS(544,514) FEC and its associated bit rate for at least one more generation, for commonality with previously standardized interfaces.
- <u>Use of a higher gain FEC for high insertion-loss or band-limited medium is not a helpful solution.</u>

Use of MLSE

- Instead of changing the encoding and permitting a higher pre-FEC BER, more elaborate signal processing might be assumed in order to achieve the currently defined pre-FEC BER targets.
  - In other words, increase the complexity of the reference receiver used assess the performance of an electrical channel.
- One DSP technique that has not been exploited, although it is in common use, is MLSE (maximum likelihood sequence estimation).
  - A well designed MLSE can improve link performance by a few dB for some channel characteristics including insertion loss, non-linearity, and dispersion.
- In order to leverage the effects of the MLSE, a way to assess channels using this receiver capability must be built into the specifications.
  - The effect cannot be applied simply by using a fixed improvement offset since the degree of improvement depends upon the channel characteristics.
- <u>Explore inclusion of the effects of MLSE in COM reference receiver.</u>

Some evidence supporting MLSE

- Yuchun Lu (Huawei) et al proposed at IEEE 802.3df that use of MLSE should be assumed. https://www.ieee802.org/3/df/public/22_02/lu_3df_01b_220215.pdf
- The analysis demonstrates that addition of MLSE in a reference receiver results in a theoretical SNR improvement of around 2.4 dB.
- The analysis further shows that the RS(544,514) combined with the MLSE, provides the same benefit as RS(576,514), but without the rate penalty, without affecting other elements in the link, and with much lower latency.



The path forward

- To incorporate MLSE effect into COM we should consider the following:
  - Is there a convenient method to accurately incorporate the effect of MLSE into COM?
  - Is there a practical MSLE implementation with appropriate power and complexity?
  - What is the net effect of MLSE given practical considerations?
- Contribution shakiba_3df_01a_2211 initiates this process, introducing a convenient methodology for incorporating MLSE into the COM methodology.

Conclusions

- Further enhancements to COM methodology used to assess channel performance are required for higher loss electrical channels.
- Assumptions of higher-gain FEC are not fruitful.
- MLSE is common in electrical long-reach receivers and should be considered when assessing the performance of electrical channels.
- Explore paths toward incorporating the effects of MLSE in the COM methodology.

THANKS!