Concatenated SFEC proposal for 200Gb/s per Lane IM-DD Optical PMD

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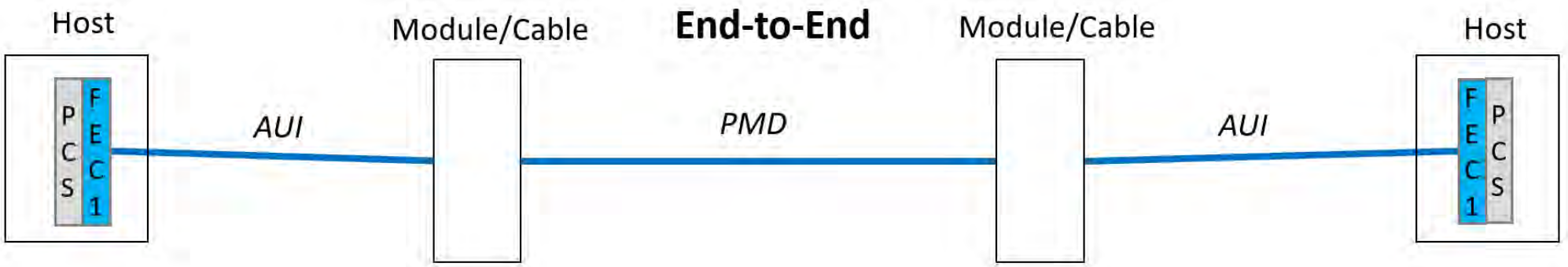
Goal of the presentation

In this presentation, we review the proposed SFEC(128,120) based on shortened Hamming code (68,60) that works in conjunction with the standard KP FEC in the host. The proposed Soft decision FEC can provide enough coding gain to enable the deployment of 200G optical PMD for DR, FR and potentially LR reaches.

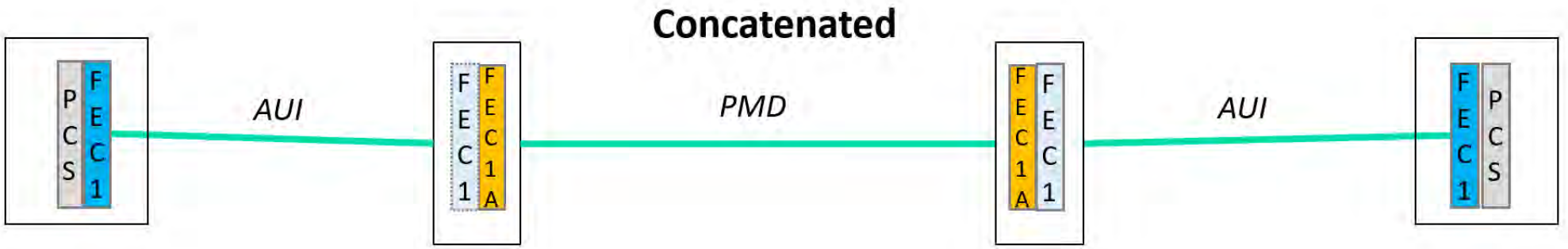
Refresh of FEC Architecture already discussed in this forum: End-to-End, Segmented, Concatenated scheme

FEC 1: is end-to-end (AUI+PMD+AUI)



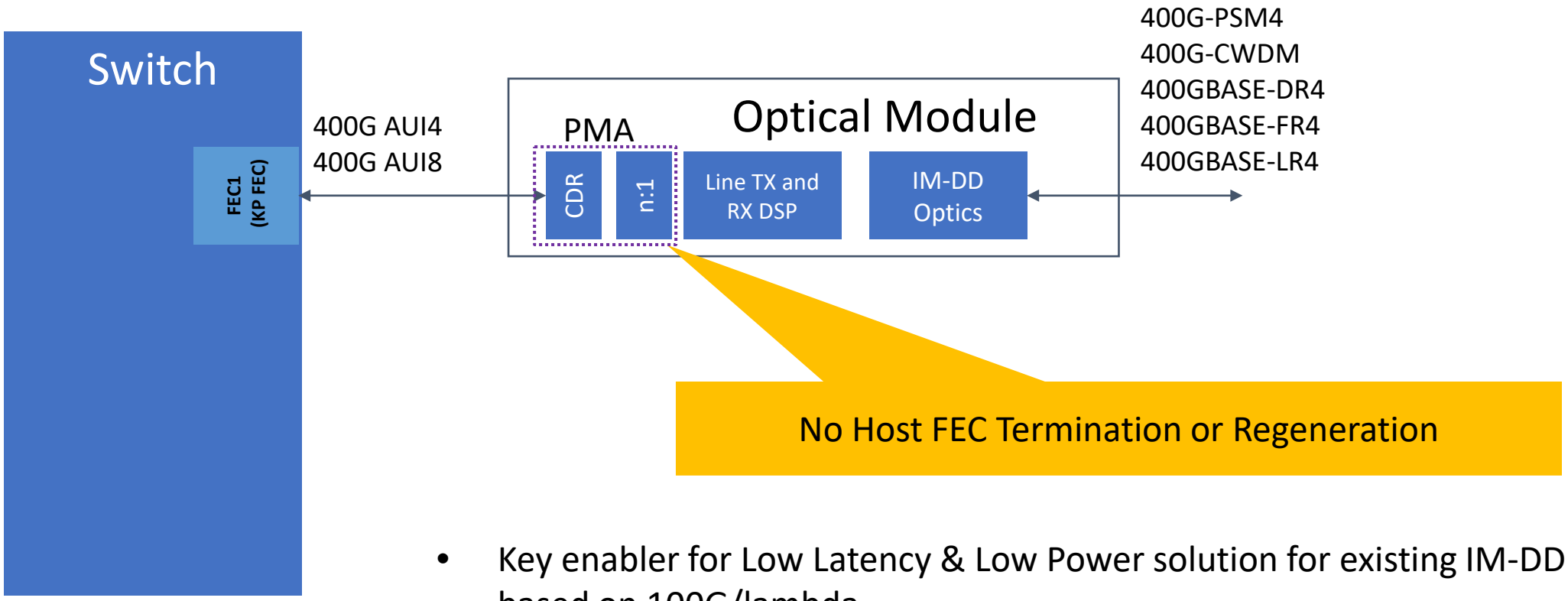
FEC 1: AUI only
FEC 2: PMD only

FEC 1 (outer) FEC: (AUI + PMD + AUI**)** Optional PMD FEC1
FEC 1A (inner) FEC: (PMD only)



What is inside the Data Center Optical modules today?

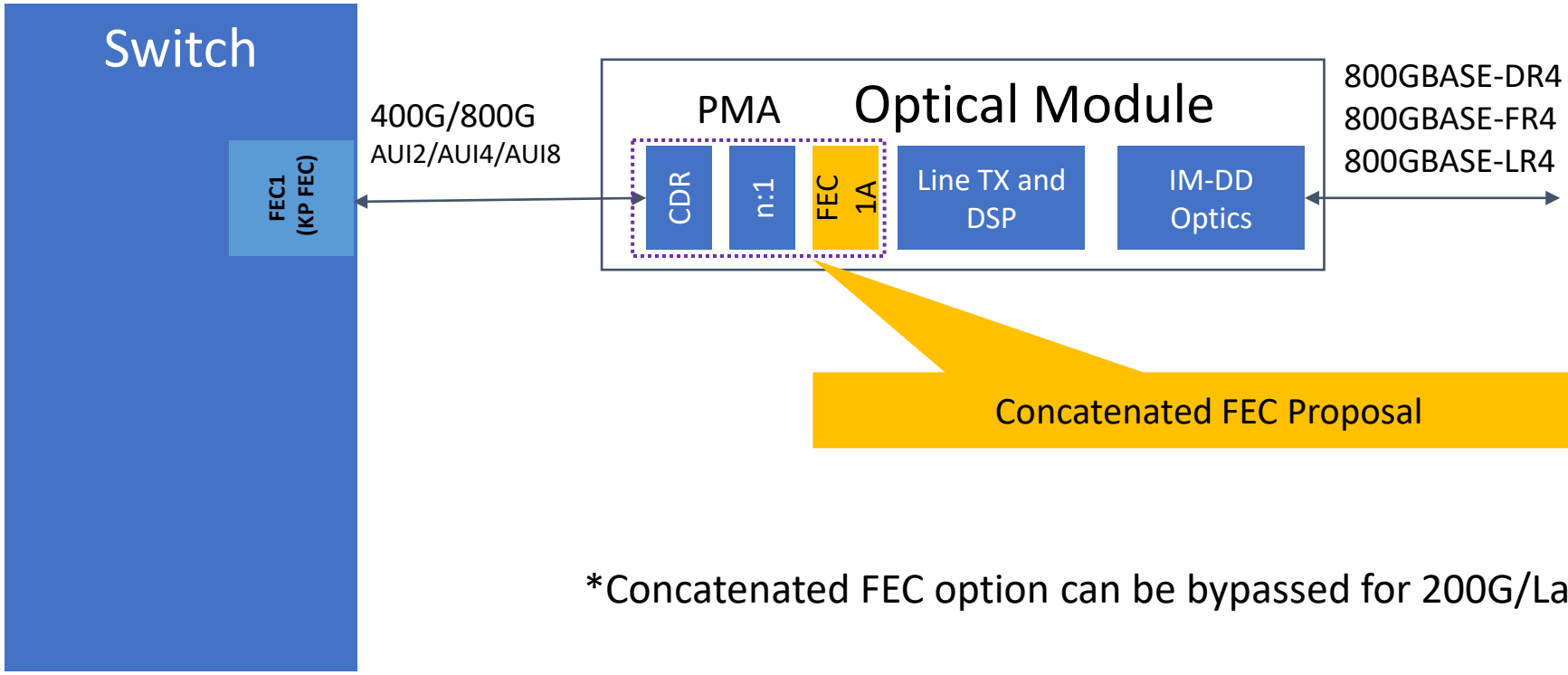
- “Re-timers” and “gearboxes” represent the bulk of DSP deployed inside the IM-DD optics today.



- Key enabler for Low Latency & Low Power solution for existing IM-DD optics based on 100G/lambda

Concatenated FEC extends the Low Latency and Low Power concept for NextGen – 200G/lambda

- n:1 “gearbox” generalized to a simple convolutional interleaver
- Inner FEC code concatenated with the interleaved bit stream



*Concatenated FEC option can be bypassed for 200G/Lambda benign links as well

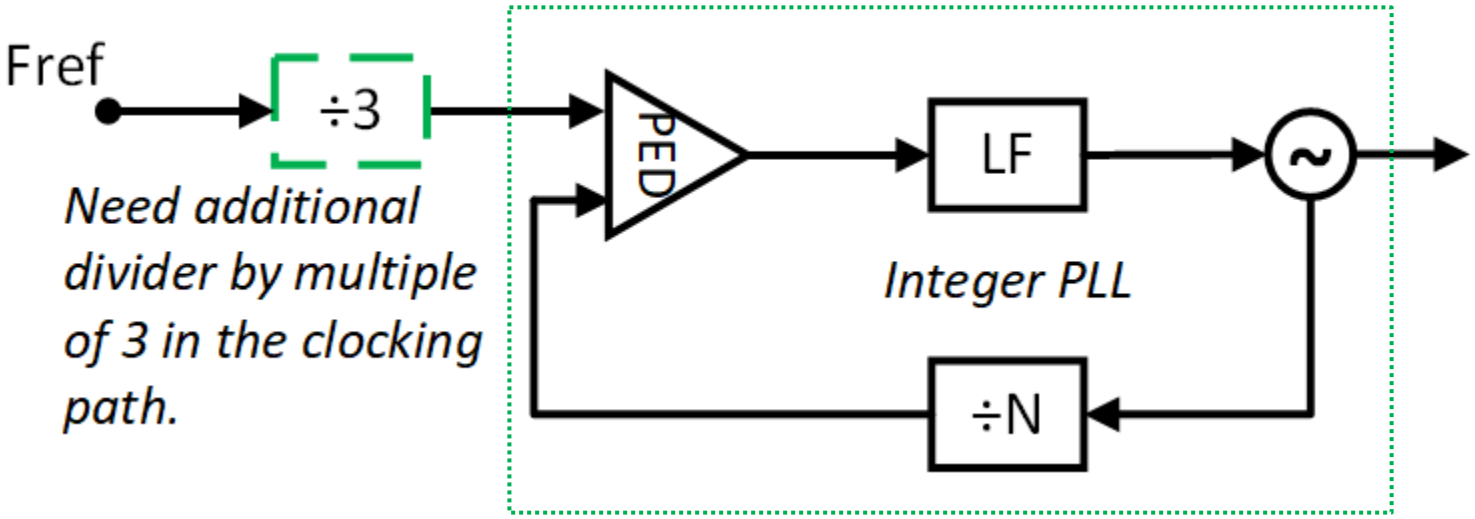
Overview of various Concatenated SFEC Proposal presented in this forum

- KP4 + Extended Hamming (128,120) – Concatenated FEC candidate – works in conjunction with Host KP4 FEC
  - patra_3df_01_ 2207, bliss_3df_01c_220517
  - A perfect multiple of 10b RS symbols → works very well with proposed convolutional interleaver
  - code length of 128b aligns nicely with power of 2 radix implementation of both Tx DSP/DAC as well as ADC/Rx DSP
  - Baud Rate: 113.33G

- KP4 + Extended Hamming (144,136) – another suitable Concatenated FEC candidate
  - he_3df_01a_220308
  - Not a multiple of 10b RS symbols → Needing gearbox kind of extra logic to work with Convolutional inter-leaver
  - Baud rate :112.5G

- KP4 + Shortened Hamming (76,68) – another suitable Concatenated FEC candidate
  - bliss_3df_01_220929.pdf
  - Not a multiple of 10b RS symbols → Needing longer inter-leaver and additional glue logic for synchronization
  - Baud rate: 112.5G

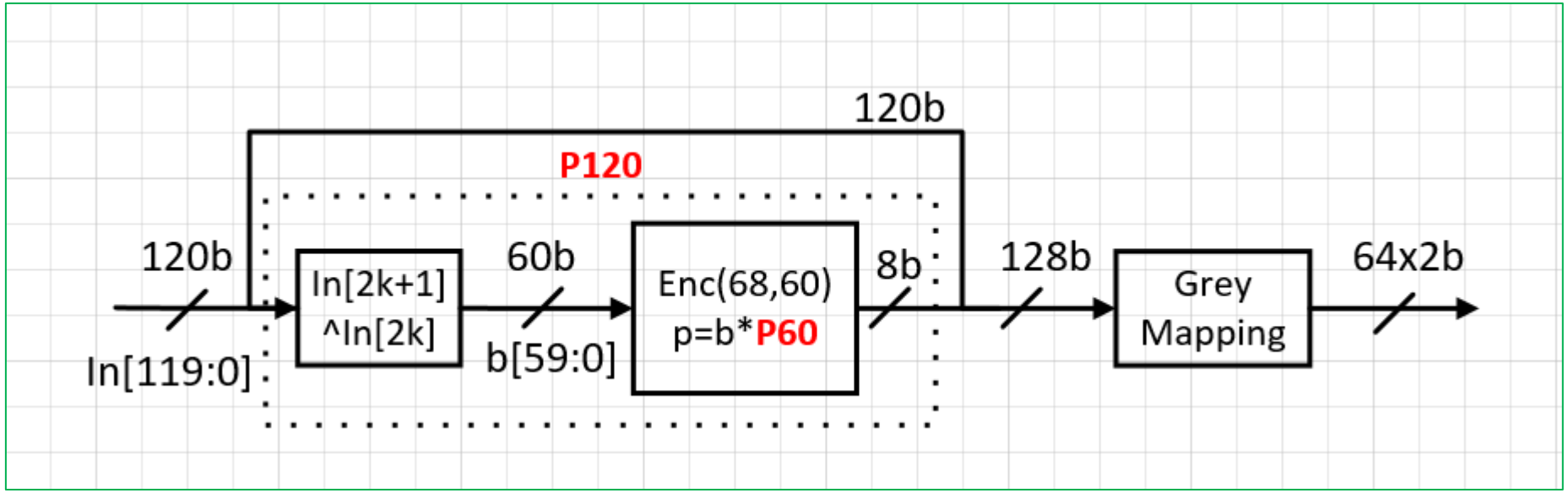
SFEC(128,120) baud rate & simplified view of the clocking implementation



- SFEC(128,120) baud rate 113.33Gbaud :
  - Fref * (p/q)
  - Fref = 156.25Mhz
  - p = 128*17
  - q = 3

- Baud rates for SFEC(128,120) or SFEC(144,136) or SFEC(76,68) can be implemented using integer PLLs
- SFEC(128,120) requires an additional, yet minor, divider by 3 in the clocking data path.
  - *In practice, the Fref is generally multiplied up to M*1GHz and the divide by 3 (or multiples of 3, comes for free)*

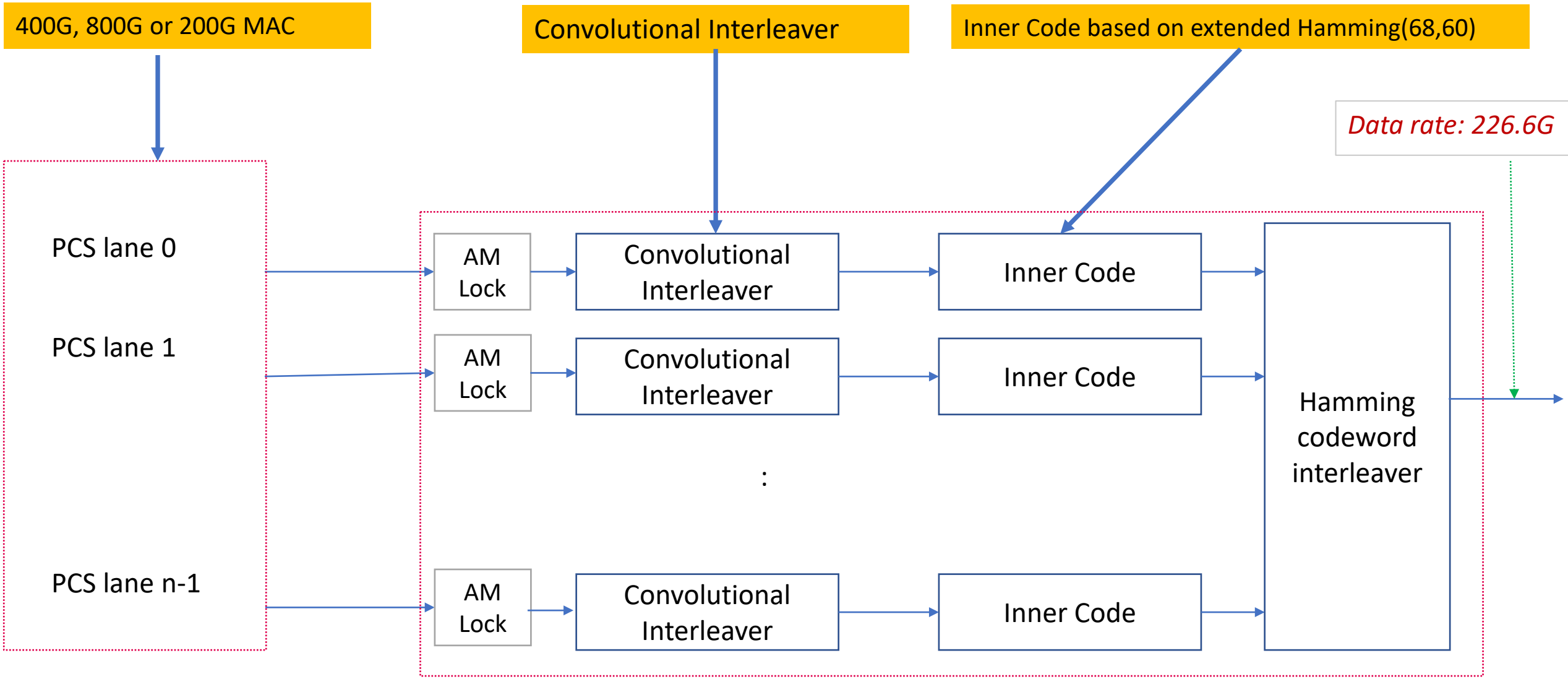
Proposed Inner code SFEC(128,120) based on Hamming(68,60)



- 60b Hamming payload is formed by XOR of bits in 2bx60 input
- Same rate as extended hamming code (128/120) and block length of 128b
  - Baud rate : KP FEC rate * 128/120 = 113.33 Gbaud
- Input is aligned with incoming 12 x 10b RS symbols from Host
- 1b per payload PAM4 UI, 2b per parity PAM4 UI
  - Benefits of smaller area due to reduction in logic for syndrome/parity calculation
- Gray mapping applied to output of systematic encoder to map to PAM4

This proposal matches the SFEC (128,120) proposal presented by patra_3df_01_ 2207, shared in IEEE previously.

Overall Representation of Proposed System TX Encoding Datapath with SFEC(128,120)

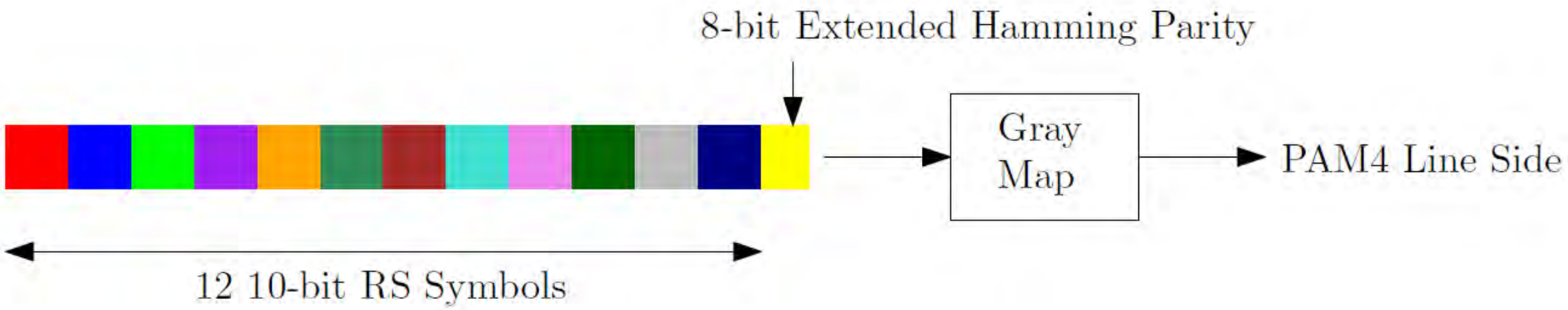


*n = 32 VL for 800G and 16 VL for 400G MAC mode based on 100G/Lane and similar VL scheme can be adopted for 200G/lane

Details of SFEC Architecture in terms of data path:

- Details of SFEC mode Processing:
  - **Per FECL** TX processing
    - **AM lock**
      - To determine KP4 symbol boundaries
    - **Convolutional Interleaving (CI)**
      - To form Hamming payload as 12x10b KP4 symbols
    - **Hamming Encoder**
      - Appends 8b parity to 120b payload
    - **Hamming Codeword Interleaver**
      - **8-way Hamming Interleaving:**
        - The 8 ENC outputs are aligned with respect to Hamming codeword boundaries
        - The 8 ENC@25G codewords are round-robin inter-leaved, in units of 2b
        - E.g., 2b from ENC0, 2b from ENC1, 2b from ENC2, …, 2b from ENC7, 2b from ENC0, etc.
      - **1-way Hamming Interleaving:**
        - 64 consecutive UI are transmitted per Hamming-encoded FECL, aligned to codeword boundaries

Purpose of Convolutional Interleaver for Concatenated FEC



- The *Convolutional Interleaver* ensures each hamming code word encodes 12 10-bit RS symbols from *different* Reed-Solomon codewords.
- 8 parity bits are computed over **12** (10b) RS Symbols.
- Burst error tolerance is a function of both convolutional interleaver and Hamming codeword interleaver.

KP4+SFEC(128,120): Convolutional Interleaver

- The “**full latency**” CI implementations guarantee that the 12x10 bit payload of the Hamming encoder comes from 12 distinct RS codewords.
- The “**low-latency**” CI implementations guarantee that the 12x10 bit payload of the Hamming encoder has at most two 10b symbols per RS codeword.

SFEC data path will provide few distinct Convolutional Interleaver options for standardization:

1) 802.3bs 400G or 800G Ethernet Consortium or 800G IEEE (**Full Latency)**
2) 802.3bs 200G (**Full Latency)**
3) 802.3bs 400G or 800G Ethernet Consortium or 800G IEEE (**Low Latency**)
4) 802.3bs 200G (**Low Latency)**

Illustration : 400G/800G ETC mode – Full latency Interleaver

- **20b** (FEC_A,FEC_B) symbols represented by **A[m]**
  - Delay lines operate on 20b symbols
- 544/16=34
  - A[m] and A[m-n] are guaranteed to come from distinct RS codewords if n>=34
- 6 “branches” of CI due to 6-way interleaving of (FEC_A,FEC_B) symbols in Hamming payload
  - Hamming payload is **(A[6k-180],A[6k-143],A[6k-106],A[6k-69],A[6k-32],A[6k+5])**

- Input/output switches are always in sync, but **no requirement** to sync relative to AM position
  - At TX, switches move from top to bottom
- Synchronization at RX is **implied** by Hamming codeword boundaries (i.e., Hamming sync implies CI sync)

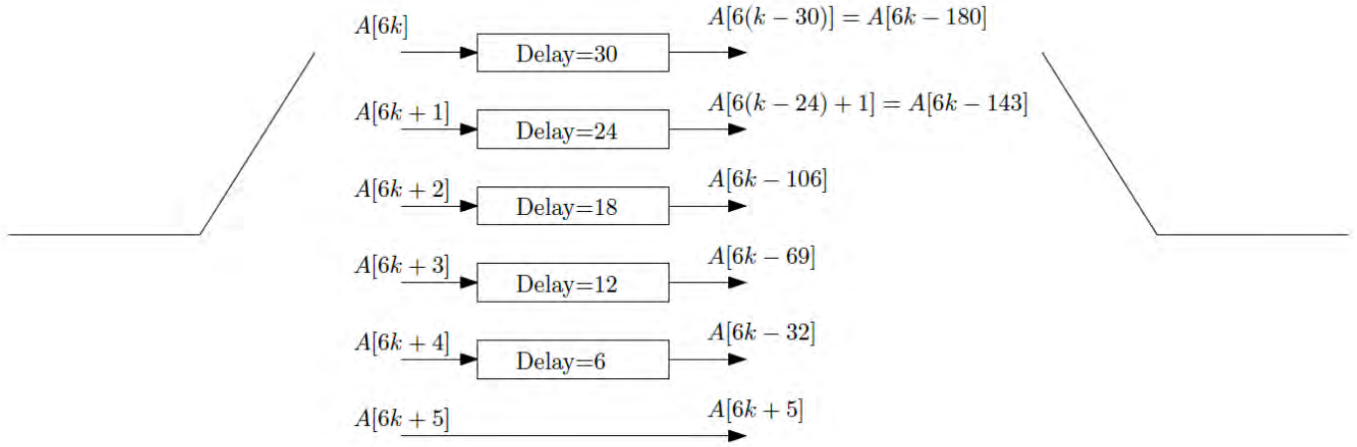
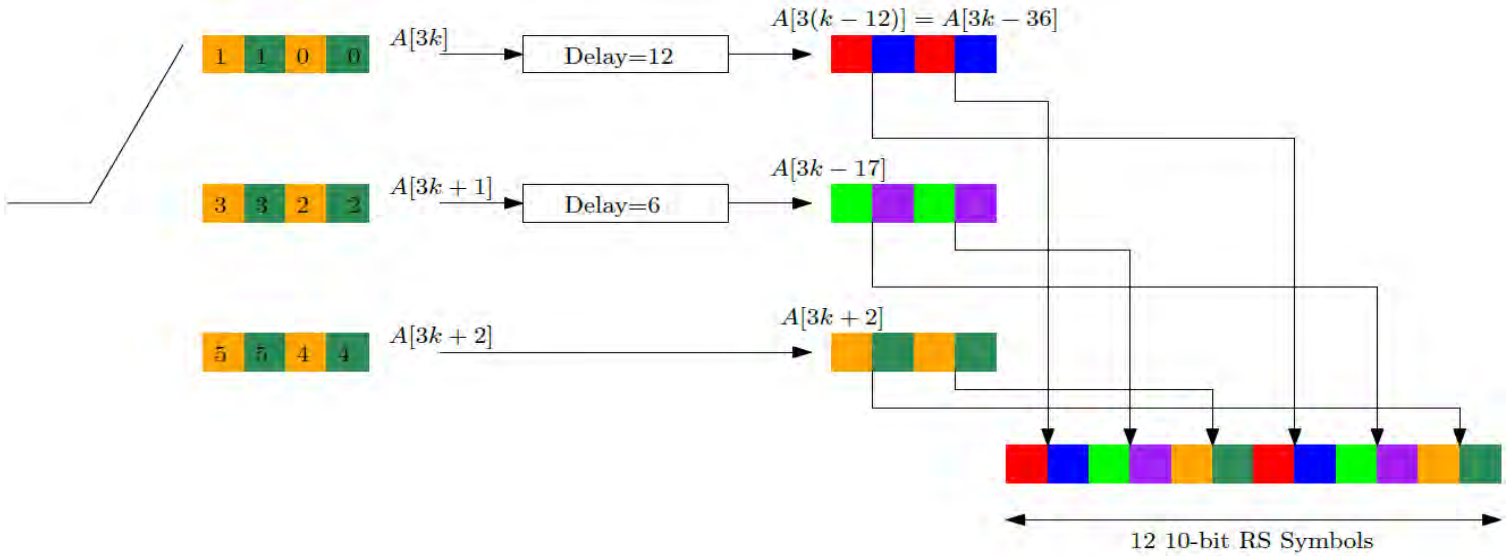


Illustration : 400G/800G ETC mode – Low Latency Interleaver

- **40b** (FEC_A,FEC_B, FEC_A,FEC_B) symbols represented by **A[m]**
  - Delay lines operate on 40b symbols
- **Total Latency (CI+CDI): 36x40=1440b @ 25G**
  - For comparison, the Full Latency mode has 20x180=3600b @ 25G



Summary of SFEC (128,120) + Convolutional Interleaver : BER and Latency trade off for various operating modes

SFEC	Baud Rate	Convolutional Interleaver	Operating Mode	Latency	Pre-FEC BER
(128,120)	113.33Gbaud	High Latency option	400G	~140ns	~4.8E-3
			800G ETC (2 way interleaved)	~140ns	~4.8e-3
			800G (4 way interleaved)	~ 56ns	~4.8E-3
			200G	~280ns	~4.8e-3
		Low Latency option ** results in 0.25dB penalty in coding gain	400G	~56ns	~4.0E-3
			800G ETC (2 way interleaved)	~56ns	~4.0e-3
			800G (4 way interleaved)	~ 25ns	~4.0E-3
			200G	~110ns	~4.0e-3

Hamming Encoder generation Matrix:

1	0	0	1	0	1	0	0
1	0	0	1	0	1	0	0
0	1	0	0	1	0	1	0
0	1	0	0	1	0	1	0
0	0	1	0	0	1	0	1
0	0	1	0	0	1	0	1
1	1	0	0	1	0	1	1
1	1	0	0	1	0	1	1
1	0	1	1	1	1	0	0
1	0	1	1	1	1	0	0
0	1	0	1	1	1	1	0
0	1	0	1	1	1	1	0
0	0	1	0	1	1	1	1
0	0	1	0	1	1	1	1
1	1	0	0	1	1	1	0
1	1	0	0	1	1	1	0
0	1	1	0	0	1	1	1
0	1	1	0	0	1	1	1
1	1	1	0	1	0	1	0
1	1	1	0	1	0	1	0
0	1	1	1	0	1	0	1
0	1	1	1	0	1	0	1
1	1	1	0	0	0	1	1
1	1	1	0	0	0	1	1
1	0	1	0	1	0	0	0
1	0	1	0	1	0	0	0
0	1	0	1	0	1	0	0
0	1	0	1	0	1	0	0
0	0	1	0	1	0	1	0
0	0	1	0	1	0	1	0
0	0	0	1	0	1	0	1
0	0	0	1	0	1	0	1
1	1	0	1	0	0	1	1
1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0
1	0	1	1	0	0	0	0
0	1	0	1	1	0	0	0
0	1	0	1	1	0	0	0

- SFEC(128,120) : P120 matrix
- This p120 matrix is simply twice the replication of P60 matrix

The 60x8 matrix P is given by:

P=

1	0	0	1	0	1	0	0
0	1	0	0	1	0	1	0
0	0	1	0	0	1	0	1
1	1	0	0	1	0	1	1
1	0	1	1	1	1	0	0
0	1	0	1	1	1	1	0
0	0	1	0	1	1	1	1
1	1	0	0	1	1	1	0
0	1	1	0	0	1	1	1
1	1	1	0	1	0	1	0
0	1	1	1	0	1	0	1
1	1	1	0	0	0	1	1
1	0	1	0	1	0	0	0
0	1	0	1	0	1	0	0
0	0	1	0	1	0	1	0
0	0	0	1	0	1	0	1
1	1	0	1	0	0	1	1
1	0	1	1	0	0	0	0
0	1	0	1	1	0	0	0
0	0	1	0	1	1	0	0
0	0	0	1	0	1	1	0
0	0	0	0	1	0	1	1
1	1	0	1	1	1	0	0
0	1	1	0	1	1	1	0
0	0	1	1	0	1	1	1
1	1	0	0	0	0	1	0
0	1	1	0	0	0	0	1
1	1	1	0	1	0	0	1
1	0	1	0	1	1	0	1
1	0	0	0	1	1	1	1
1	0	0	1	1	1	1	0
0	1	0	0	1	1	1	1
1	1	1	1	1	1	1	0
0	1	1	1	1	1	1	1
1	1	1	0	0	1	1	0
0	1	1	1	0	0	1	1
1	1	1	0	0	0	0	0
0	1	1	1	0	0	0	0
0	0	1	1	1	0	0	0
0	0	0	1	1	1	0	0
0	0	0	0	1	1	1	0
0	0	0	0	0	1	1	1
1	1	0	1	1	0	1	0
0	1	1	0	1	1	0	1
1	1	1	0	1	1	1	1
1	0	1	0	1	1	1	0

Hamming (68,60)

P60 matrix

Summary

- SFEC(128,120) proposal based on shortened Hamming code(68,60) can provide more than enough coding boost to enable the deployment of 200G Optical PMDs.

- KP4 + SFEC(128,120) proposal is aligned with incoming payload from the Host as a pack of 10b RS symbols, simplifying the convolutional Interleaver and providing lowest latency, lowest power benefit to overall 200G PMD subsystem.

- Code length of 128b aligns nicely with power of 2 radix implementation of both Tx DSP/DAC as well as ADC based Rx DSPs.

- Overhead for KP4 + SFEC (128,120) is 113.3Gbaud, very similar to the baud rate proposed with different concatenated FECs in IEEE. But it does NOT necessarily warrant a Fractional PLL implementation.

- Leveraging the existing KP4 FEC for 200G AUI will benefit the industry and will ease the backward compatibility issues.

Thanks !