# 212.5 Gbps-PAM4 Chip-to-Module Link Simulation and Analysis with a High-Loss Channel

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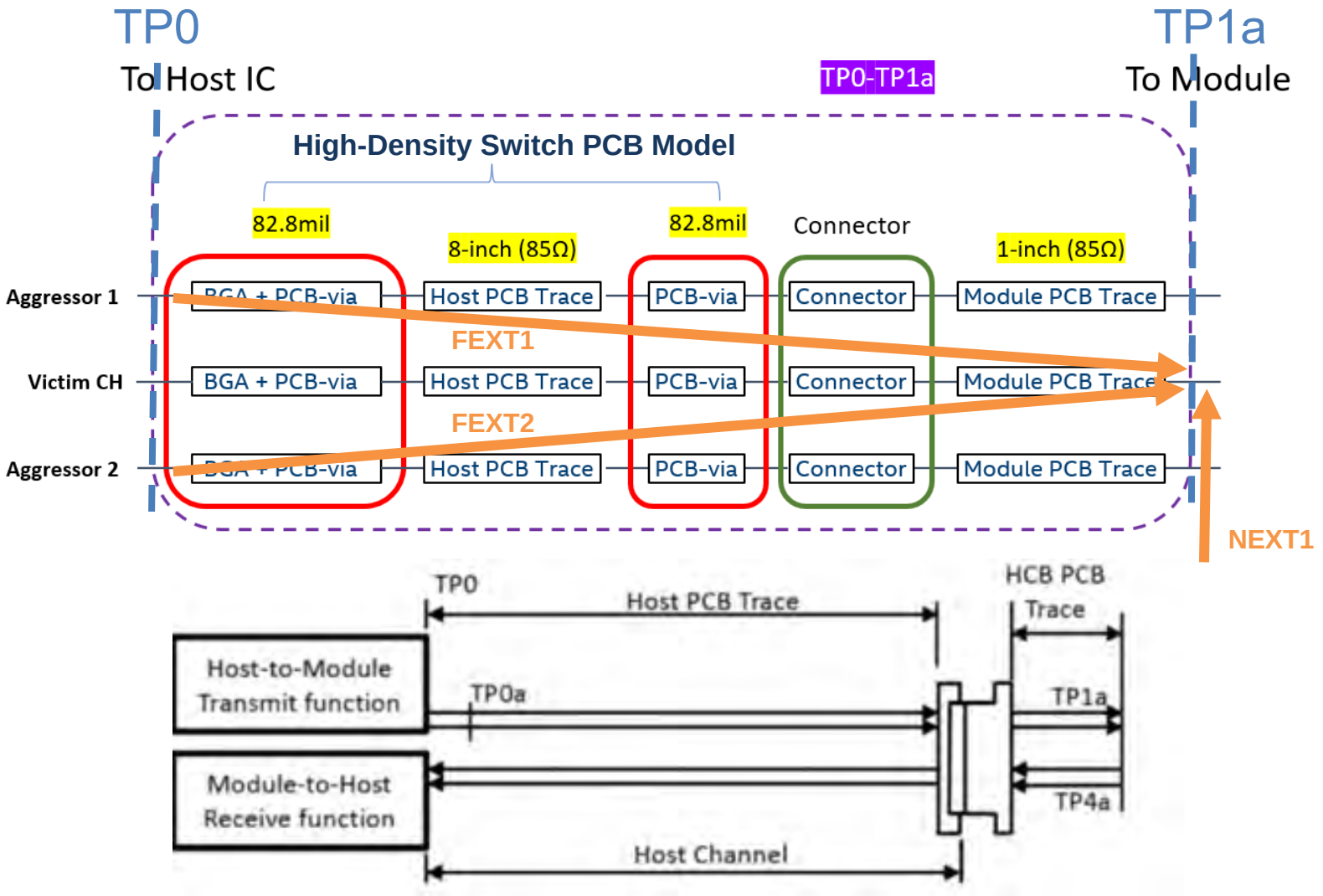
# Background and Introduction

- Update to Q3'22 presentation "224 Gbps Chip-to-Module Link Simulation and Analysis Update 2" (oif2022.355.00), with
  - Updated chip-to-module channel which is based on a real/practical high-density/radix switch device and board design
- Progress history
  - Update to Q2'22 presentation "224 Gbps Chip-to-Module Link Simulation and Analysis Update" (oif2022.174.01), with
    - Updated chip-to-model COM configuration and analysis results
    - Time-domain link simulation results
  - Update to Q3'21 presentation "212/224 Gbps Chip-to-Module Link Simulation and Analysis" (oif2021.446.00), with
    - Latest C2M channel model(s)
    - Proposed CEI-224G-LR-PAM4 reference TX (oif2022.067.00)
    - Proposed CEI-224G-LR-PAM4 reference die/package model (oif2022.065.02)
    - TP1a reference scope RX based on the proposed CEI-224G-LR-PAM4 reference RX AFE (oif2022.067.00)

# C2M Channel Topology



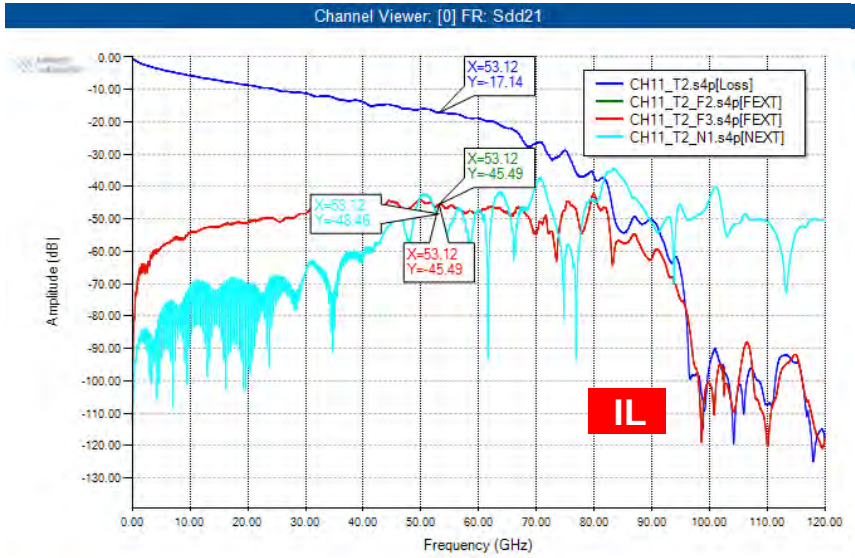

Channel Configuration Summary

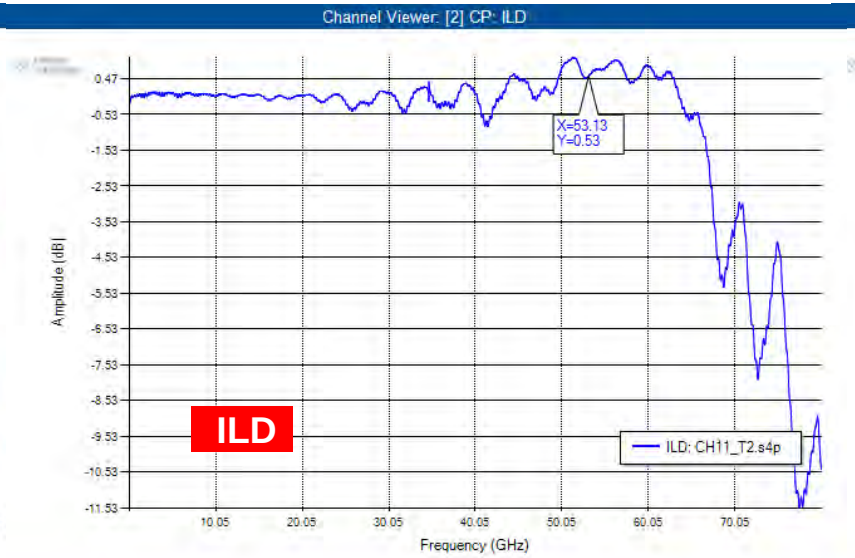
- 2 Channels were analyzed
  - CH11: Shown on the left
  - CH12: Same as CH11 with 10-in Host PCB
- Crosstalk
  - 2 FEXT
  - 1 NEXT

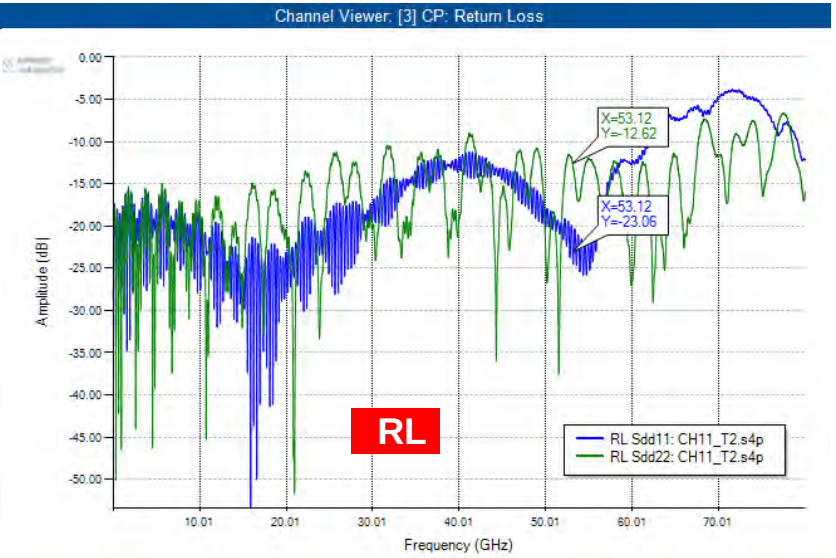
**Insertion Loss Break Down**

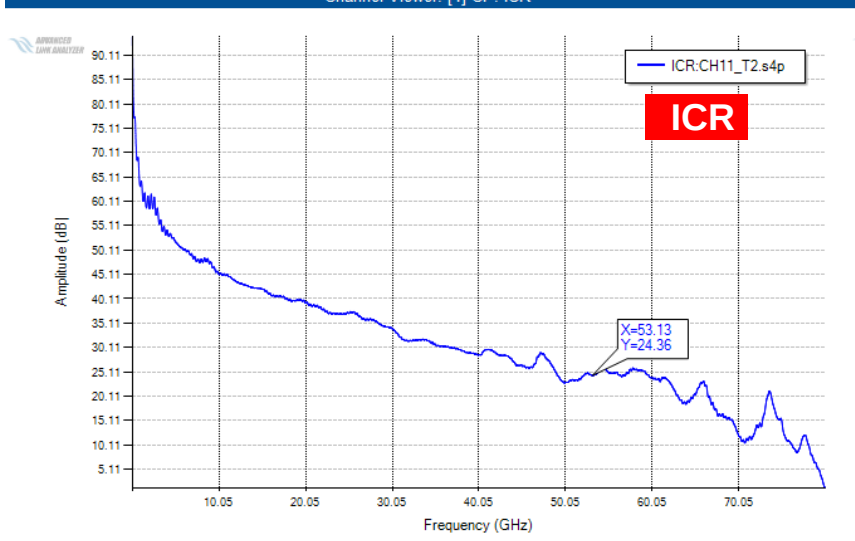
| Component | Insertion Loss (dB) @ 53.125GHz | |
|---|---|---|
| | CH11 (8-in) | CH12 (10-in) |
| BGA via | 0.95 | |
| PCB | 11.2 | 14.2 |
| Connector via | 0.95 | |
| Connector | 1.5 | |
| Module card | 2.37 | |
| Total | 17.14 | 20.03 |

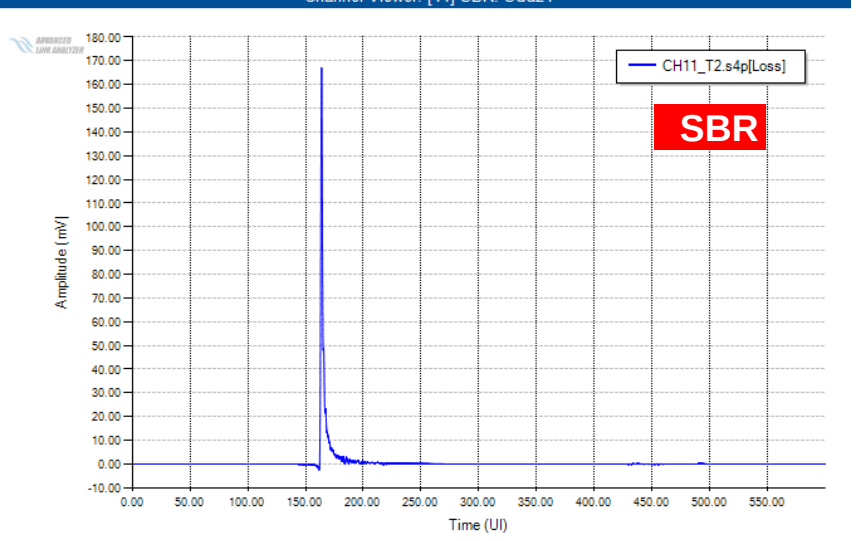
# C2M Channel Characteristics (CH11)



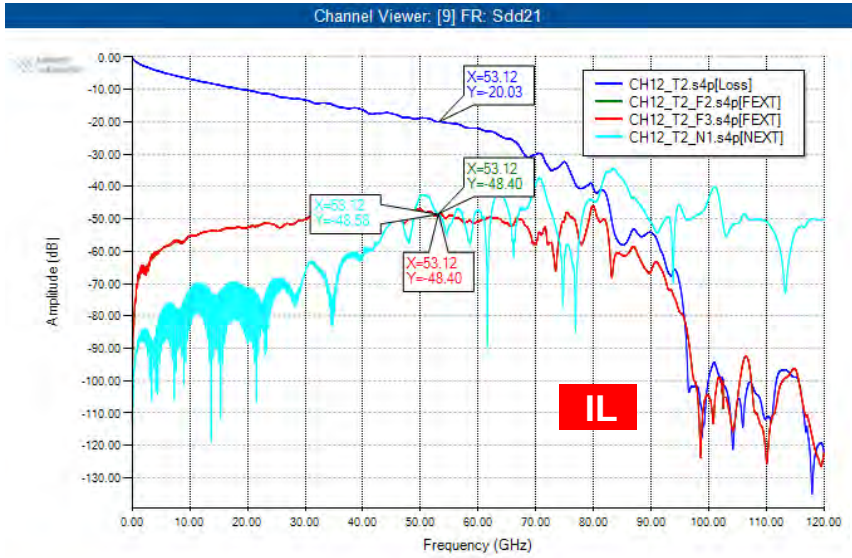



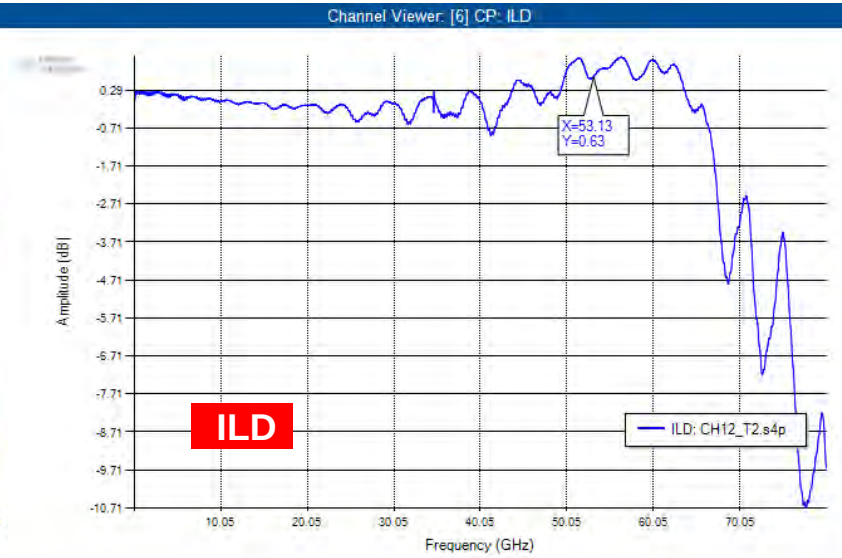



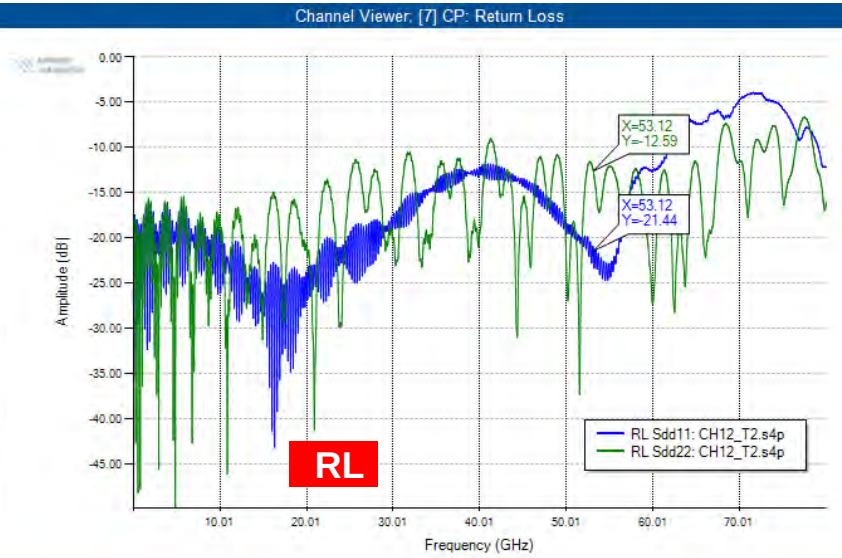



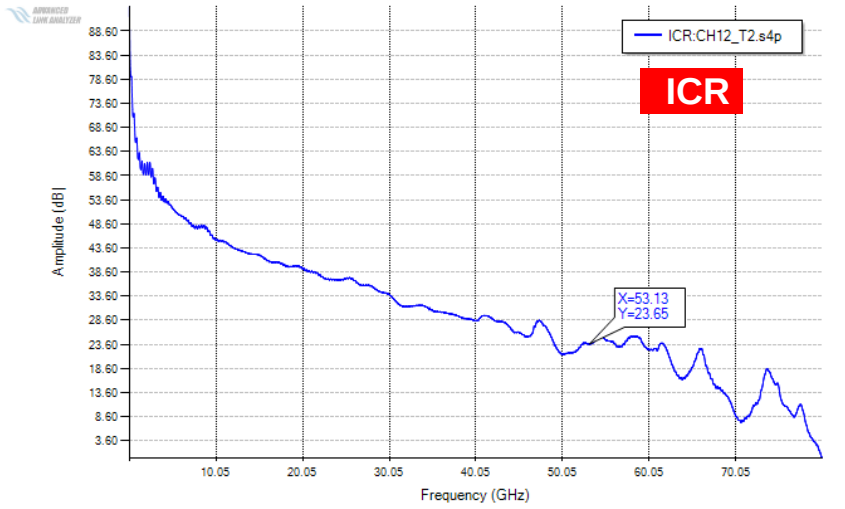

- IL: 17.14dB @ 53.125 GHz
- ILD ~= 1dB
- RL ~= 10dB
- FEXT ~= 46dB NEXT ~= 48dB, ICR ~= 24.36dB

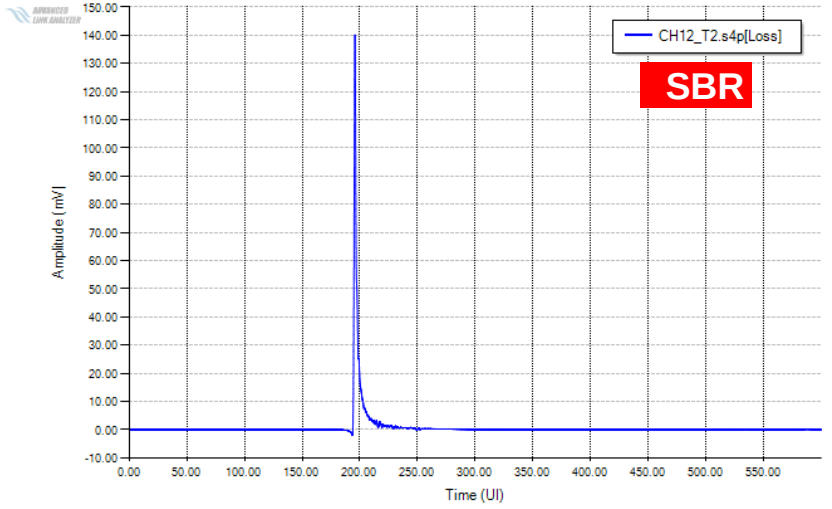
# C2M Channel Characteristics (CH12)




- IL: 20.03dB @ 53.125 GHz
- ILD ~= 1dB
- RL ~= 10dB
- FEXT ~= 48dB NEXT ~= 49dB, ICR ~= 23.65dB

# Preliminary 212.5 Gbps PAM4 COM Analysis

*for C2M Channel TP1a Test*

- Based on 802.3ck chip-to-module COM with the following changes
  - TP1a COM Test Configuration:
    - Proposed CEI-224G-VSR-PAM4 reference TX
      - RLM = 0.95, $SNR_{TX}$=33dB, BUJ = 0.02$UI_{pk}$, RJ = 0.01$UI_{RMS}$
      - 20%-80% Rise/Fall Time (*T_r*): ~3ps (*i.e. 0.31875x UI*)
      - TX FIR: 4-pre, 1-post
      - TX Die: No change (see oif2022.065.02)
      - TX Package:
        - $Z_p$ = 33mm, $Z_{p2}$ = 2.1mm (to support high-density/radix switch)
        - $\gamma_0$ $a_2$, and $C_p$ updated to reflected the latest design (see COM table)
    - TP1a Reference Receiver (Scope)
      - Based on scaled 802.3ck CR/C2M reference RX with DFE (8 fixed, 6 groups of 3 consecutive floating taps up to 80 UI), and Input Referred Noise = $5x10^{-9}$ $V^2$/GHz
    - Measurement Window: +/-50mUI
    - DER: $10^{-6}$, $10^{-5}$, and $10^{-4}$

**Changes are in red**

# Preliminary 212.5 Gbps PAM4 COM Analysis *(cont.)*

*for C2M Channel TP1a Test*

- Preliminary COM analysis results

**DER =$10^{-6}$**

| Channel | EH | VEC | COM |
|---|---|---|---|
| CH11 | 5.61 mV | 12.69 dB | 2.29 dB |
| CH12 | 3.68 mV | 13.79 dB | 1.99 dB |

**DER =$10^{-5}$**

| Channel | EH | VEC | COM |
|---|---|---|---|
| CH11 | 7.64 mV | 10.01 dB | 3.30 dB |
| CH12 | 5.49 mV | 10.89 dB | 2.92 dB |

**DER =$10^{-4}$**

| Channel | EH | VEC | COM |
|---|---|---|---|
| CH11 | 9.93 mV | 7.73 dB | 4.59 dB |
| CH12 | 6.99 mV | 8.21 dB | 4.27 dB |

# Proposed COM Configuration

| Table 93A-1 parameters | | | |
|---|---|---|---|
| **Parameter** | **Setting** | **Units** | **Information** |
| f_b | 106.25 | GBd | |
| f_min | 0.05 | GHz | |
| Delta_f | 0.01 | GHz | |
| C_d | [0.4e-4 0e-4; 0.9e-4, 0e-4; 1.1e-4, 0e-4] | nF | [TX RX] |
| L_s | [0.13, 0; 0.15, 0; 0.14, 0 ] | nH | [TX RX] |
| C_b | [0.3e-4, 0e-4] | nF | [TX RX] |
| z_p select | [ 2 ] | | [test cases to run] |
| z_p (TX) | [15 33; 2.1 2.1 ] | mm | [test cases] |
| z_p (NEXT) | [ 0 0 ; 0 0 ] | mm | [test cases] |
| z_p (FEXT) | [15 33; 2.1 2.1 ] | mm | [test cases] |
| z_p (RX) | [ 0 0 ; 0 0 ] | mm | [test cases] |
| C_p | [0.6e-4 0e-4] | nF | [TX RX] |
| R_0 | 50 | Ohm | |
| R_d | [50 50] | Ohm | [TX RX] |
| A_v | 0.413 | V | vp/vf=.694 |
| A_fe | 0.413 | V | vp/vf=.694 |
| A_ne | 0.608 | V | |
| L | 4 | | |
| M | 32 | Samp/UI | |
| samples_for_C2M | 100 | Samp/UI | |
| T_O | 50 | mUI | |
| AC_CM_RMS | 0 | V | [test cases] |
| **filter and Eq** | | | |
| f_r | 0.5 | *fb | |
| c(0) | 0.5 | | min |
| c(-1) | [-0.4:0.02:0] | | [min:step:max] |
| c(-2) | [0:0.02:0.16] | | [min:step:max] |
| c(-3) | [-0.1:0.02: 0] | | [min:step:max] |
| c(-4) | [0] | | |
| c(1) | [-0.1:0.02:0] | | [min:step:max] |
| N_b | 8 | UI | |
| **b_max(1)** | 0.85 | | **As/dffe1** |
| **b_max(2..N_b)** | [0.3 0.2*ones(1,6)] | | **As/dfe2..N_b** |
| **b_min(1)** | 0.3 | | **As/dffe1** |
| **b_min(2..N_b)** | [-0.3 -0.2*ones(1,6)] | | **As/dfe2..N_b** |
| g_DC | [-20:1:-0] | dB | [min:step:max] |
| f_z | 25.16 | GHz | |
| f_p1 | 40 | GHz | |
| f_p2 | 56 | GHz | |
| g_DC_HP | [-6:1:-0] | | [min:step:max] |
| f_HP_PZ | 1.4 | GHz | |
| G_Qual | [] | dB | ranges |
| G2_Qual | [] | dB | ranges |
| GDC_Min | 0 | dB | 0 disables check. maybe different for each interface. |

| I/O control | | |
|---|---|---|
| DIAGNOSTICS | 1 | logical |
| DISPLAY_WINDOW | 1 | logical |
| CSV_REPORT | 1 | logical |
| RESULT_DIR | .\results\100GEL_C2M_host_{date}\ | |
| SAVE_FIGURES | 0 | logical |
| Port Order | [ 1 3 2 4 ] | |
| RUNTAG | C2M_eval_ | |
| COM_CONTRIBUTION | 0 | logical |
| Local Search | 2 | |
| **Operational** | | |
| VEC Pass threshold | 12 | db |
| EH_min | 8 | mV |
| ERL Pass threshold | 7.3 | dB |
| Min_VEO_Test | 5 | mV |
| DER_0 | 1.00E-06 | |
| T_r | 0.002845982 | ns |
| FORCE_TR | 1 | 5 |
| PMD_type | C2M | |
| BREAD_CRUMBS | 0 | logical |
| SAVE_CONFIG2MAT | 1 | logical |
| PLOT_CM | 0 | logical |
| **TDR and ERL options** | | |
| TDR | 1 | logical |
| ERL | 0 | logical |
| ERL_ONLY | 0 | logical |
| TR_TDR | 0.01 | ns |
| N | 800 | |
| beta_x | 0 | |
| rho_x | 0.618 | |
| fixture delay time | [ 0 0.2e-9 ] | [ port1 port2 ] |
| TDR_W_TXPKG | 1 | |
| N_bx | 20 | UI |
| Tukey_Window | 1 | |
| **Receiver testing** | | |
| RX_CALIBRATION | 0 | logical |
| Sigma BBN step | 5.00E-03 | V |
| **Noise, jitter** | | |
| sigma_RJ | 0.01 | UI |
| A_DD | 0.02 | UI |
| eta_0 | 5.00E-09 | V^2/GHz |
| SNR_TX | 33 | dB |
| R_LM | 0.95 | |

different for each test fixture

| Table 93A–3 parameters | | |
|---|---|---|
| **Parameter** | **Setting** | **Units** |
| package_tl_gamma0_a1_a2 | [0.0005 0.00089 0.0002] | |
| package_tl_tau | 0.006141 | ns/mm |
| package_Z_c | [87.5 87.5 ; 92.5 92.5 ] | Ohm |
| **ICN & FOM_ILD parameters** | | |
| f_v | 0.742 | *Fb |
| f_f | 0.742 | GHz f_r specified in first column |
| f_n | 0.742 | GHz |
| f_2 | 40 | GHz |
| A_ft | 0.600 | V |
| A_nt | 0.600 | V |
| Histogram_Window_Weight | Gaussian | gaussian. triangle, rectangle |
| sigma_r | 0.02 | sigma in UI fo or gaus.. Wind |

| Table 92–12 parameters | | |
|---|---|---|
| **Parameter** | **Setting** | |
| board_tl_gamma0_a1_a2 | [0 3.8206e-04 9.5909e-05] | |
| board_tl_tau | 0.00579 | ns/mm |
| board_Z_c | 100 | Ohm |
| z_bp (TX) | 407 | mm |
| z_bp (NEXT) | 407 | mm |
| z_bp (FEXT) | 407 | mm |
| z_bp (RX) | 407 | mm |
| C_0 | 0 | nF |
| C_1 | 0 | nF |
| Include PCB | 0 | logical |

upodated for D3.1

| Floating Tap Control | | |
|---|---|---|
| N_bg | 6 | 0 1 2 or 3 groups |
| N_bf | 3 | taps per group |
| N_f | 80 | UI span for floating taps |
| bmaxg | 0.2 | max DFE value for floating taps |

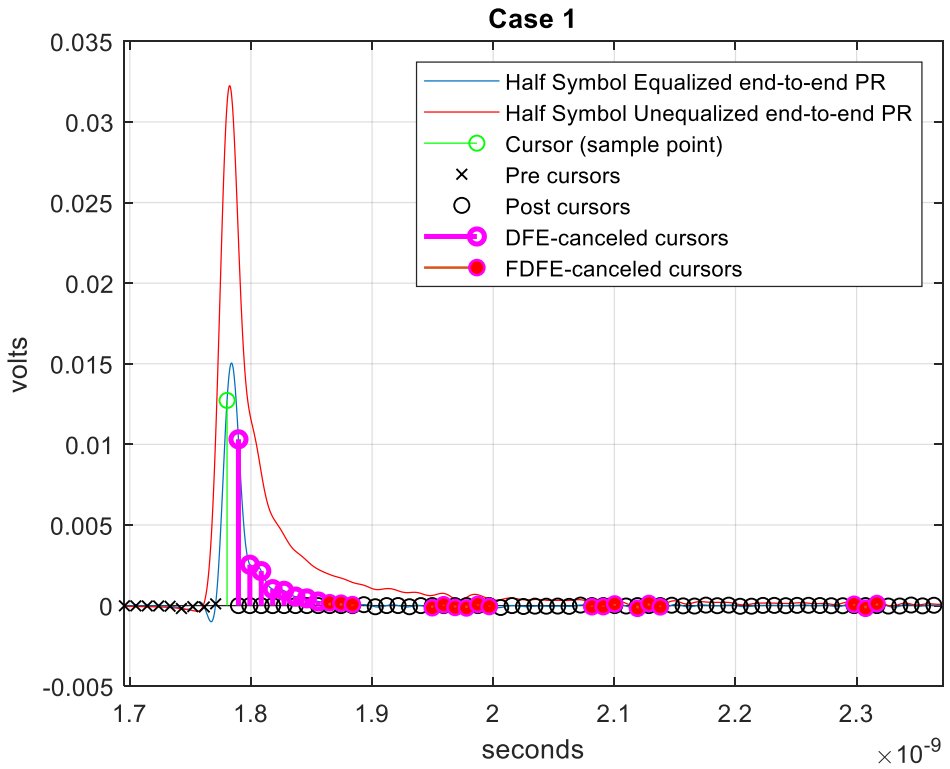
***Changes highlighted in yellow***

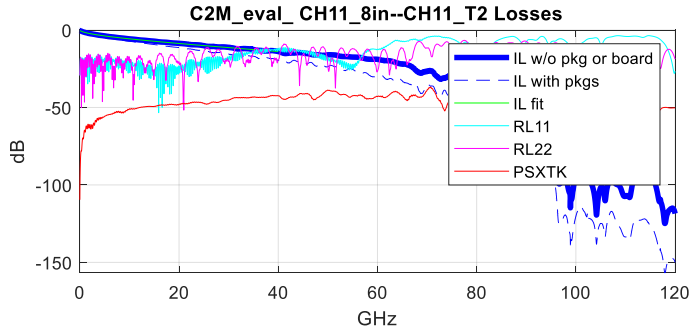
***Notes:***

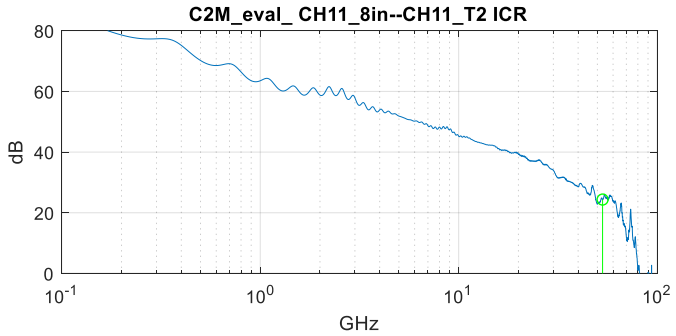
- ***Key changes are marked in yellow.***
- ***COM v3.70 was used in this study.***

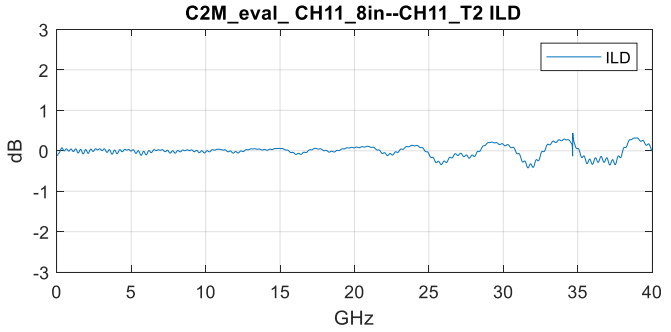
# Preliminary 212.5 Gbps PAM4 COM Analysis (CH11)

## TP1a

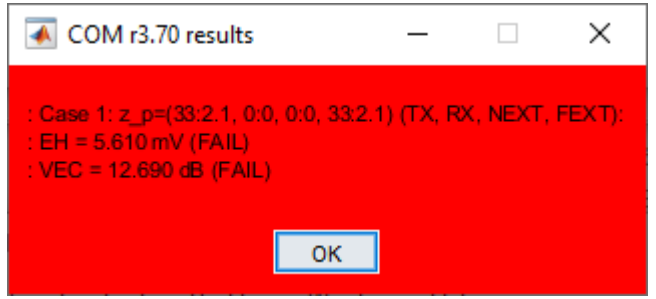


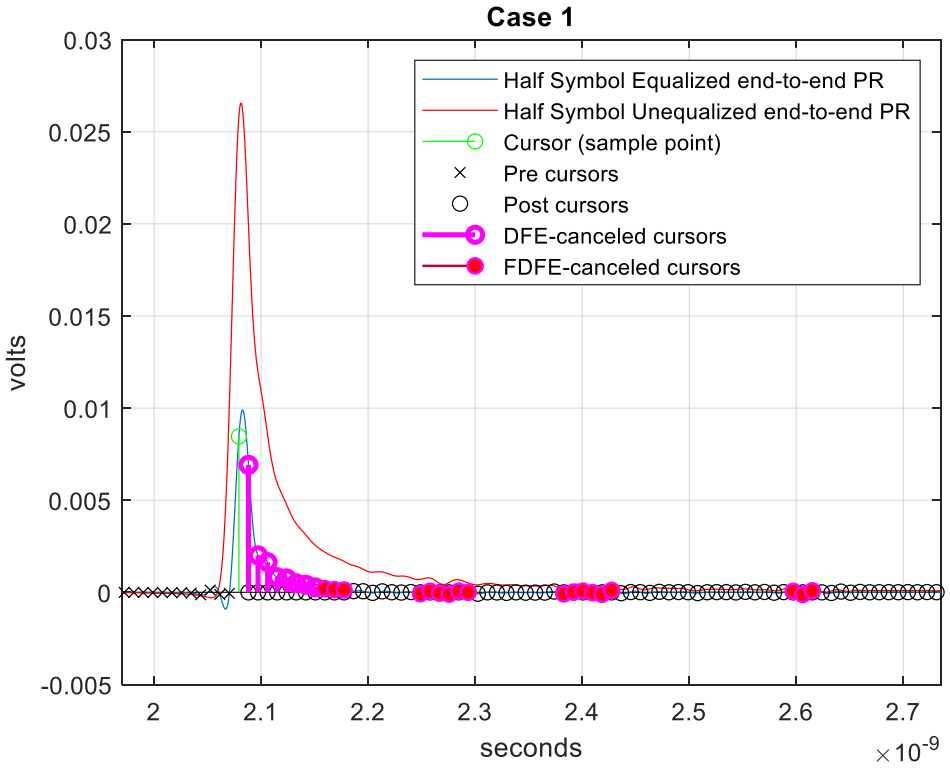



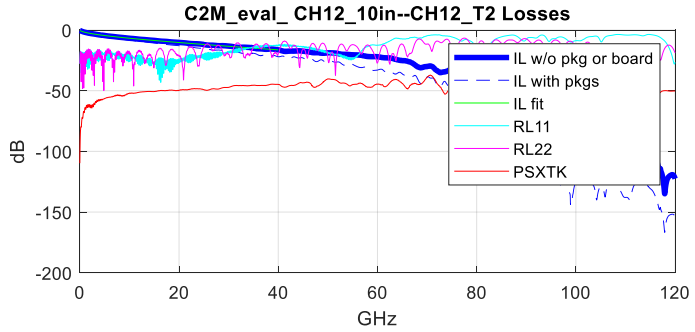

- DFE Taps = 8 + 6x3
- EH = 5.61 mV
- VEC = 12.69dB
- DER = 1e-6
- COM = 2.29dB

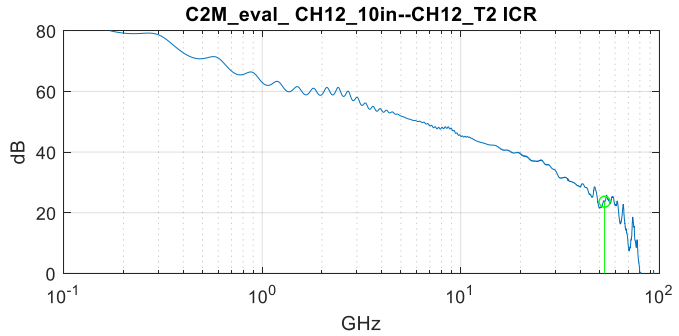


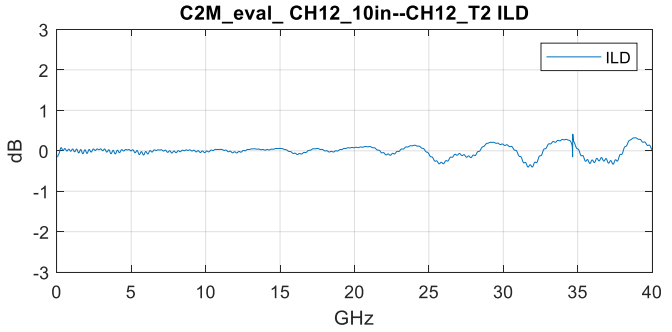
# Preliminary 212.5 Gbps PAM4 COM Analysis (CH12)

## TP1a

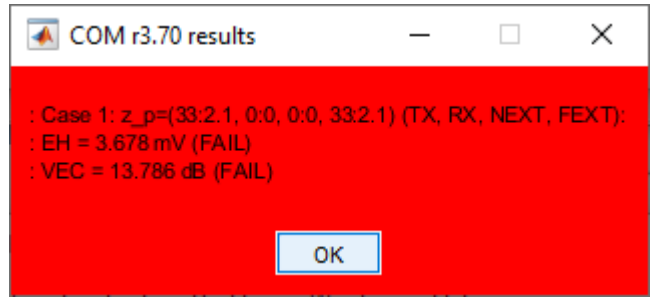


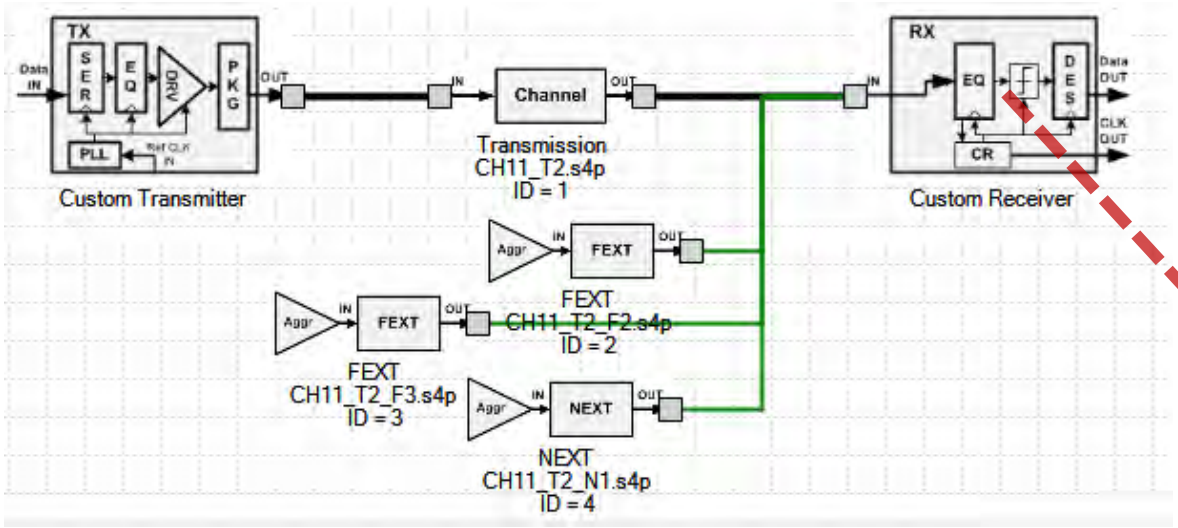



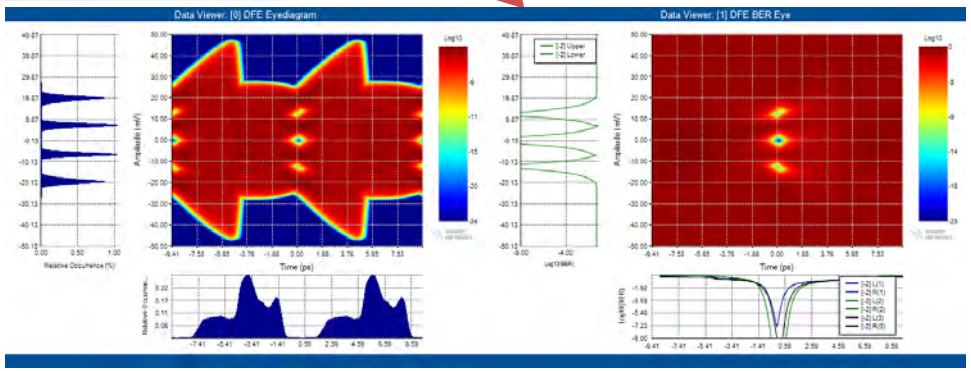

- DFE Taps = 8 + 6x3
- EH = 3.68 mV
- VEC = 13.79 dB
- DER = 1e-6
- COM = 1.99dB



# 212.5 Gbps PAM4 C2M TP1a Simulation (CH11)




**Changes are in red**



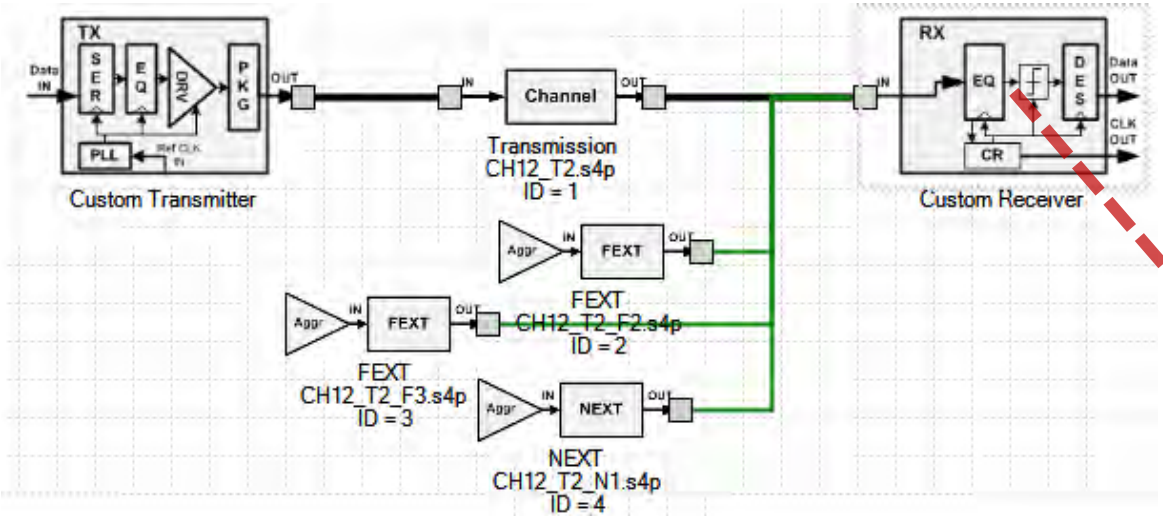

**TP1a RX output**
**EH = 3.63mV, EW = 0.11UI VEC = 8.78dB**
**@ DER=1e-6**

Simulation Configuration

- Test Pattern: QPRBS13-CEI
- Transmitter: Proposed CEI-224G-VSR-PAM4 reference TX, die, and package
  - RLM = 0.95, $SNR_{TX}$=33dB, BUJ = 0.02$UI_{pk}$, RJ = 0.01$UI_{RMS}$
  - 20%-80% Rise/Fall Time (*T_r*): ~3ps (*i.e. 0.31875x UI*)
  - TX Package:
    - Zp = 33mm, Zp2 = 2.1mm (to support high-density/radix switch)
    - a0 a2, and Cp updated to reflected the latest design (see COM table)
- TP1a Reference Receiver (Scope)
  - Based on scaled 802.3ck CR/C2M reference RX with DFE (8 fixed and 6 groups of 3 consecutive floating taps up to 80 UI), and Input Referred Noise = 5x$10^{-9}$ $V^2$/GHz*
- Channel: C2M channel with 2 FEXTs and 1 NEXT
- DER = $10^{-6}$

*Notes: *: RX optimizes signal-to-noise-and-distortion ratio for CDR and EQ.*

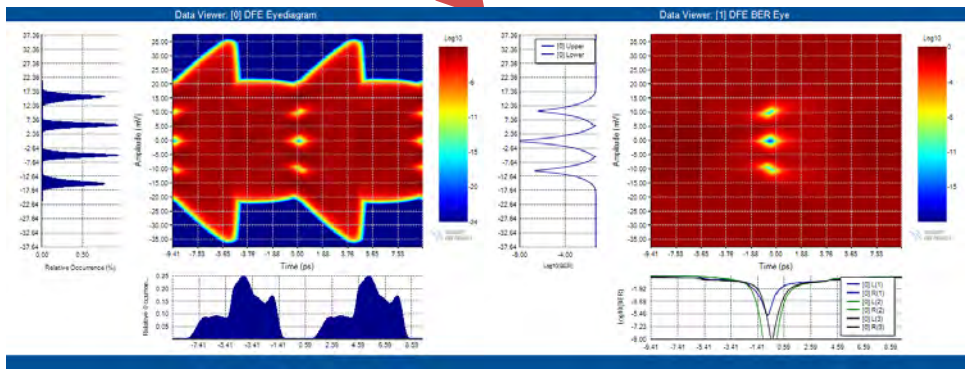
# 212.5 Gbps PAM4 C2M TP1a Simulation (CH12)




**Changes are in red**

Simulation Configuration

- Test Pattern: QPRBS13-CEI
- Transmitter: Proposed CEI-224G-VSR-PAM4 reference TX, die, and package
  - RLM = 0.95, $SNR_{TX}$=33dB, BUJ = 0.02$UI_{pk}$, RJ = 0.01$UI_{RMS}$
  - 20%-80% Rise/Fall Time (*T_r*): ~3ps (*i.e. 0.31875x UI*)
  - TX Package:
    - Zp = 33mm, Zp2 = 2.1mm (to support high-density/radix switch)
    - a0 a2, and Cp updated to reflected the latest design (see COM table)
- TP1a Reference Receiver (Scope)
  - Based on scaled 802.3ck CR/C2M reference RX with DFE (8 fixed and 6 groups of 3 consecutive floating taps up to 80 UI), and Input Referred Noise = 5x$10^{-9}$ $V^2$/GHz*
- Channel: C2M channel with 2 FEXTs and 1 NEXT
- DER = $10^{-6}$




**TP1a RX output**
**EH = 2.34mV, EW = 0.10UI VEC = 10.08dB @ DER=1e-6**

*Notes: *: RX optimizes signal-to-noise-and-distortion ratio for CDR and EQ.*

# Summary & Conclusions

**COM and Link Simulation Result Summary**
**212.5 Gbps PAM4**

| DER | Channel | COM EH | COM VEC | Simulation Eye Opening Height | Simulation VEC |
|---|---|---|---|---|---|
| $10^{-6}$ | CH11 | 5.61 mV | 12.69 dB | 3.63 mV | 8.78 dB |
| | CH12 | 3.68 mV | 13.79 dB | 2.34 mV | 10.08 dB |
| $10^{-5}$ | CH11 | 7.64 mV | 10.01 dB | 4.44 mV | 7.52 dB |
| | CH12 | 5.49 mV | 10.89 dB | 3.04 mV | 8.62 dB |
| $10^{-4}$ | CH11 | 9.93 mV | 7.73 dB | 5.47 mV | 6.16 dB |
| | CH12 | 6.99 mV | 8.21 dB | 3.91 mV | 7.04 dB |

# Summary & Conclusions *(cont.)*

- Preliminary COM and time-domain simulations with updated Intel/Amphenol C2M channels, reference package, and COM configuration,  suggest reasonable 212.5 Gbps C2M TP1a performance/solution space with PAM4 modulation scheme.
- Given that 212.5 Gbps chip-to-module channel's IL is approaching that of conventional KR/CR, more capable reference receiver, e.g., stronger EQ and smaller noise, are needed for plausible solution, as had demonstrated in this investigation.
- Further investigations on channel improvements and alternative reference RX giving better performance are planned.