Supporting presentation to comment #I-15 to D3.0 of P802.3df

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Introduction

Comment #12 was submitted by author to D2.0 to address potential inconsistencies in amount of MPI penalty between 500m and 2km specifications

Cl **124** *SC* **124.7.3** *P* **110** *L* **16** # 12

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Comment Type **TR** *Comment Status* **D** *penalties*

In clause 124, Table 124-8, for 400G-DR4 and 800G-DR8, the allocation for penalties is 3.5 dB, whereas for 400G-DR4-2 and 800G-DR8-2 it is 3.8 dB.
The difference of 0.3 dB seems to originate from the FR4 spec in Clause 151, which is potentially suffering a higher MPI penalty due to larger individual reflections in an FR4 configuration compared to a DR4/DR8 configuration.
Because it was agreed (during the TF phase) to use the same list of requirements for discrete reflectances as shown in in-force Table 124-13, also the same (lower) allocation for MPI penalty can be assumed for DR4/DR8 and DR4-2/DR8-2.

SuggestedRemedy

In Table 124-8, in the columns for 400GBASE-DR4-2 and 800GBASE-DR8-2, change the allocation for penalties from 3.8 dB to 3.5 dB.
Furthermore change Tx min power from x to y and Rx sensitivity from a to b. A supporting presentation will be provided for the comment resolution meeting

Proposed Response *Response Status* **W**

PROPOSED ACCEPT IN PRINCIPLE.
A presentation will be available for task force discussion.
Pending review of presentation and task force discussion.

Rejection of comment #12

During D2.0 comment resolution it was agreed to reject this comment because during discussion it appeared incomplete.

REJECT.

The following presentation was reviewed by the comment resolution group:
https://www.ieee802.org/3/df/public/23_0523/stassar_3df_01_230523.pdf

Based on further discussion, the information presented in stassar_3df_01_230523 appeared to be incomplete.

There was no consensus to make a change at this time.

The commenter is invited to prepare a more complete proposal for the review against a future draft.

Illustrative power budget in D2.0 Clause 124

Table 124–8—400GBASE-DR4, 800GBASE-DR8, 400GBASE-DR4-2, and 800GBASE-DR8-2 illustrative link power budgets

Parameter	400GBASE-DR4 800GBASE-DR8	400GBASE-DR4-2 800GBASE-DR8-2	Unit
Power budget (for max TDECQ)	6.5	7.8	dB
Operating distance	500	2000	m
Channel insertion loss[a]	3	4	dB
Maximum discrete reflectance	See 124.11.2.2	See 124.11.2.2	dB
Allocation for penalties[b] (for max TDECQ)	3.5	3.8	dB
Additional insertion loss allowed	0	0	dB

[a] The channel insertion loss is calculated using the maximum distance specified in Table 124–5 and cabled optical fiber attenuation of 0.5 dB/km at 1304.5 nm plus an allocation for connection and splice loss given in 124.11.2.1.
[b] Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested.

For x00GBASE-DR4y the total penalty allocation is 3.5 dB, whereas for x00GBASE-DRy-2 it is 3.8 dB, the difference being an additional allocation of 0.3 dB. Additional MPI penalty 0.2 dB and 0.1 dB DGD penalty. Thanks to Gary Nicholl identifying the DGD penalty allocation.

The allocation of 3.8 dB seems to have been taken from 100GBASE-FR1 in Clause 140.

While it makes sense to base x00GBASE-DRy=2 on 100GBASE-FR1, the channel discrete reflection conditions are different.

x00GBASE-DRy versus 100GBASE-DR1 discrete reflectances

Table 124–13—Maximum value of each discrete reflectance

Number of discrete reflectances above –55 dB	Maximum value for each discrete reflectance
1	–37 dB
2	–42 dB
4	–45 dB
6	–47 dB
8	–48 dB
10	–49 dB

Table 140–15—Maximum value of eac

Number of discrete reflectances above –55 dB	Maximum value for eac
	100GBASE-FR1
1	–25
2	–31
4	–35
6	–38
8	–40
10	–41

Previously it was agreed that the same maximum discrete reflectance applies to all x00GBASE-DRy (both 500m and 2km applications).

This maximum level is significantly higher for 100GBASE-FR1 and therefore the allocation of a higher MPI penalty (+0.2 dB) and DGD penalty (0.1 dB) is very appropriate for this case.

Considering that for all x00GBASE-DRy codes the maximum discrete reflectance in the channel is the same, the author suggests the TF to use the same allocation for MPI penalty.

Recommendations

- In Table 124-8 change the allocation for penalties for 400GBASE-DR4-2 and 800GBASE-DR8-2 from 3.8 dB to 3.6 dB.
- Further recommendations: split the “gain” of 0.2 dB over Tx and Rx power levels, thus decreasing Tx minimum OMA and / or increase the Rx sensitivity. How much? TBD and for discussion within the TF.
- Strawman proposal to allocate the “gain” to the receiver only:
  - Increase Receiver sensitivity (OMA_{outer}), each lane (max) by 0.2 dB from –4.5 dBm to –4.3 dBm and from –5.9 +TECQ dBm to –5.7 +TECQ dBm for both Receiver sensitivity values
- For those worried about inconsistency with 100GBASE-FR1, there is the choice for the implementers to follow the 100GBASE-FR1 specification while meeting the narrower budget at the same time.

Details of proposed modifications

In Table 124-7, for 400GBASE-DR4-2 and 800GBASE-DR8-2, change to:

- Receiver sensitivity (OMA_{outer}), each lane (max)
  - For TECQ < 1.4 dB to “–4.3 dBm”
  - For 1.4 dB ≤ TECQ ≤ 3.4 dB to “–5.7 + TECQ dBm”
- Stressed receiver sensitivity (OMAouter), each lane max
  - To “–2.3 dBm”

In Table 124-8, for 400GBASE-DR4-2 and 800GBASE-DR8-2, change:

- Power budget (for max TDECQ) to “7.6 dB”.
- Allocation for penalties (for max TDECQ) to “3.6 dB”

Revise Figure 124–2b, Figure 124–2c, and Figure 124–2d accordingly, with editorial license.

Thanks!