# COM analysis of contributed C2M channels – towards a 200 Gb/s per lane AUI proposal

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### Intro

- For a C2M baseline proposal we need to agree on channels and endpoint assumptions
- Effects on the architecture should also be considered
- This presentation addresses
  - What channels are feasible
  - What error statistics can be expected
  - What would it take

## Previous work

- Several sets of AUI channels have been contributed
  - <u>akinwale 3df 01 2209</u>, <u>akinwale 3df 02 2209</u>, <u>akinwale 3df 03 2209</u> (chip to module, range of losses)
  - mellitz 3df 02 2207 (chip to chip)
  - <u>rabinovich 3df 01 2209</u>, <u>rabinovich 3df 01 2209</u> (chip to module) (+some earlier contributions)
- <u>mli 3df 02a 220316</u> proposes die termination and package model
- <u>benartsi 3df 01b 2207</u> proposes model and parameters for largescale switch package
- kareti 3df 01a 2207 suggests large-scale switch applications may need 36-38 dB die to die

# Goals of this presentation

- Propose a set of COM parameters (and a configuration spreadsheet) for 200 Gb/s AUI application
- Propose a loss budget for C2M
- Highlight effects on the 802.3dj architecture beyond electrical specifications

## Method

- 1. Define channel construction for C2M simulation
- 2. Identify the key COM parameters for a selected subset of C2M channels
- 3. Propose a set of values for these parameters (operating point)
- 4. Examine sensitivity around the working point
- 5. Run COM on the full set of channels

# Channel construction



# Channel set for operating point selection

Channel #	Source	File/folder Name(s)	IL [dB] @ 56.125 GHz (Thru, BGA to BGA)	IL [dB] including packages (min, max)	
1-3	rabinovich_3df_02_2209	Rabinovich_C2M_200G_Paral_*mil_092122 [19, 67, 93]	12.3, 13.3, 13.4	21.3 – 26.4	
4-5	mellitz_3df_02_2207	TA_6002_6003 TA_6002_6003_tp0_tp5	13.9 24.3	22.9 – 37.3	
6-12	akinwale_3df_02_2209	C2M_PCB_93ohms_*dB_202208016_v2 [10, 15, 20, 22, 24, 26, 28]	8.8, 13, 18.1, 20.6, 22.3, 24.9, 26.6	17.8 – 39.9	

15 mm / 30 mm host packages and module package add 9 / 13 dB to each channel (without die models)

# Key parameters

- Initial analysis identified the following parameters as having a large effect on COM:
  - η<sub>0</sub> (receiver input noise spectral density)
  - T<sub>r</sub> (transmitter bandwidth)
  - f<sub>r</sub> (receiver bandwidth)
  - Max b(1)
  - DER<sub>0</sub>

(other parameters that may also have a large effect, but are considered hard to change, were not included in the analysis)

- A set of values for these parameters, which makes two challenging channels have COM≈3 dB, was defined as the "operating point"
  - Channel # 5 (37.3 dB die-to-die)
  - Channel #10 (35.3 dB die-to-die)

# Proposed values for key parameters

Parameter	In 100GBASE-CR (Clause 162)	In 100GAUI-1 C2C (Annex 120F)	Proposed Value for 200GAUI	Rationale
η <sub>0</sub> [V²/GHz]	9e-9	2e-8	4e-9	About the same RMS with doubled bandwidth. Related to package xtalk, thermal and device noise; Challenging but achievable
T <sub>r</sub> [ps]	7.5	7.5	6	Silicon switching speed does not scale; improved only by process
f <sub>r</sub>	0.75*f <sub>b</sub> (≈40 GHz)	0.75*f <sub>b</sub> (≈40 GHz)	0.55*f <sub>b</sub> (≈58 GHz)	High bandwidth is challenging; lower BW improves COM results
bb <sub>max</sub> (1)	0.85	0.65	1	High value required for high loss channels; error propagation can be addressed
SNR <sub>TX</sub>	32.5	33	32.5	Increasing would burden design and has diminishing return on high loss channels
DER <sub>0</sub>	1e-4	1e-5	1e-4	RS544 with uncorrelated errors needs DER=4e-4 for FLR=1e-12 BER budgeting with a low portion for AUIs does not seem feasible (may be split between 2 AUIs)
N <sub>b</sub>	12	6	24	Scale with UI
N <sub>f</sub>	40	0	80	Scale with UI
Tx FFE length	5 (3 pre)	5 (3 pre)	6 (4 pre)	Compensate better for pulse rise time; relatively cheap to implement

#### Note: full proposed parameter table in the final slide

# COM results at operating point

Failing cases



# Implications

- DER0=1e-4 is close to the full RS544 correction capability
  - We need to enable error correction for the electrical segment alone
  - Operating with 1e-5 may be possible with lower loss channels in these cases it may be
    possible to bypass error correction
  - Possible solution: Flexible segmented / concatenated architecture
- Large value of  $b_{max}(1) \Rightarrow$  correlated errors are possible
  - If bit muxing is used, the actual BER will need to be much lower than DER<sub>0</sub>/2 to get equivalent FEC performance
  - Possible solution: **Symbol muxing PMA**
- Tx FFE values have a large variation over the channels considered (see backup)
  - This is for a specific reference receiver; real receivers may vary further
  - Tx parameters may need to be optimized per AUI channel/receiver
    - Module output too
  - Possible solution: Link training over the AUI segment

# Effect of $\eta_0$ $\eta_0$ [V²/GHz] sweep from 1e-9 to 9e-9 in 1e-9 step



### Effect of $T_r$ T<sub>r</sub> [ps] sweep from 3.5 to 7.5 in 0.5 step



### Effect of $f_r$ $f_r/f_b$ sweep from 0.4 to 0.75 in 0.05 step



### Effect of $bb_{max}(1)$ bb\_max(1) sweep from 0.5 to 1 in 0.1 step



# $\begin{array}{l} \mbox{Effect of SNR}_{TX} \\ \mbox{SNR}_{TX} \mbox{ sweep from 29 to 34 in 0.5 step} \end{array}$



### Effect of $DER_0$ DER<sub>0</sub> sweep from 1e-5 to 1e-3, 4 steps per decade



# Future work

- Fine-tune parameters with more channels
- Analyze the effect of bit/symbol muxing on FLR with given DER
- Consider electrical specification method for C2M
  - What should be similar to C2C / backplane
  - What should be different
- Address functional aspects
  - Symbol muxing
  - Link training on AUIs within a segmented link (optical/electrical)

# Summary

- Feasibility of contributed C2M channels with die-to-die IL from 18 dB to 37 dB has been demonstrated by COM analysis
- An operating point for key parameters is proposed
- Implications beyond electrical specifications must be considered
  - FEC scheme
  - Symbol muxing
  - Link training on AUI

# Proposed COM spreadsheet (operating point)

ParameterSettingUnitsInformation11002662010.0267202.00.0267202.00.0267202.00.027002.00.027002.00.027002.00.027002.00.027002.00.027002.00.027002.00.020002.00.020002.00.0200002.00.020.020002.00.020.0200002.00.020.0200002.00.020.0200002.00.020.0200002.00.020.000002.00.020.000003.00.00000003.00.00000003.00.00000003.00.00000003.00.00000003.00.00000003.00.000000<	Table 93A-1 parameters			I/O control		Table 93A–3 parameters				Float		
Lb         158.75         6.84            Lm         0.02         CH <th>Parameter</th> <th>Setting</th> <th>Units</th> <th>Information</th> <th>DIAGNOSTICS</th> <th>1</th> <th>logical</th> <th>Parameter</th> <th>Setting</th> <th>Units</th> <th>N_bg</th> <th></th>	Parameter	Setting	Units	Information	DIAGNOSTICS	1	logical	Parameter	Setting	Units	N_bg	
Left0.0220%0%0%Cobst0.0020%	f_b	106.25	GBd		DISPLAY_WINDOW	0	logical	package_tl_gamma0_a1_a2	[0 1.33e-3 3.9525e-4]		N_bf	
Defa         ODC         OH         TX AC         Max         State (SUC) DIR         Vessel (Suc) (SUC	f_min	0.02	GHz		CSV_REPORT	1	logical	package_tl_tau	6.420E-03	ns/mm	N_f	
C_d         4409 0100 4090 10071s-6         rf         (T/K R)           L s         0130 103 40, 400 50.5341         rf         (T/K R)           C b         031 40 50, 40, 400 50.5414         rf         (T/K R)           r_prott         1.2         (T/K R)	Delta_f	0.02	GHz		RESULT_DIR	.\results\{date}\	Path	package_Z_c	[94 94; 90 90; 200 200; 70 70]	Ohm	bmaxg	
L. 5         D132 03 04 0.03 03 03 0.01         PM         T/T RM           L. 5         D134 03 03 04 0.03 03 03 0.01         PM         T/T RM         R	C_d	[40 90 110; 40 90 110]*1e-6	nF	[TX RX]	SAVE_FIGURES	0	logical	ICN & FOM_ILD parameters			N_tail_start	
C.b.UD24-03-04nfUT R0R1R1 Ref Case 1 on 04R1C2M, eval.R1R1C371Git $f_{\pm}$ spectred in fract ours 1 ours1 g. p(N2)15 Sic 2.2 0.18 0.80, 0.00.01mn[lett cases](lett cases)(lett cases) <t< td=""><td>L_s</td><td>[0.13 0.15 0.14; 0.13 0.15 0.14]</td><td>nH</td><td>[TX RX]</td><td>Port Order</td><td>[1324]</td><td></td><td>f_v</td><td>0.371</td><td>*Fb</td><td>B_float_RSS_MAX</td><td></td></t<>	L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]	Port Order	[1324]		f_v	0.371	*Fb	B_float_RSS_MAX	
$L_p$ prix(12)(1et) (test cases to val)000 </td <td>C_b</td> <td>[0.3e-4 0.3e-4]</td> <td>nF</td> <td>[TX RX]</td> <td>RUNTAG</td> <td>C2M_eval_</td> <td></td> <td>f_f</td> <td>0.371</td> <td>GHz f_r specified in first column</td> <td></td> <td></td>	C_b	[0.3e-4 0.3e-4]	nF	[TX RX]	RUNTAG	C2M_eval_		f_f	0.371	GHz f_r specified in first column		
$L_p$ [NX][153] 22, 218, 0138, 00.03]mm[1ct class] $2$ $2$ $1$ <th< td=""><td>z_p select</td><td>[1 2]</td><td></td><td>[test cases to run]</td><td>COM_CONTRIBUTION</td><td>0</td><td>logical</td><td>f_n</td><td>0.371</td><td>GHz</td><td></td><td></td></th<>	z_p select	[1 2]		[test cases to run]	COM_CONTRIBUTION	0	logical	f_n	0.371	GHz		
$z_p(FKT)$ [66, 0.050; 0.10, 0.050, 0.01]mm[fet case]Operational $A_n^R$ 0.600V $z_p(FKT)$ [15, 0.22, 0.12, 0.02, 0.01]mm[fet case]0 $A_n^R$ 0.600V $C_p$ [8-6]0m[Tx R)0000000 $R_0$ 0.500(Tx R)00 </td <td>z_p (TX)</td> <td>[15 30; 2 2; 0.18 0.18; 0.5 0.5 ]</td> <td>mm</td> <td>[test cases]</td> <td>Local Search</td> <td>2</td> <td></td> <td>f_2</td> <td>58.4375</td> <td>GHz</td> <td></td> <td></td>	z_p (TX)	[15 30; 2 2; 0.18 0.18; 0.5 0.5 ]	mm	[test cases]	Local Search	2		f_2	58.4375	GHz		
L.p. (PKT)         (15.80) 22, 0.128, 0.128, 0.40.4)         mm         (let c.ose)         (let c.ose	z_p (NEXT)	[66;0.50.5;0.180.18;0.40.4]	mm	[test cases]	Operational			A_ft	0.600	v		
$  z_{e}   R X  $ $  fest 20.5 x_{2}, 0.5 x_{2}, 0.5 x_{3}, 0.5 x_{4}, 0.5 x_{3}, 0.5 x_{4}, 0.5 x_{3}, 0.5 x_{4}, 0.5 x_{3}, 0.5 x_{4}, 0.5$	z_p (FEXT)	[15 30; 2 2; 0.18 0.18; 0.5 0.5 ]	mm	[test cases]	COM Pass threshold	3	dB	A_nt	0.600	V		
C_p         [Re-60]         nf         [T K K]         [R] Pass therebold         7.3         dB         [Histgarm, Window, Weight         Guassian         gaassian, triangle, rectangle           R, d         (50 50)         Ohm         Tr         6.00C-63         ns         1.00C-64	z_p (RX)	[66;0.50.5;0.180.18;0.40.4]	mm	[test cases]					•			
R, 050OhmDR0R, d[505]Ohm[Tx R]A, v0.413VDER.01.006-04A, le0.608VIA, le0.608VIL4MDER.01.006-04L4MDER.01.006-04M3.2Samp/UBER.0.CNM850logicalT, O50mUIBBE.0.CNM850logicalT, O50mUBER.0logical2.1030.007.9T, O50mUIlogical2.2 by (N)407mmFiter and FqIlogicalIlogical2.2 by (N)407mmC(1)(0.340.020)IIminstepmatiRT RT DR0.01nFC(2)(0.02.02.01)IIminstepmatinG_A/dft1logicalC,10h_max0.4121.0040logicalC,10nFC(1)(0.10.02.01)IminstepmatinG_A/dft1logicalC,10nFh_max0.3A/dffc1Nbx0UNbx0Uh_max0.4040UNbx0UIndude PCB0logicalb_max0.3A/dffc1Nbx0UIndude PCB0logicalh_f z4.25GHzNbx0UIndude PCB0logicalb_max0.00UIminstepmatiNbx0<	С_р	[8e-6 0]	nF	[TX RX]	ERL Pass threshold	7.3	dB	Histogram_Window_Weight	Gaussian	gaussian. triangle, rectangle		
R A(150 50) AOhm(Tr R) T CDBR, 01.00E A1.00E C1.00E 1.00E C1.00E 1.00E C <t< td=""><td>R_0</td><td>50</td><td>Ohm</td><td></td><td></td><td></td><td></td><td>sigma_r</td><td>0.02</td><td>sigma in UI fo or gaus Wind</td><td></td><td></td></t<>	R_0	50	Ohm					sigma_r	0.02	sigma in UI fo or gaus Wind		
$A_v$ $0.413$ $V$ $T_r$ $6.063$ $ns$ $A_ne$ $0.668$ $V$ $V$ $V$ $V$ $L$ $A$ $A$ $V$ $V$ $V$ $L$ $A$ $A$ $V$ $V$ $V$ $V$ $M$ $3.2$ $Samp/U$ $V$ $V$ $V$ $V$ $V$ $r_0$ $50$ $mU$ $V$ $V$ $V$ $V$ $V$ $V$ $r_0$ $50$ $mU$ $V$ $V$ $V$ $V$ $V$ $V$ $RCC$ $RVS$ $0$ $V$ $V$ $V$ $V$ $V$ $V$ $r_1$ $0.55$ $mU$ $V$ $V$ $V$ $V$ $V$ $V$ $RTR$ $1$ $V$	R_d	[50 50]	Ohm	[TX RX]	DER_0	1.00E-04						
$A, fe$ $0.413$ $V$ $A, fe$ $0.608$ $V$ $L$ $4$ $ L$ $4$ $ L$ $4$ $ L$ $4$ $ M$ $32$ $Samp/U$ $ BEAD_CRUMBS$ $0$ $logical$ $T_O$ $50$ $ T_O$ $50$ $ T_O$ $50$ $ fr$ $0.55$ $ fr$ $0.55$ $ fr$ $0.55$ $ fr$ $0.55$ $ (-1)$ $(0.20.20)$ $(minstepmat)$ $(-1)$ $(0.20.20)$ $(minstepmat)$ $(-1)$ $(0.20.20)$ $(minstepmat)$ $(-1)$ $(0.20.20)$ $(minstepmat)$ $h_{D,mat(1)$ $3$ $A_s/dfe1$ $b_{mat(1)$ $0.3$ $A_s/dfe1$ $b_{mat(1)$ $0.3$ $A_s/dfe1$ $b_{mat(1)$ $0.3$ $A_s/dfe1$ $f_1$ $2.50$ $f_1$ $2.25$ $d_1$ $boldsi$ $f_2$ $42.5$ $f_1$ $0.66$ $f_1$ $0.66$	A_v	0.413	V		T_r	6.00E-03	ns	Table 92–12 parameters				
$ \begin{array}{ c c c c c c c c c c c c c c c c c c c$	A_fe	0.413	V		FORCE_TR	1	5	Parameter	Setting			
L4-M32Samp/Usamples_for_C2M100Samp/UT_050mUT_050mU $A \subseteq CM_RMS$ 0Vfilterand Eqf.fr0.55*Dc(-1)[03.00.250][minstep:max]c(-2)[0.00.22.14][minstep:max]c(-3)[-0.00.20.30][minstep:max]c(-3)[-0.00.20.30][minstep:max]c(-3)[-0.00.20.30][minstep:max]nb_max(1)1As/dfe1.b_max(1)1As/dfe1.b_max(1)1As/dfe1.b_max(1)1As/dfe1.b_max(1)1As/dfe1.b_max(2,N_b)0.3As/dfe1.f_r242.5GHzf_r2106.25GHzf_r2106.25GHzf_r2106.25GHzf_r220.06GHzf_r220.06GHzf_r20.66GC, HPZ0.66GC, HPZ0.66	A_ne	0.608	V		PMD_type	C2C		board_tl_gamma0_a1_a2	[0 3.8206e-04 9.5909e-05]			
M32Sam/UIsamples for C2M1000Sam/UIisamples for C2M1000Sam/UITO50mUIAC CM EMS0VTest casefifter and faIIIogicalf. fr0.35minc(1)(0.34.0.020)[min:step:max]f. (2)100.02.014)[min:step:max]c(2)100.02.014)[min:step:max]c(3)(0.60.022)[min:step:max]f. (4)10.00.013[min:step:max]kmax(1)1Ac/dfe1b_max(1)1Ac/dfe1b_max(1)0.3Ac/dfe1b_max(1)0.3Ac/dfe1b_max(1)0.3Ac/dfe1b_max(1)0.3Ac/dfe1b_max(2,Nb)0.3Ac/dfe1b_max(2,Nb)0.3Ac/dfe1f. f. 2306.55G. C.143.48d, f. p.2306.55f.	L	4			BREAD_CRUMBS	0	logical	board_tl_tau	0.00579	ns/mm		
samples for C2M         100         Samp/U           T_O         S0         mU $\square$ AC_CM_RMS         0         V         [test case] $\square$ $\square$ filter and Eq $\square$ $\square$ $\square$ $\square$ $\square$ f(tr and Eq $\square$ $\square$ $\square$ $\square$ $\square$ f(tr and Eq $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ f(tr) $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ f(tr) $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ $\square$ f(tr) $\square$	М	32	Samp/UI		SAVE_CONFIG2MAT	1	logical	board_Z_c	100	Ohm		
T.O.S0MUITDR and ERL optionsTDR and ERL optionsLo $AC_CM_RMS$ 0V[test case]TDR1logical $2_{DP}$ (PKT)407mm $f_{T}$ 0.55fbERL1logical $2_{DP}$ (PKX)407mm $c(:1)$ $[c0360020]$ ministepmax]FR_DNLY0logical $C_O$ 0nF $c(:2)$ $[0.002.01.4]$ ministepmax]ministepmax]N12001Include PCB0logical $c(:4)$ $[0.010.03]$ ministepmax]fixture delay time $[0.0]$ [port] port]fixture delay time $[0.0]$ [port] port]fixture delay time $[0.0]$ [port] port]include PCB0logical $b_max[2.N_b)$ 0.3 $A_{S}/dfe1.N_b$ Nb0UITukey_Window1Tukey_WindowTukey_WindowTukey_WindowTukey_WindowNb $f_{T}$ $A_{25}$ $GHz$ Sigma BN Step $5.0E-03$ VNbSigma BN Step $5.0E-03$ V $f_{T}$ $A_{25}$ $GHz$ Sigma BN Step $5.0E-03$ VSigma BN Step $5.0E-03$ V $f_{T}$ $A_{25}$ $GHz$ Sigma RN 0.01UIUISigma RN 0.01UI $f_{T}$ $A_{25}$ $GHz$ Sigma RN 0.01UISigma RN 0.01UI $f_{T}$ $A_{25}$ $GHz$ Sigma RN 0.01UISigma RN 0.02UI $f_{T}$ $f_{2.0}$ $f_{2.0}$ $f_{2.0}$ $f_{2.0}$ <t< td=""><td>samples_for_C2M</td><td>100</td><td>Samp/UI</td><td></td><td>PLOT_CM</td><td>0</td><td>logical</td><td>z_bp (TX)</td><td>407</td><td>mm</td><td></td><td></td></t<>	samples_for_C2M	100	Samp/UI		PLOT_CM	0	logical	z_bp (TX)	407	mm		
AC_CM_RMS       0       V       [text cases]       TDR       1       logical $z_b p(FEXT)$ 407       mm         filter and Eq	T_0	50	mUI		TDR and ERL options			z_bp (NEXT)	407	mm		
filter and Equu $[r]$ 0.55"fb $(c)$ 0.55min $(c(-1)$ $[-0.34.00.20]$ $[minstep:max]$ $(c(-1)$ $[-0.36.00.20]$ $[minstep:max]$ $(c(-2)$ $[0.06.00.20]$ $[minstep:max]$ $(c(-4)$ $[0.06.00.20]$ $[minstep:max]$ $(c(-4)$ $[0.06.00.20]$ $[minstep:max]$ $(c(-4)$ $[0.06.00.20]$ $[minstep:max]$ $(c(-4)$ $[0.01.0.02]$ $[minstep:max]$ $(c(-4)$ $[0.01.0.02.0]$ $[minstep:max]$ $(r)$ $2.4$ $U$ $b_{max}(1)$ 1 $As/dfe1$ $b_{max}(1)$ 1 $As/dfe1$ $b_{min}(2.N,b)$ $-0.15$ $As/dfe1$ $b_{min}(2.N,b)$ $-0.15$ $As/dfe1$ $b_{min}(2.N,b)$ $-0.15$ $As/dfe1$ $f_{p2}$ $10.62.5$ $GHz$ $f_{p2}$ $10.62.5$ $GHz$ $f_{p2}$ $10.62.5$ $GHz$ $f_{p2}$ $10.62.5$ $f_{p2}$ $10.62.5$ $f_{p1}$ $A_{2.55.0$ $f_{p2}$ $10.65.50$ $f_{p1}P2$ $0.66$ $GHz$ $R_{LM}$ $0.502$ $R_{LM}$	AC_CM_RMS	0	V	[test cases]	TDR	1	logical	z_bp (FEXT)	407	mm		
f_r0.55*fbC0logicalC,00nFc(1)(0.340 020)(minstep:max)(minstep:max)N1200N11c(-2)(0.00.20.34)(minstep:max)(minstep:max) $b ta x$ 01110110111 $b ta x$ 01111 $b ta x$ 01111 $b ta x$ 01111 $b ta x$ 0111 $b ta x$ 01111 $b ta x$ 0111 $b ta x$ 011111 $b ta x$ 011111111111111111111111 <t< td=""><td>filter and Eq</td><td></td><td></td><td></td><td>ERL</td><td>1</td><td>logical</td><td>z_bp (RX)</td><td>407</td><td>mm</td><td></td><td></td></t<>	filter and Eq				ERL	1	logical	z_bp (RX)	407	mm		
C(0)         0.5         min         TR_TDR         0.01         ns         C_1         0         nF           c(-2)         [0.0.02.0.14]         [min:step:max]         N         1200         Include PCB         0         Include	f_r	0.55	*fb		ERL_ONLY	0	logical	C_0	0	nF		
C(-1)         [-0.34.0.02.0]         [min:step:max]         N         1200         Include PCB         0         logical           c(-2)         [0.0.02.0.14]         [min:step:max]         min.step:max]         min.step:max	c(0)	0.5		min	TR_TDR	0.01	ns	C_1	0	nF		
c(-2)         [00.020.3.14]         [min:step:max]           c(-3)         [-0.06.0.02.0]         [min:step:max]           c(-4)         [00.01.0.03]         [min:step:max]           c(1)         [01.0.0.03]         [min:step:max]           c(1)         [-0.1:0.02:0]         [min:step:max]           b_max[1)         1         As/dffe1           b_max[2,N_b)         0.3         As/dffe1           b_min(2N_b)         0.15         As/dffe1           f_2         42.5         GHz           f_p2         106.25         GHz           f_p2         106.25         GHz           f_p2         0.6.         GHz           f_p1P         F[-30.5:0]         [min:step:max]           f_p1P         0.6.         GHz	c(-1)	[-0.34:0.02:0]		[min:step:max]	N	1200		Include PCB	0	logical		
$c(-3)$ $[-0.06; 0.02:0]$ $[min:step:max]$ $mo_x$ $0.618$ $min:step:max]$ $c(-4)$ $[0.0.01; 0.03]$ $[min:step:max]$ $[fixture delay time[0 0][port]c(1)[-0.1:0, 02:0][min:step:max][fixture delay time[0 0][port]N_b24UTDR_W_TXPKG0UIb_max(2.N_b)0.3As/dffe1N_b x0UIb_min(1)0.3As/dffe1.Rceiver testingRt_CALIBRATION0b_min(2.N_b)-0.15As/dffe1.Sigma BBN step5.00c-03Vg_DC[18:1:-8]dB[min:step:max]Sigma_R U0.01UIf_f z42.5GHzNoise, jitterIitterIitterf_f p110c.25GHzSNN_T TX32.5dBf_F P20.6GHzR_LM0.95Iitter$	c(-2)	[0:0.02:0.14]		[min:step:max]	beta_x	0						
c(-4)         [0:0.01:0.03]         [min:step:max]           c(1)         [-0.1:0.02:0]         [min:step:max]           N_b         24         Ul           b_max(1)         1         As/dffe1           b_max(2.N_b)         0.3         As/dffe1           b_min(1)         0.3         As/dffe1           b_min(2.N_b)         0.15         As/dffe1           b_min(2.N_b)         0.15         As/dffe1           b_min(2.N_b)         0.15         As/dffe1           f_r         4.3/dffe1         R2_CALIBRATION         0         logical           sigma BBN step         5.00E-03         V           Noise, jitter         Ul         Noise, jitter         Ul           d_f_p2         10.625         GHz         SINR_TX         32.5         dB           f_HP_PZ         0.6         GHz         SINR_TX         32.5         dB	c(-3)	[-0.06:0.02:0]		[min:step:max]	rho_x	0.618						
c(1)         [-0.1:0.02:0]         [min:step:max]           N_b         24         UI           b_max(1)         1         N_bx         0         UI           b_max(2.N_b)         0.3         As/dff21         N_bx         0         UI           B_max(2.N_b)         0.3         As/dff21         Receiver testing         Max         <	c(-4)	[0:0.01:0.03]		[min:step:max]	fixture delay time	[0 0]	[ port1 port2 ]	different for each test fixture	1			
N_b         24         UI         M_bx         0         UI           b_max(1)         1         M_bx         0         UI           b_max(2.N_b)         0.3         As/dfe2.N_b         Tukey_Window         1         Image: Mark (Mark (M	c(1)	[-0.1:0.02:0]		[min:step:max]	TDR_W_TXPKG	0						
b_max(1)         1         As/dffe1           b_max(2.N_b)         0.3         As/dffe1           B_min(1)         0.3         As/dffe1           b_min(2.N_b)         0.0.15         As/dffe1           B_min(2.N_b)         0.0.15         As/dffe1           B_min(2.N_b)         0.0.15         As/dffe2.N_b         0           g_DC         [-18:1:-8]         dB         [min:step:max]         Sigma BBN step         5.00E-03         V           f_z         42.5         GHz         Noise, jitter         Noise, jitter         Noise, jitter           f_p2         106.25         GHz         A_DD         0.01         Uli           dEa_0         4.00E-09         V^2/GHz         SNR_TX         32.5         dB           f_HP_PZ         0.6         GHz         R_LM         0.95         KB	N_b	24	UI		N_bx	0	UI		-			
b_max(2N_b)         0.3         As/dfe2N_b         Receiver testing         Addition           b_min(1)         0.3         As/dfe1         RX_CALIBRATION         0         logical           b_min(2N_b)         -0.15         As/dfe2N_b         Sigma BBN step         5.00 - 03         V           g_DC         [-18:1:-8]         dB         [min:step:max]         Sigma BBN step         5.00 - 03         V           f_f_2         42.5         GHz         Sigma BBN step         0.01         UI           f_p1         42.5         GHz         Sigma_RJ         0.01         UI           f_p2         106.25         GHz         -         -         -           g_DC_HP         [-3:0.5:0]         [min:step:max]         SNR_TX         32.5         dB           f_HP_PZ         0.6         GHz         R_LM         0.95         -	b_max(1)	1		As/dffe1	Tukey_Window	1		updated for 802.3df/dj C2M				
b_min(1)         0.3         As/dffe1         RX_CALIBRATION         0         logical           b_min(2.N_b)         -0.15         As/dfe2.N_b         Sigma BBN step         5.00E-03         V           g_DC         (-181:1-8)         dB         (min:step:max)         Noise, jitter         V           f_z         42.5         GHz         As/dfe2         Noise, jitter         V           f_p1         42.5         GHz         A_DD         0.01         Ul           f_p2         106.25         GHz         A_DD         0.02         Ul           eta_0         4.00E-09         V^2/GHz         SNR_TX         32.5         dB           f_HP_PZ         0.6         GHz         R_LM         0.95         dB	b_max(2N_b)	0.3		As/dfe2N_b	Receiver testing							
b_min(2N_b)         -0.15         As/dfe2N_b         Sigma BBN step         5.00E-03         V           g_DC         (-18:1:-8)         dB         (min:step:max)         Noise, jitter         V           f_z         42.5         GHz          Noise, jitter         U           f_p1         42.5         GHz          A_DD         0.01         UI           f_p2         106.25         GHz          eta_0         4.00E-09         V^2/GHz           g_DC_HP         (-30.5:0)         (min:step:max)         SNR_TX         32.5         dB           f_HP_PZ         0.6         GHz         R_LM         0.95	b_min(1)	0.3		As/dffe1	RX_CALIBRATION	0	logical					
g_DC         [-18:1:-8]         dB         [min:step:max]         Noise, jitter         Mode           f_z         42.5         GHz         Sigma_RJ         0.01         Ul           f_p1         42.5         GHz         A_DD         0.02         Ul           f_p2         106.25         GHz         Edual         4.00E-09         V^2/GHz           g_DC_HP         [-3.0.5:0]         [min:step:max]         SNR_TX         32.5         dB           f_HP_PZ         0.6         GHz         R_LM         0.95         dB	b_min(2N_b)	-0.15		As/dfe2N_b	Sigma BBN step	5.00E-03	V					
f_z     42.5     GHz     sigma_RJ     0.01     UI       f_p1     42.5     GHz     A_DD     0.02     UI       f_p2     106.25     GHz     eta_0     4.00E-09     V^2/GHz       g_DC_HP     [-3:0.5:0]     [min:step:max]     SNR_TX     32.5     dB       R_LM     0.95     R_LM     0.95	g_DC	[-18:1:-8]	dB	[min:step:max]	Noise, jitter							
f_p1     42.5     GHz     A_DD     0.02     UI       f_p2     106.25     GHz     eta_0     4.00E-09     V^2/GHz       g_DC_HP     [-3:0.5:0]     [min:step:max]     SNR_TX     32.5     dB       f_HP_PZ     0.6     GHz     R_LM     0.95	f_z	42.5	GHz		sigma_RJ	0.01	UI					
f_p2         106.25         GHz         eta_0         4.00E-09         V^2/GHz           g_DC_HP         [-3:0.5:0]         [min:step:max]         SNR_TX         32.5         dB           f_HP_PZ         0.6         GHz         R_LM         0.95	f_p1	42.5	GHz		A_DD	0.02	UI					
g_DC_HP         [-3:0.5:0]         [min:step:max]         SNR_TX         32.5         dB           f_HP_PZ         0.6         GHz         R_LM         0.95	f_p2	106.25	GHz		eta_0	4.00E-09	V^2/GHz					
f_HP_PZ         0.6         GHz         R_LM         0.95	g_DC_HP	[-3:0.5:0]		[min:step:max]	SNR_TX	32.5	dB					
	f_HP_PZ	0.6	GHz		R_LM	0.95						

Floating Tap Control						
N_bg	3	0 1 2 or 3 groups				
N_bf	3	taps per group				
N_f	80	UI span for floating taps				
bmaxg	0.2	max DFE value for floating taps				
N_tail_start	24					
B_float_RSS_MAX	0.1					

# Backup

# All contributed channels at operating point (Color scale: IL D2D)

#### min(COM) per channel\_id

akinwale\_3df\_2209/100ohms/C2M\_PCB\_100ohms\_11dB\_202208016\_v2 akinwale\_3df\_2209/100ohms/C2M\_PCB\_100ohms\_14dB\_202208016\_v2 akinwale\_3df\_2209/100ohms/C2M\_PCB\_100ohms\_17dB\_202208016\_v2 akinwale\_3df\_2209/100ohms/C2M\_PCB\_100ohms\_20dB\_202208016\_v2 akinwale\_3df\_2209/100ohms/C2M\_PCB\_100ohms\_23dB\_202208016\_v2 akinwale\_3df\_2209/100ohms/C2M\_PCB\_100ohms\_26dB\_202208016\_v2 akinwale\_3df\_2209/85ohms/C2M\_PCB\_85ohms\_12dB\_202208016\_v2 akinwale\_3df\_2209/85ohms/C2M\_PCB\_85ohms\_15dB\_202208016\_v2 akinwale\_3df\_2209/85ohms/C2M\_PCB\_85ohms\_18dB\_202208016\_v2 akinwale\_3df\_2209/85ohms/C2M\_PCB\_85ohms\_21dB\_202208016\_v2 akinwale\_3df\_2209/85ohms/C2M\_PCB\_85ohms\_24dB\_202208016\_v2 akinwale\_3df\_2209/93ohms/C2M\_PCB\_93ohms\_10dB\_202208016\_v2 akinwale\_3df\_2209/93ohms/C2M\_PCB\_93ohms\_13dB\_202208016\_v2 akinwale\_3df\_2209/93ohms/C2M\_PCB\_93ohms\_16dB\_202208016\_v2 akinwale\_3df\_2209/93ohms/C2M\_PCB\_93ohms\_19dB\_202208016\_v2 akinwale\_3df\_2209/93ohms/C2M\_PCB\_93ohms\_22dB\_202208016\_v2 akinwale\_3df\_2209/93ohms/C2M\_PCB\_93ohms\_25dB\_202208016\_v2 mellitz\_3df\_02\_2207/TA\_6002\_6003\_tp0\_tp5 rabinovich\_3df\_01\_2209/rabinovich\_C2M\_200G\_Ortho\_93mil\_092122

channel\_id



Color by:

IL (die to die)

min(COM)

# All contributed channels at operating point (Color scale: ICN)

#### min(COM) per channel\_id

akinwale\_3df\_2209/100ohms/C2M\_PCB\_100ohms\_11dB\_202208016\_v2 akinwale\_3df\_2209/100ohms/C2M\_PCB\_100ohms\_14dB\_202208016\_v2 akinwale\_3df\_2209/100ohms/C2M\_PCB\_100ohms\_17dB\_202208016\_v2 akinwale\_3df\_2209/100ohms/C2M\_PCB\_100ohms\_20dB\_202208016\_v2 akinwale\_3df\_2209/100ohms/C2M\_PCB\_100ohms\_23dB\_202208016\_v2 akinwale\_3df\_2209/100ohms/C2M\_PCB\_100ohms\_26dB\_202208016\_v2 akinwale\_3df\_2209/85ohms/C2M\_PCB\_85ohms\_12dB\_202208016\_v2 akinwale\_3df\_2209/85ohms/C2M\_PCB\_85ohms\_15dB\_202208016\_v2 akinwale\_3df\_2209/85ohms/C2M\_PCB\_85ohms\_18dB\_202208016\_v2 akinwale\_3df\_2209/85ohms/C2M\_PCB\_85ohms\_21dB\_202208016\_v2 akinwale\_3df\_2209/85ohms/C2M\_PCB\_85ohms\_24dB\_202208016\_v2 akinwale\_3df\_2209/93ohms/C2M\_PCB\_93ohms\_10dB\_202208016\_v2 akinwale\_3df\_2209/93ohms/C2M\_PCB\_93ohms\_13dB\_202208016\_v2 akinwale\_3df\_2209/93ohms/C2M\_PCB\_93ohms\_16dB\_202208016\_v2 akinwale\_3df\_2209/93ohms/C2M\_PCB\_93ohms\_19dB\_202208016\_v2 akinwale\_3df\_2209/93ohms/C2M\_PCB\_93ohms\_22dB\_202208016\_v2 akinwale\_3df\_2209/93ohms/C2M\_PCB\_93ohms\_25dB\_202208016\_v2 mellitz\_3df\_02\_2207/TA\_6002\_6003\_tp0\_tp5

rabinovich\_3df\_01\_2209/rabinovich\_C2M\_200G\_Ortho\_93mil\_092122



channel\_id

# Tx FFE coefficients



# COM/IL scatter plot



# COM/ICN scatter plot

