Adding Sequence Ordered Set to MII

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March 11, 2024

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MII vs. XGMII

- XGMII and MII are similar in transporting data, errors, idles, and low power idles
  - MII – Less than 1G
  - XGMII – More than 1G
  - GMII – 1G (Not discussed in this presentation)
- Half duplex features in MII not present in XGMII
- XGMII has useful features to send ordered sets
  - Local Fault
  - Remote Fault
  - Link Interruption
  - Open way to add new ordered sets while keeping the transport backwards compatible.

Tx MII vs XGMII

Table 22–1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Reserved
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON request
0	1	0011	PLCA COMMIT request
0	1	0100 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

Table 46–3—Permissible encodings of TXC and TXD

TXC	TXD	Description	PLS_DATA.request parameter
0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	00 through 05	Reserved	—
1	06	Only valid on all four lanes simultaneously to request LPI	No applicable parameter (normal interframe)
1	07	Idle	No applicable parameter (Normal inter-frame)
1	08 through 9B	Reserved	—
1	9C	Sequence (only valid in lane 0)	No applicable parameter (Inter-frame status signal)
1	9D through FA	Reserved	—
1	FB	Start (only valid in lane 0)	No applicable parameter, replaces first eight ZERO, ONE of a frame (preamble octet)
1	FC	Reserved	—
1	FD	Terminate	DATA_COMPLETE
1	FE	Transmit error propagation	No applicable parameter
1	FF	Reserved	—

NOTE—Values in TXD column are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>).

- MII is missing ability to send Sequence Ordered Sets

Rx MII vs XGMII

Table 22–2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON indication
0	1	0011	PLCA COMMIT indication
0	1	0100 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

Table 46–4—Permissible lane encodings of RXD and RXC

RXC	RXD	Description	PLS_DATA.indication parameter
0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1	00 through 05	Reserved	—
1	06	Only valid on all four lanes simultaneously to indicate LP_IDLE is asserted	No applicable parameter (Normal interframe)
1	07	Idle	No applicable parameter (Normal inter-frame)
1	08 through 9B	Reserved	—
1	9C	Sequence (only valid in lane 0)	No applicable parameter (Inter-frame status signal)
1	9D through FA	Reserved	—
1	FB	Start (only valid in lane 0)	No applicable parameter, first eight ZERO, ONE of a frame (a preamble octet)
1	FC	Reserved	—
1	FD	Terminate	No applicable parameter (Start of inter-frame)
1	FE	Receive error	No applicable parameter
1	FF	Reserved	—
NOTE—Values in RXD column are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>).			

MII Sequence Ordered Set Coding Proposal

TX_EN/ RX_DV	TX_ER/ RX_ER	TXD<3:0>/ RXD<3:0>	
0	1	0100	Sequence Ordered Set 1st Half
0	1	0100	Sequence Ordered Set 2nd Half
0	0	Lane1<3:0>	Ordered Set Value Lane 1 LSB
0	0	Lane1<7:4>	Ordered Set Value Lane 1 MSB
0	0	Lane2<3:0>	Ordered Set Value Lane 2 LSB
0	0	Lane2<7:4>	Ordered Set Value Lane 2 MSB
0	0	Lane3<3:0>	Ordered Set Value Lane 3 LSB
0	0	Lane3<7:4>	Ordered Set Value Lane 3 MSB

XGMII

Table 46–5—Sequence ordered sets

Lane 0	Lane 1	Lane 2	Lane 3	Description
Sequence	0x00	0x00	0x00	Reserved
Sequence	0x00	0x00	0x01	Local Fault
Sequence	0x00	0x00	0x02	Remote Fault
Sequence	0x00	0x00	0x03	Link Interruption
Sequence	≥ 0x00	≥ 0x00	≥ 0x04	Reserved

NOTE—Values in Lane 1, Lane 2, and Lane 3 columns are in hexadecimal, most significant bit to least significant bit (i.e., <7:0>). The link fault signaling state diagram allows future standardization of reserved Sequence ordered sets for functions other than link fault indications

- If two ordered set codes seen in a row, the next 6 nibbles are the 24-bit ordered set value
- Legacy MACs – RX_DV = 0, RX_ER = 1, RXD = 0100 currently reserved
  - Does legacy MACs treat this as idles?
- The 6 nibbles recognized by legacy MACs as idles

Connecting to Legacy MACs

- Option 1:
  - Standard stays silent. Proprietary method to convert Sequence Order Set symbol to idles in implementations
- Option 2:
  - Specify IEEE define register to give applications hint
    - OS_ABILITY – Read only register indicating PHY can handle ordered set
    - OS_ENABLE –

      1 = PHY passes ordered set through on RX_DV/RX_ER/RXD,
      0 = PHY converts ordered set to idles

THANK YOU