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IEEE P802.3dg 100BASE-T1L PHY Time Domain Simulations PAM-3 and PAM-4

Brian Murray
Philip Curran
Michal Brychta

Introduction

- The presentation compares time domain results of a generic 100BASE-T1L PHY architecture for PAM-3 and PAM-4
  - Example 100BASE-T1L results under the same conditions for PAM-3 and for PAM-4
- The presentation outlines the test bench (channel, noise model) used to evaluate time domain simulation results
  - Using the Insertion Loss model from the adopted Link Segment (as of 9/7/23)
  - Scaled the noise model from 802.3cg to 100 MHz
- Real cable model data and noise models are required
  - It would greatly help to have S-parameter data for real cables of existing installed base and proposed 100BASE-T1L cables so that these could be used in the time domain simulations
  - It would greatly help to have real interference noise models, e.g. equivalent to EFT
- Results show that both PAM-3 and PAM-4 can support 100BASE-T1L
  - But that PAM-4 has a disadvantage in terms of SNR performance at 500m
  - And that PAM-4 has a disadvantage in terms of latency

Recap – of where we have come from

- 10BASE-T1L was a relatively easy problem to solve
  - Low speed, so operates at a low symbol rate
    - Low symbol rate results in lower Insertion Loss
    - Hence, have lots of SNR margin at 1000 m and in practice operates up to 2000 m depending on the level of noise
- Symbol rate for 10BASE-T1L is 7.5 MSym/s
  - Nyquist at 3.75 MHz, typically use < 10 MHz of bandwidth
  - Low bandwidth so can filter out noise and interference which greatly helps with EFT
  - Low bandwidth helps with Alien Crosstalk
- Latency for 10BASE-T1L is low
  - About 5 μs for Tx and Rx including implementation delays
  - This is 60 symbols or 50 bits times – translates **towards 500 ns** at 100BASE-T1L
    - 100BASE-TX (MII) is 300 ns; 37 symbols or 30 bits times
    - 1000BASE-T (RGMII) is 290 ns; 36 symbols or 290 bits times

Progress so far in 802.3dg

- Early analysis shows that PAM-3, PAM-4, PAM-5 are all options
- But that reaching 500 m was going to be much more challenging
  - In particular, with the Insertion Loss of the existing cables and increased cross talk due to higher bandwidth
- The converse of '*Low symbol rate results in lower Insertion Loss*' is that Insertion Loss is much higher for 100BASE-T1L
  - The improvement from the 802.3dg adopted Link Segment is very important and beneficial
  - We still should consider the case of using 802.3cg cable models that will represent some of the installed base of cables, but expect 500 m to be challenging for these cables
- The converse of '*Low bandwidth helps with Alien Crosstalk*' is that cross talk will be much worse for 100BASE-T1L
  - Proposed improvements to mitigate cross talk are also very important and beneficial

Latency and DC Balance

- Two topics that have not received much attention prior to this meeting are latency and DC balance
  - Latency has been clearly called out as a requirement for the motor encoder application
    - Other applications can tolerate higher latency but it's not unbounded
  - Intrinsic Safety is part of our objectives, and the importance of DC balance was discussed in the July meeting
    - *'Do not preclude working within an Intrinsically Safe device and system as defined in IEC 60079'*
- Ethernet Control Codes are required for framing and this can impact Latency
  - Typically, lower speed Ethernet PHYs put the control codes in the constellation
    - E.g. in 10BASE-T1L we reserved a 3T code group [0, 0,0] as a Comma Code; similar approach in 1000BASE-T
    - An 8B10B low latency block code is sometimes used (100BASE-TX), but is a 25% overhead in symbol rate
  - Typically, higher speed PHYs (10G) use a block code like 64B/65B or 80B/81B to embed control codes
    - At the higher speeds of 10G and above the latency of these very efficient block codes is a small portion of the overall latency
    - But as pointed out in Lo_3dg_01_011024.pdf that is not the case at 100 Mb/s
    - A 64B/65B block code add adds 640 + 220 = 860 ns to the latency

DC Balance: Complexity of SPoE verses PoE [from July 2023]

- In PoE where we have 2-pairs, power is applied at the center tap of the transformers
  - Positive to one transformer pair and negative to the 2nd transformer
  - Hence, half of the current flows in each of the wires in the pair, travelling in the same direction on both wires
    - So down from the center tap on one half of the winding and up on the other half of the winding
  - Hence the flux cancels and thus the cost of an inductor the required OCL is reasonable
- In SPoE we only have a single pair and the current has to travel in opposite directions on each wire
  - So the current travels in the same direction in both halves of the winding
  - And the magnetic flux adds and the result is that the cost and size of an inductor with the same OCL as PoE is much higher
    - This is so that we avoid saturation in the inductor
    - For reference previous IEEE presentations have discussed the trade-off of inductor size and OCL in more detail, see for example Stewart_3dd_01_09072021.pdf and paul_01_da_120220.pdf

DC Balance: Impact of Droop on the Inductor Size for SPoE [from July 2023]

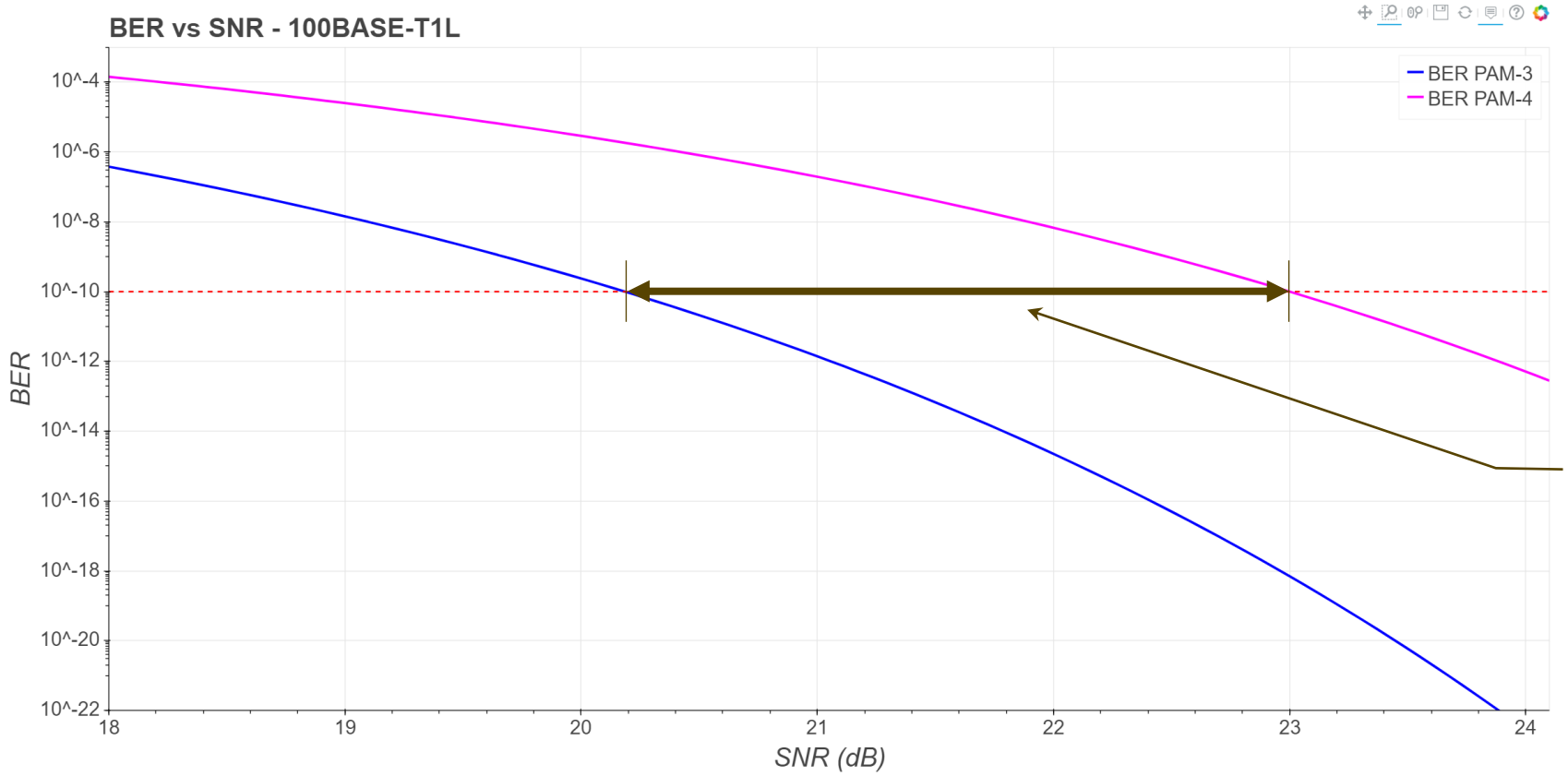
- In any baseband signaling, even using scramblers and encoding there are sequences of symbols of the same sign
  - DC content cannot get through the transformer or capacitor coupling, resulting in droop or Base Line Wander (BLW)
  - Ideally in any given window we minimize the length of these runs
  - Even a well design scrambler has low probability events with specific sequences
- The PHY transmitter and Receiver must allow for extra signal range to account for BLW
  - In some BASE-T PHYs these effects can double the required signal range
  - On the PHY receiver side this cost is in lost SNR – which is even more important than gates or bits because you can't get it back
- The lower the inductance (OCL) the greater this effect for a given sequence length
- Controlling the running disparity is a method to limit the length of the sequence of symbols of the same sign, reducing BLW
- **Running disparity allows us to use lower OCL inductors in SPoE** results in lower cost and smaller size inductors!
- Key is to **include consideration of SPoE up front in the definition of the PHY line code**

Higher Versus Lower Levels of PAM Coding

- Lower levels of PAM coding, e.g. PAM-2 & PAM-3 have the widest spacing between thresholds and better immunity to noise
  - Especially non-Gaussian noise and interference like Electrical Fast Transients (EFT) common in Industrial Noise Environments
  - They have the disadvantage of lower bits / symbol so require a higher symbol rate
  - They are less susceptible to droop and support lower OCL SPoE inductors
- Higher levels of PAM coding, e.g. PAM-4 & PAM-5 have less spacing between thresholds and worse noise immunity
  - They have higher bits / symbol and can operate at a lower symbol rate which can sometimes be a trade-off against the noise performance
  - But are affected more by droop, resulting in a loss of SNR
  - Usually, we include coding gain to recover some of the loss in noise performance
- For very high speeds with more limited channel bandwidth you have to go to higher levels of PAM coding to achieve the bit rate
  - Generally, it is better to use the lowest possible PAM order than can achieve the reach and speed to maintain the best noise performance and lower complexity
    - Especially for real world Industrial Ethernet noise like EFT
  - For example, 10G – 25Gb/s Serdes still use 2-level PAM on fiber as the bandwidth is there
  - In BASE-T moved to PAM-5 to get 1G speeds and PAM-16 to get 10G speeds; but 100BASE-TX is 3-level, 100BASE-T1 and 1000BASE-T1 are also PAM-3

SNR verses BER or Packet Error Rate

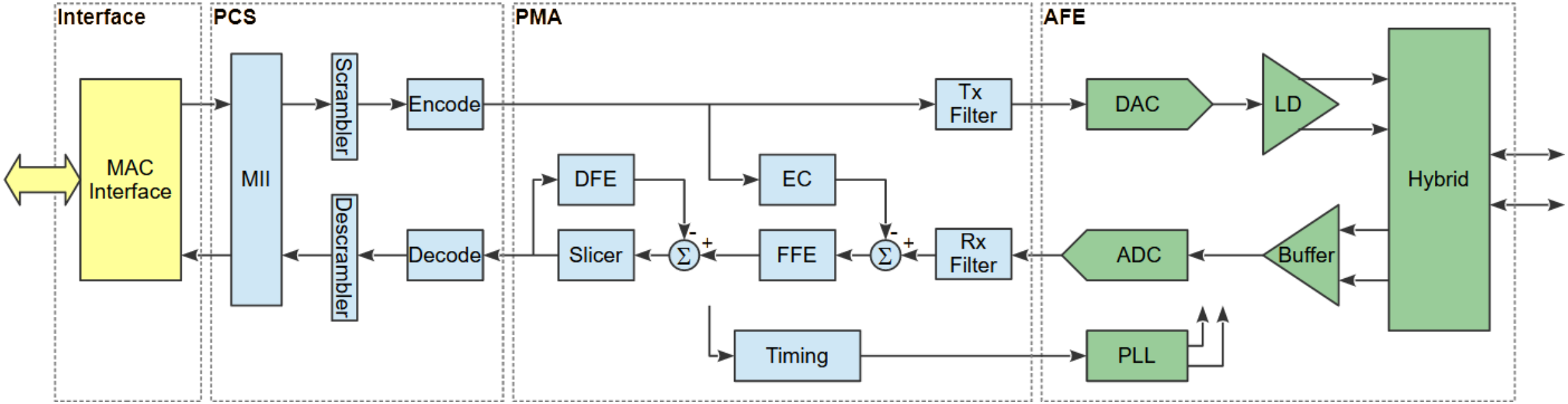
- 802.3dg standard mandates a BER ≤ 10^{-10}
  - PAM-3 4B3T coding has a symbol power of 0.64422 and requires an SNR of 20.2 dB for a BER ≤ 10^{-10}
  - PAM-4 4B2T coding has a symbol power of 0.55555 and requires an SNR of 23.0 dB for a BER ≤ 10^{-10}
    - Worse by $10\log_{10}(2/3) = 3.5$ dB due to the ratio of thresholds and helped by lower symbol power – 2.8 dB delta



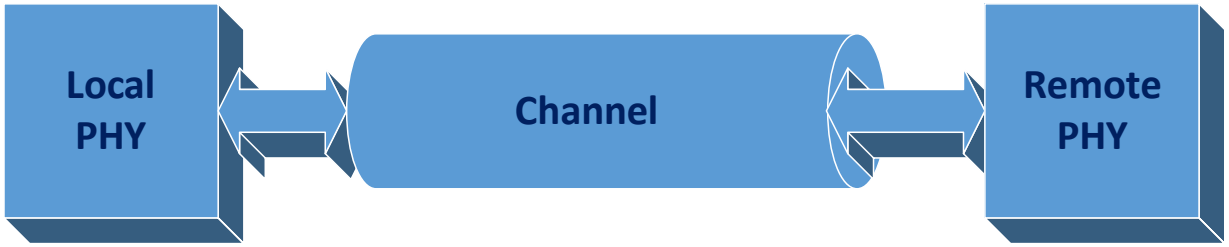
- 2.8 dB difference between PAM-3 and PAM-4
- So need to get 2.8 dB elsewhere to stay still

Generic 100BASE-T1L PHY Architecture

- Generic block diagram of a BASE-T PHY architecture



- A time domain simulation is run for a range of cable lengths / noise to determine SNR margin verses reach



Other example PHY architecture diagrams
10BASE-T1L .cg Jan 2017 Graber_10SPE_10_0117.pdf

100BASE-T1L Time Domain Simulation

- Compare 100BASE-T1L PAM-3 and PAM-4 under the same conditions
- Generic 100BASE-T1L Architecture with following parameters
  - PAM-3 using 802.3cg Scrambler and 802.3cg 4B3T PCS at 75 MSym/s
  - PAM-4 using 802.3cg Scrambler and 4B2T PCS at 62.5 MSym/s
  - Ideal DAC & line driver, 2.4V Tx, 12-bit ADC
  - DFE using 48 feed forward taps and 64 feedback taps, ideal data path
- 802.3cg and 802.3dg Insertion Loss model

802.3dg IL	$IL(f) \leq \left(5.42 \times \sqrt{f} + 0.044 \times f + \frac{1.76}{\sqrt{f}}\right) + 5 \times 0.02 \times \sqrt{f} \quad (\text{dB})$
802.3cg IL	$IL(f) \leq 10\left(1.23 \times \sqrt{f} + 0.01 \times f + \frac{0.2}{\sqrt{f}}\right) + 10 \times 0.02 \times \sqrt{f} \quad (\text{dB})$

- 802.3cg External Noise Model extended to 100 MHz
  - Noise with a Gaussian distribution and magnitude of **–116 dBm/Hz**
  - 5mV rms over a flat 100 MHz

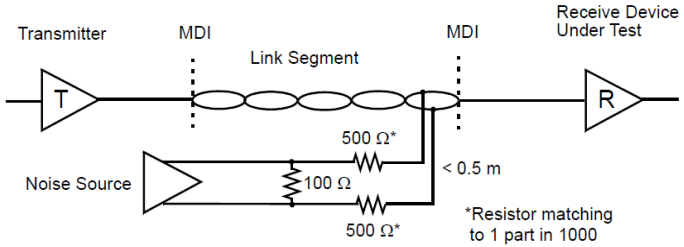
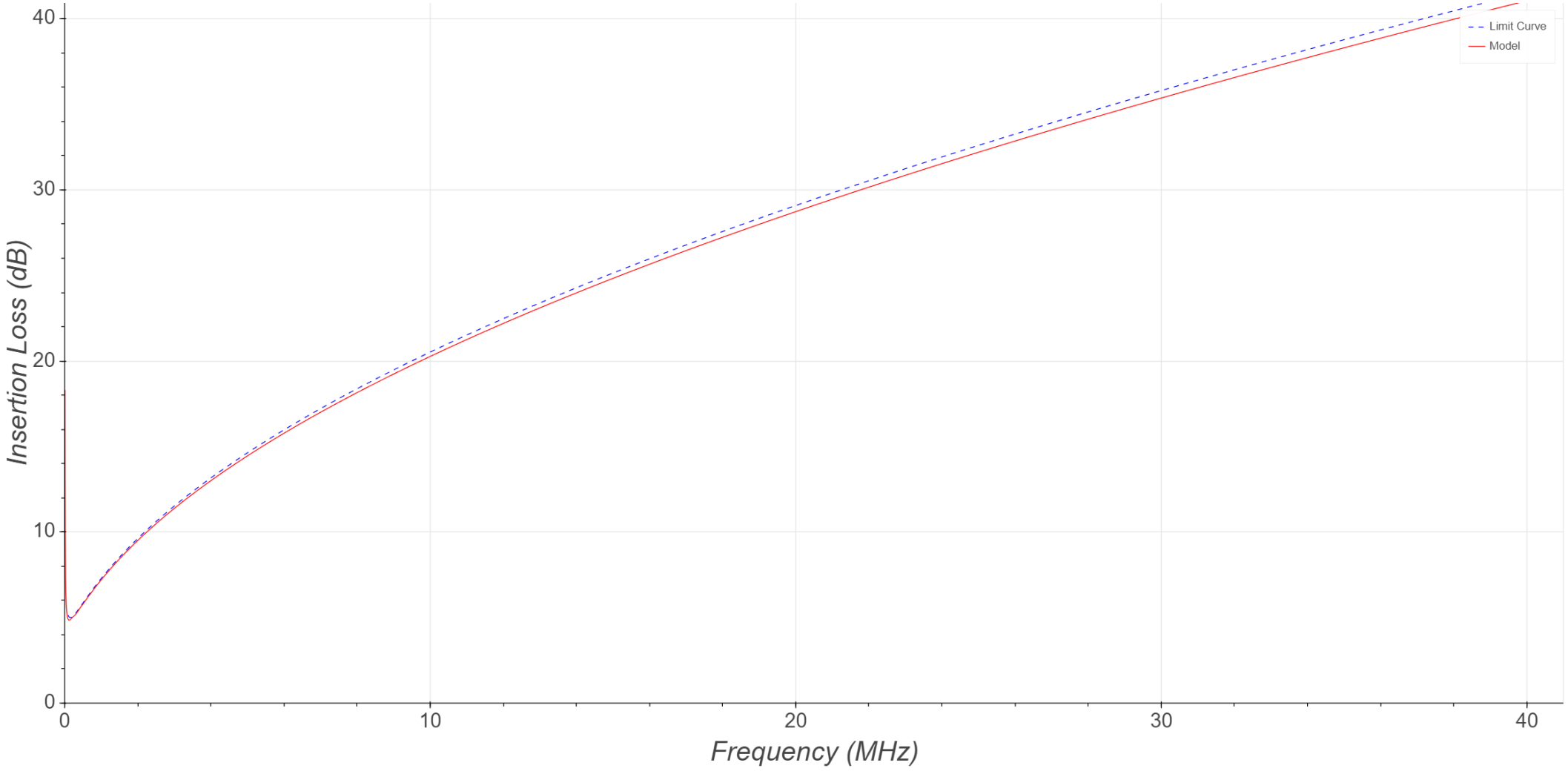
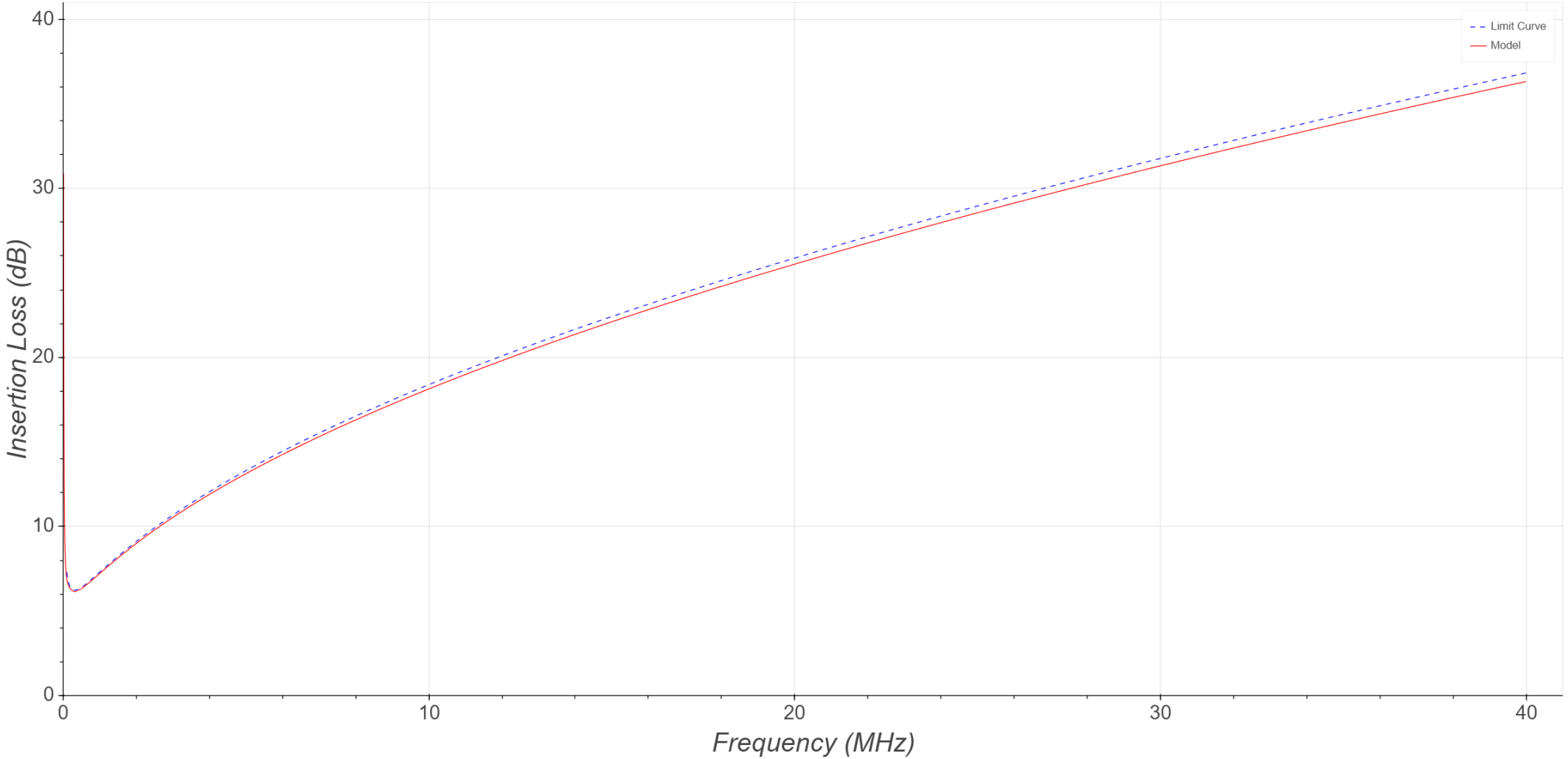


Figure 146–24—Alien crosstalk noise rejection test set-up

Insertion Loss 500m – 802.3cg Extended to 40 MHz

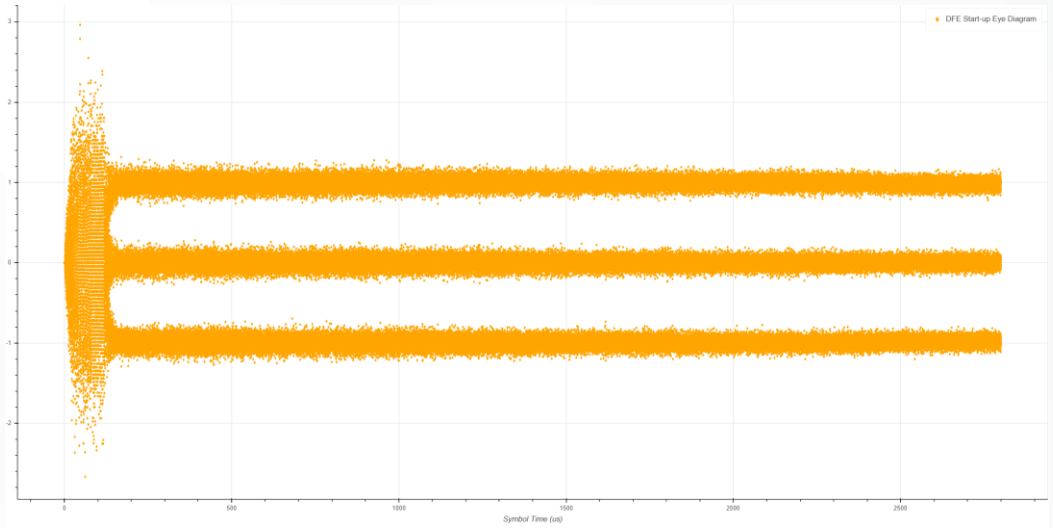


Insertion Loss 500m – 802.3dg Extended to 40 MHz

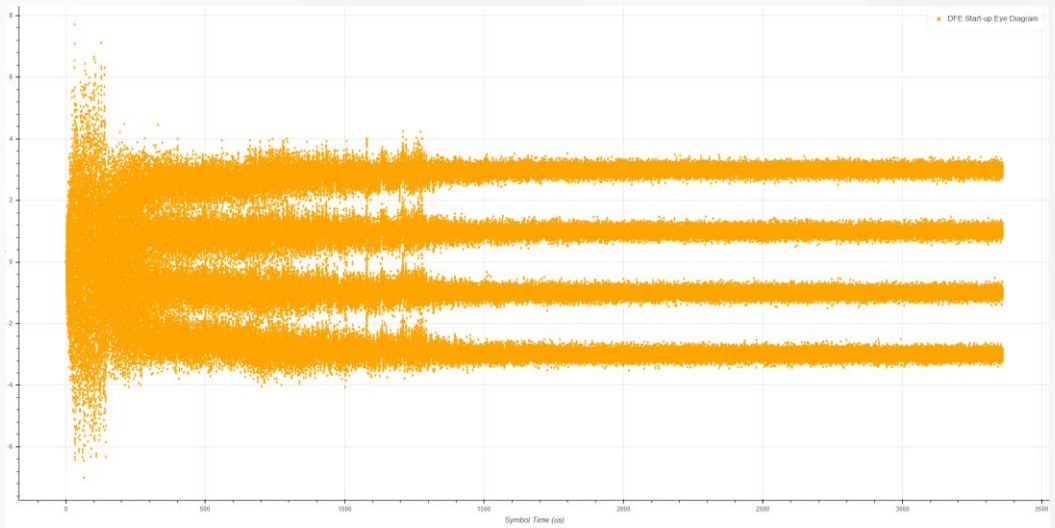


100BASE-T1L PAM-3 & PAM-4 802.3dg IL, 2.4V Tx, 500m & 3 mV Noise

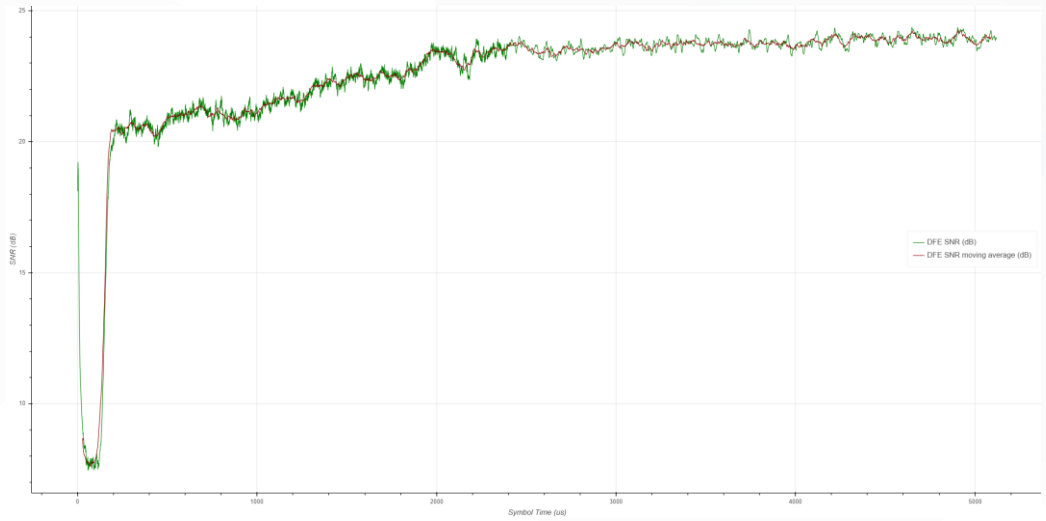
PAM-3: Start-up Data Pattern



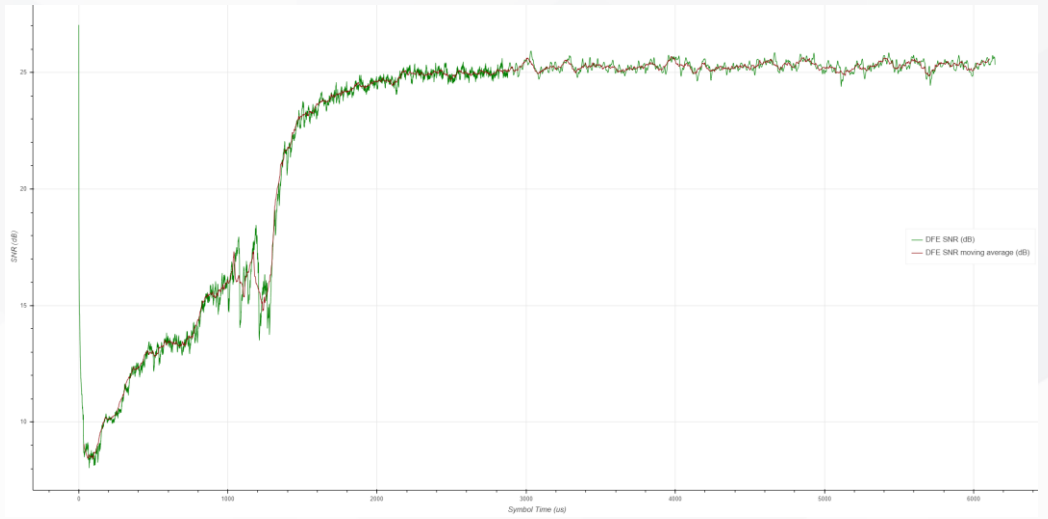
PAM-4: Start-up Data Pattern



PAM-3: SNR Convergence 0 – 5 ms

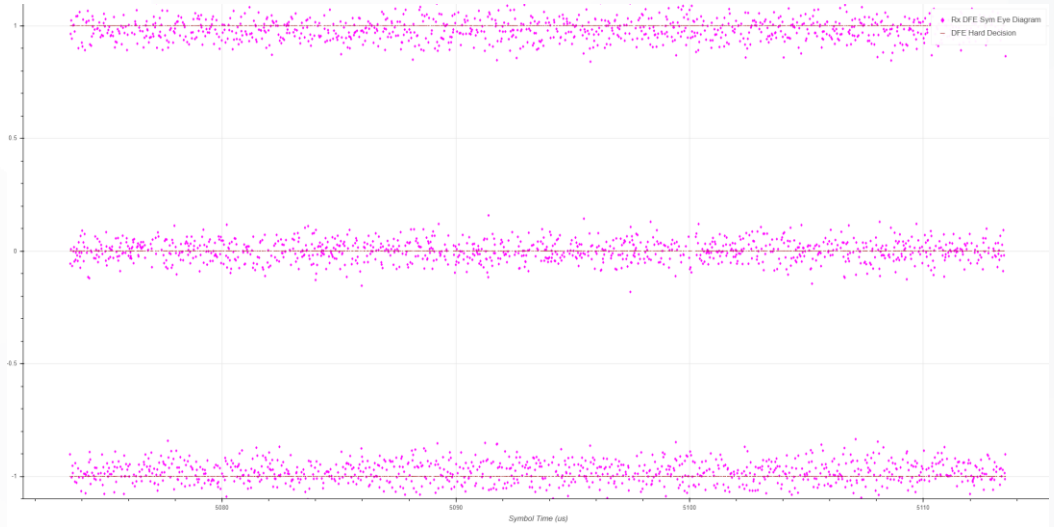


PAM-4: SNR Convergence 0 – 5 ms

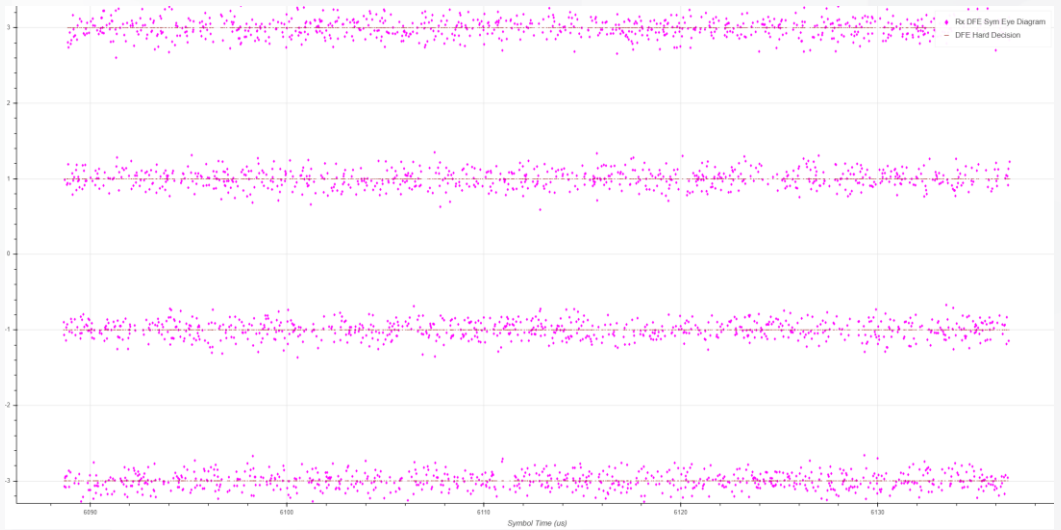


100BASE-T1L PAM-3 & PAM-4 802.3dg IL, 2.4V Tx, 500m & 3 mV Noise

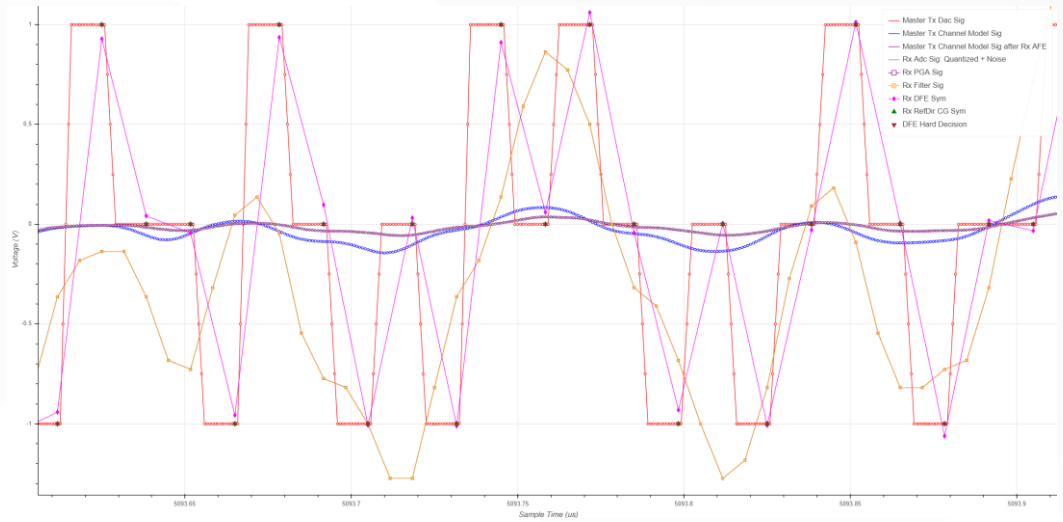
PAM-3: Data Pattern During Data



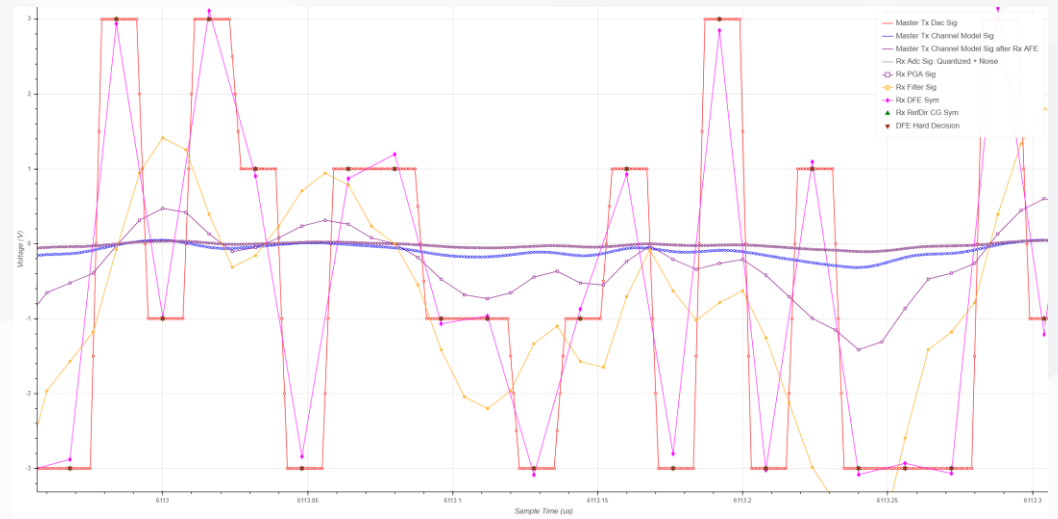
PAM-4: Data Pattern During Data



PAM-3: Time Domain Waveforms during Data



PAM-4: Time Domain Waveforms during Data

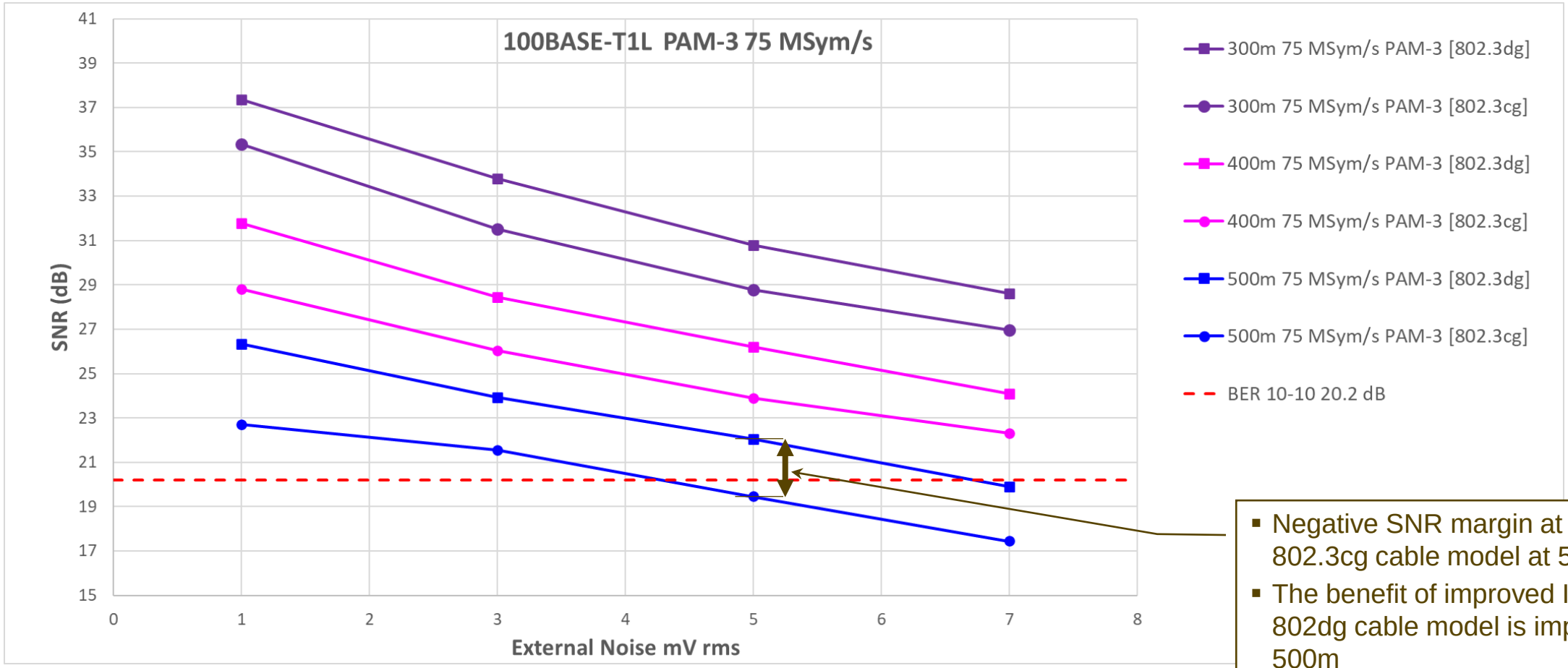


100BASE-T1L SNR vs Ext Noise

- Plot SNR versus external Gaussian noise
  - For values of 1, 3, 5, 7 mV
  - For cable lengths 300, 400, 500 m
  - For Insertion Loss cable model proposed for 802.3dg and IL model used in 802.3cg
  - At 2.4V transmit level
  - After 384K symbols of start-up (~ 5000 μs)
- Compare 100BASE-T1L using PAM-3 and PAM-4
  - 75 MSym/s PAM-3
  - 62.5 MSym/s PAM-4
  - 50 MSym/s PAM-4

100BASE-T1L SNR vs Ext Noise – 75 MSym/s PAM-3

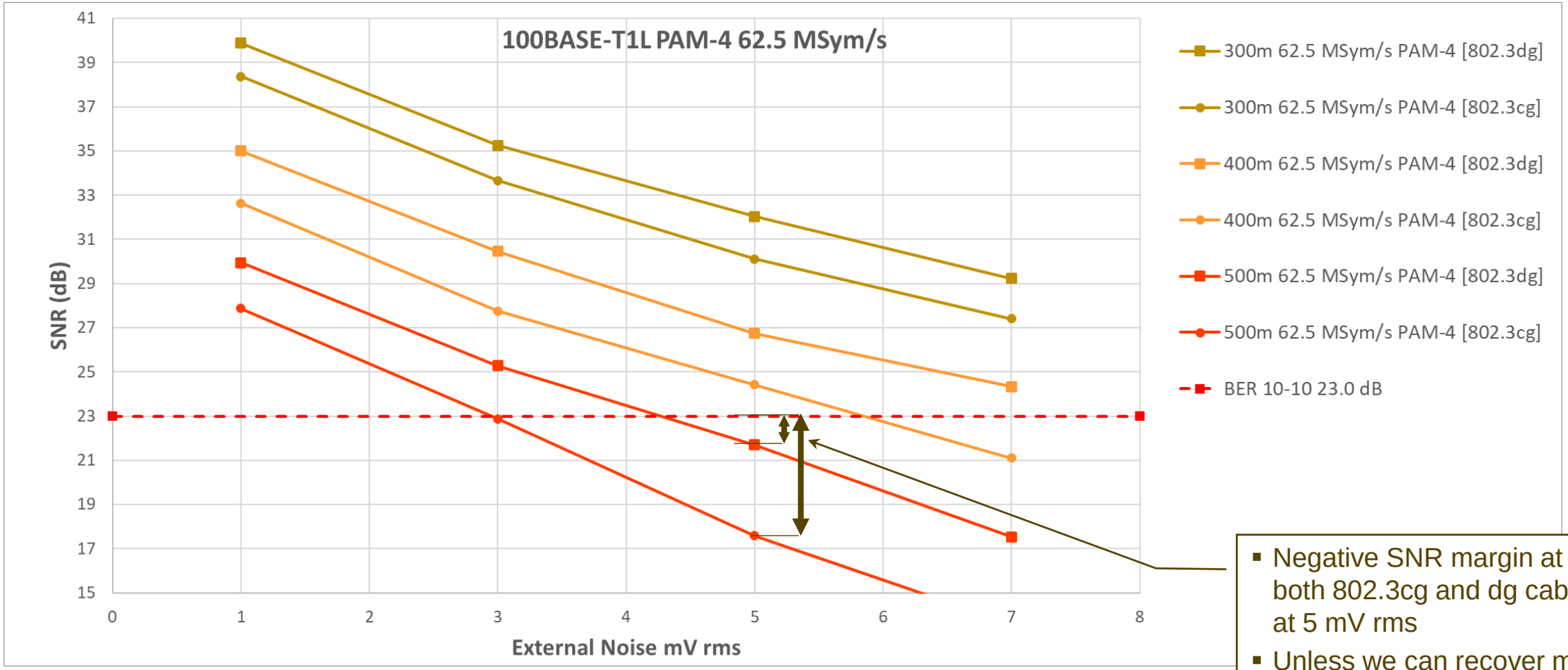
100BASE-T1L 75 MSym/s PAM-3: SNR versus External Noise – 2.4V Tx Amplitude



- Negative SNR margin at 500m and 802.3cg cable model at 5 mV rms
- The benefit of improved IL with 802dg cable model is important at 500m

100BASE-T1L SNR vs Ext Noise – 62.5 MSym/s PAM-4

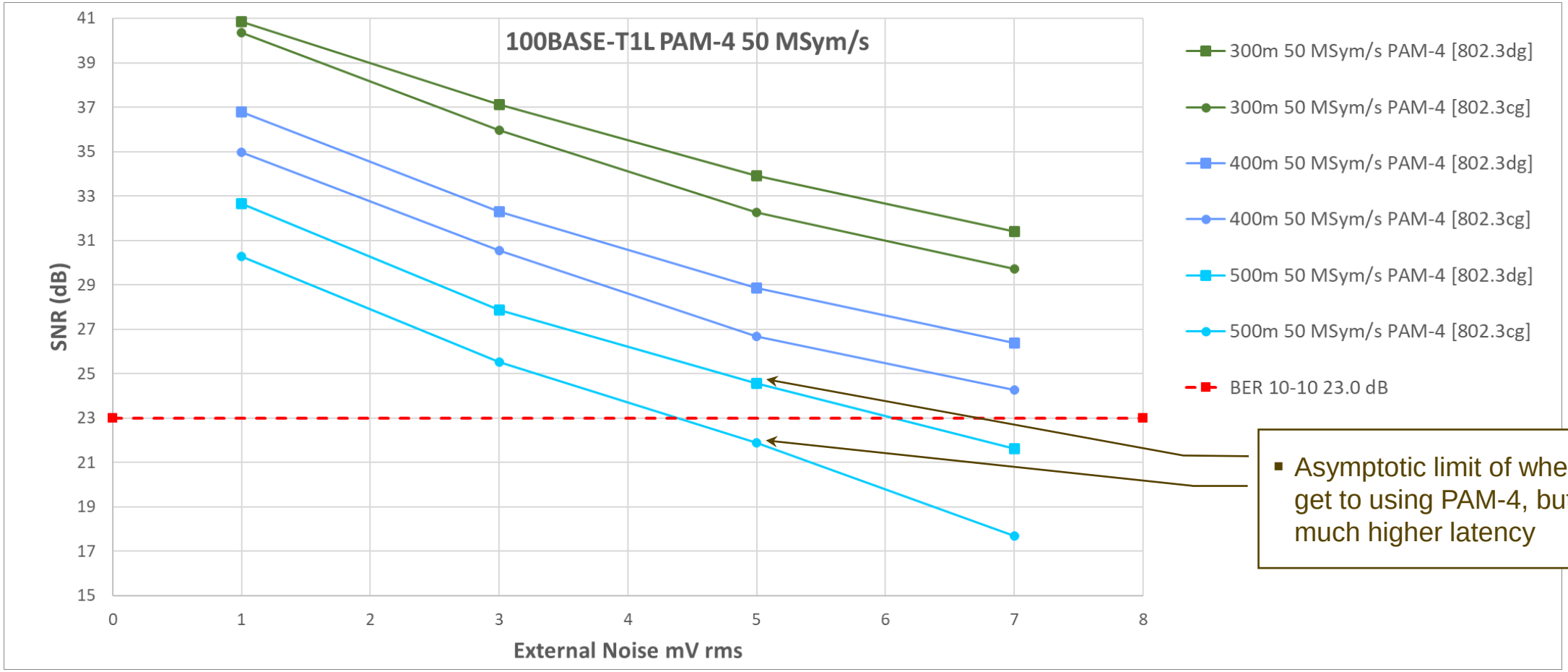
100BASE-T1L 62.5 MSym/s PAM-4: SNR versus External Noise – 2.4V Tx Amplitude



- Negative SNR margin at 500m for both 802.3cg and dg cable models at 5 mV rms
- Unless we can recover margin with coding gain we have pushed too far

100BASE-T1L SNR vs Ext Noise – 50 MSym/s PAM-4

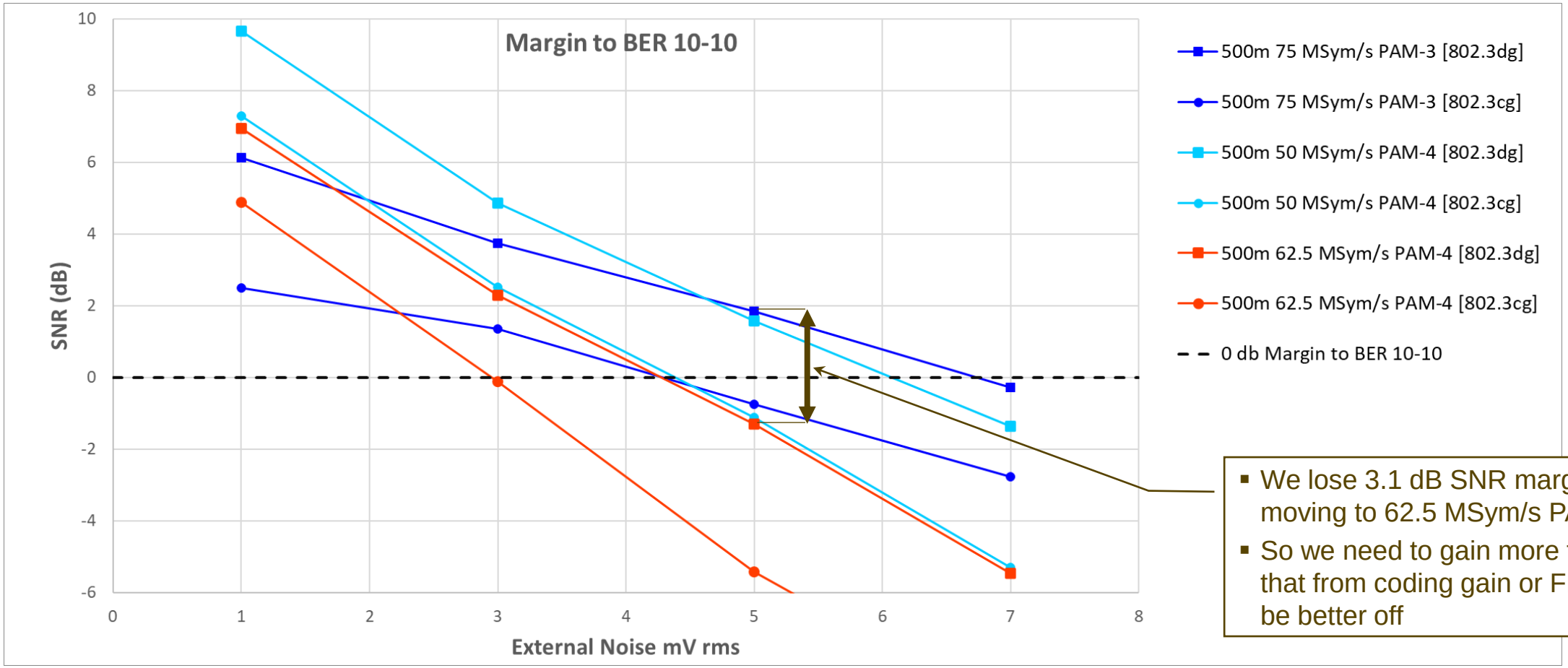
100BASE-T1L 50 MSym/s PAM-4: MSE versus External Noise – 2.4V Tx Amplitude



- Asymptotic limit of where we can get to using PAM-4, but at cost of much higher latency

SNR Margin to 10^{-10} for 100BASE-T1L PAM-3 and PAM-4

100BASE-T1L 75 MSym/s PAM-3, 62.5 MSym/s PAM-4 & 50 MSym/s PAM-4



- We lose 3.1 dB SNR margin moving to 62.5 MSym/s PAM-4
- So we need to gain more than that from coding gain or FEC to be better off

Comparison of 100BASE-T1L PAM-3 and PAM-4

- No advantage moving to PAM-4 and it is worse for SNR margin at 500m
  - Obviously is better at much lower noise levels
- PAM-4 will be worse for impulsive noise interference like EFT
- RS-Coding or other FEC can be used in addition to PAM-4 to mitigate the bit errors induced by EFT or other interference sources
  - But can also use RS-coding or FEC with PAM-3
  - Need analysis of EFT like noise to determine if RS coding is required and what it can achieve
- We can use a more efficient block code like 64B/65B but at the cost of much higher latency
  - Even at 50 MSym/s (the asymptotic limit) PAM-4 has worse SNR margin to 10^{-10} BER
- Have not considered PAM-5 as this would have to operate at 50 MSym/s and would require an even higher SNR margin for 10^{-10} BER

Key PHY Questions and Work Still to be Done

- Do we need to include RS coding / FEC ?
  - Is it necessary to use RS Coding /FEC to meet the BER requirements at 100m with low latency and /or 500m with higher latency
  - And how do we add RS coding / FEC so that we gain more than we lose
- We need use real cable model data and impulsive noise models to help answer these questions
  - Need an interference noise model, e.g. equivalent to EFT
  - We have some initial measured data from a standard EFT test and plan to present some results on this soon
    - We should be able to generate a simple model of the interference from this data
- We can continue to use the IL curves to generate cable models
  - But it would be much better to have S-parameter data for real cables of existing installed base and proposed 100BASE-T1L cables so that these could be used in the time domain simulations

Summary

- PAM-3 coding meets the reach requirements of 500 m on the proposed link segment specifications with some SNR margin
- PAM-3 coding schemes can be implemented with low latency by adopting similar approaches to other low speed PHYs like 10BASE-T1L and embed the control codes in the constellation
- PAM-3 has the advantage of wider spacing of decision thresholds which gives the greatest immunity to impulsive noise
- RS Coding / FEC can be added to PAM-3 or PAM-4 modulation
- Consideration and analysis of characteristics, amplitude and burst duration, of the impulsive noise found in Industrial Environments will tell us if there is any benefit to using higher order PAM modulation and / or RS coding / FEC

Questions ?