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IEEE P802.3dg 100BASE-T1L PHY Time Domain Simulations PAM-3 and PAM-4

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Introduction

- The presentation compares time domain results of a generic 100BASE-T1L PHY architecture for PAM-3 and PAM-4
  - Example 100BASE-T1L results under the same conditions for PAM-3 and for PAM-4 with running disparity
  - Under the same conditions of cross-talk modelled with AWGN
- Proposed AWGN Noise models for PHY Evaluation *have been presented to the group*
  - *zimmerman_3dgah_01b_01292024.pdf*
  - This approximates to a flat AWGN Noise source at -113 dBm/Hz over 0 to 100 MHz for a 75 MSym/s baud rate which is 7 mV rms
- Example PAM-4 modulation schemes that support running disparity have been presented to the group
  - Lo_3dg_01_012524.pdf and Tingting_3dg_25_01_2024.pdf
  - Nominally PAM-4 operates at 2.0 bits/symbol (without running disparity) resulting in 50 MSym/s for 100Mb/s
  - Adding running disparity to a PAM-4 modulation scheme using 5B/3Q and 7B/4Q (or 9B5Q) line codes results in symbol rates of 55.55 to 60 MSym/s

PAM-3 and PAM-4 with Running Disparity

- 10BASE-T1L used a 4B3T coding to support running disparity at 1.33 bits/symbol
  - The theoretical limit of PAM-3 is 1.58 bits/symbol (without running disparity) which corresponds to 63 MSym/s at 100Mb/s
  - Alternative PAM-3 modulation schemes support running disparity at bits/symbol rates closer to the theoretical limit
    - Examples are 7B5T, 13B9T and 15B10T at 1.4, 1.44 and 1.5 bits/symbol resulting in symbol rates of 66.66 to 71.42 MSym/s
- Both PAM-3 and PAM-4 can trade symbol rate for coding gain and use higher symbol rates
  - A valid comparison is **PAM-3 at 66.66 – 75 MSym/s** versus **PAM-4 at 55.55 – 62.5 MSym/s**
  - A well design coding scheme should recover more in SNR / bit error rate performance than is lost by operating at the higher symbol rate

100BASE-T1L Time Domain Simulation

- Compare 100BASE-T1L PAM-3 and PAM-4 under the same conditions
- Generic 100BASE-T1L Architecture with following parameters
  - PAM-3 using 802.3cg Scrambler and 802.3cg 4B3T PCS with running disparity at 66 - 75 MSym/s
  - PAM-4 using 802.3cg Scrambler and 5B3Q PCS with running disparity at 50 - 62.5 MSym/s
  - Ideal DAC & line driver, 2.4V Tx, 12-bit ADC
  - DFE using 48 feed forward taps and 64 feedback taps, ideal data path
- 802.3cg and 802.3dg Insertion Loss model

802.3dg IL	$IL(f) \le \left(5.42 \times \sqrt{f} + 0.044 \times f + \frac{1.76}{\sqrt{f}}\right) + 5 \times 0.02 \times \sqrt{f} \quad \text{(dB)}$
802.3cg IL	$IL(f) \le 10\left(1.23 \times \sqrt{f} + 0.01 \times f + \frac{0.2}{\sqrt{f}}\right) + 10 \times 0.02 \times \sqrt{f} \quad \text{(dB)}$

- External Noise Model proposed in
  - Noise with a Gaussian distribution and magnitude of **–113 dBm/Hz**
  - 7 mV rms over a flat 100 MHz

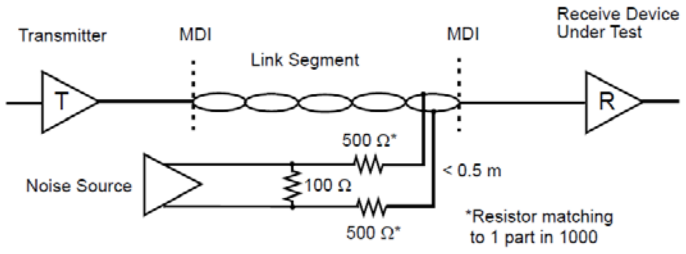

Figure 146–24—Alien crosstalk noise rejection test set-up

100BASE-T1L SNR vs Ext Noise

- Plot SNR versus external Gaussian noise
  - For values of 3, 5, 7 and 9 mV rms
  - For cable lengths 300, 400, 500 m
  - For Insertion Loss cable model proposed for 802.3dg and IL model used in 802.3cg
  - At 2.4V transmit level
  - After 384K symbols of start-up, idle and data (~ 5000 μs)
- Compare 100BASE-T1L using PAM-3 and PAM-4 with running disparity
  - 66.66 and 75 MSym/s PAM-3
  - 50 and 62.5 MSym/s PAM-4

100BASE-T1L SNR vs Ext Noise – PAM-3 dg IL Model

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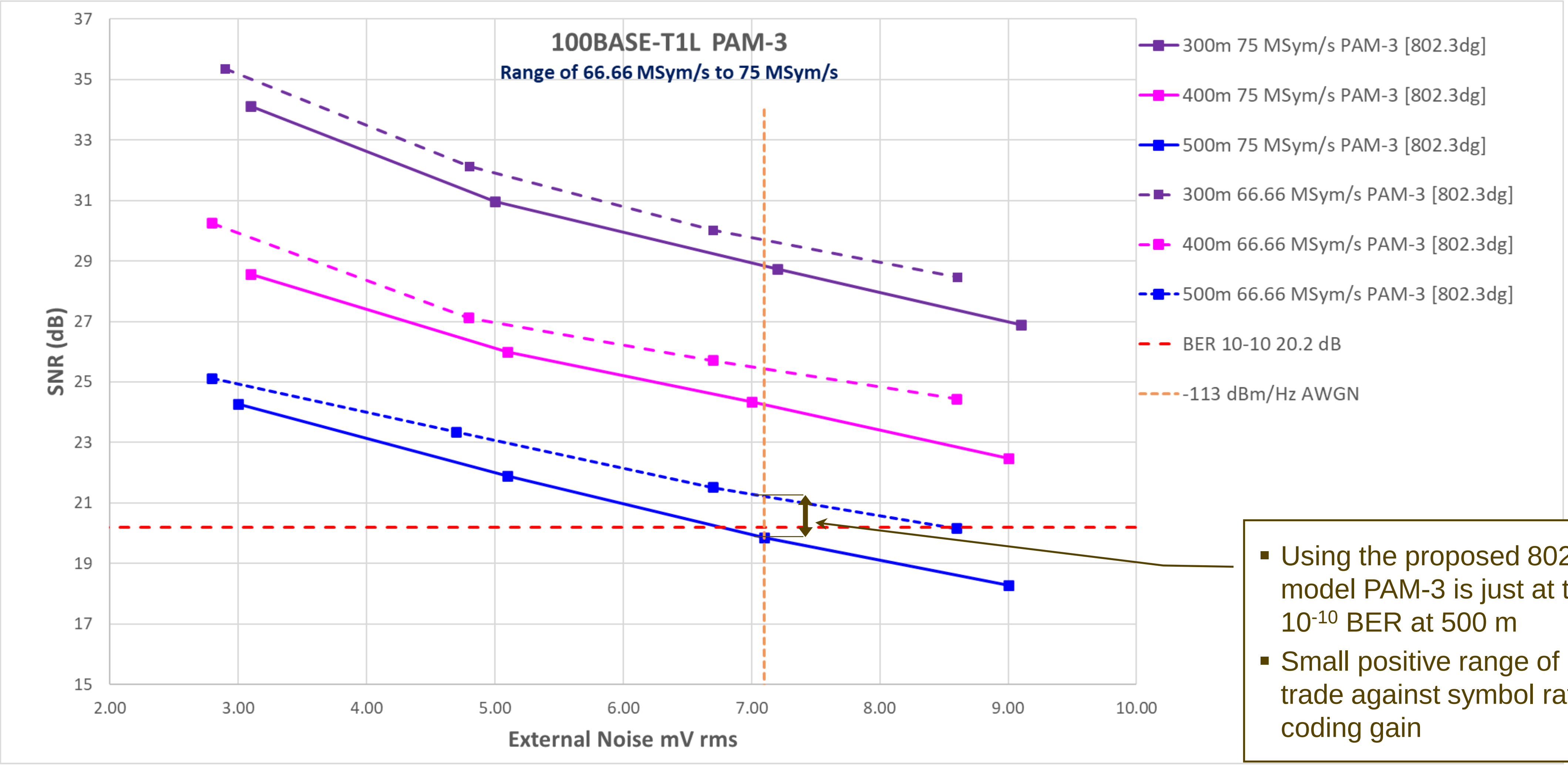
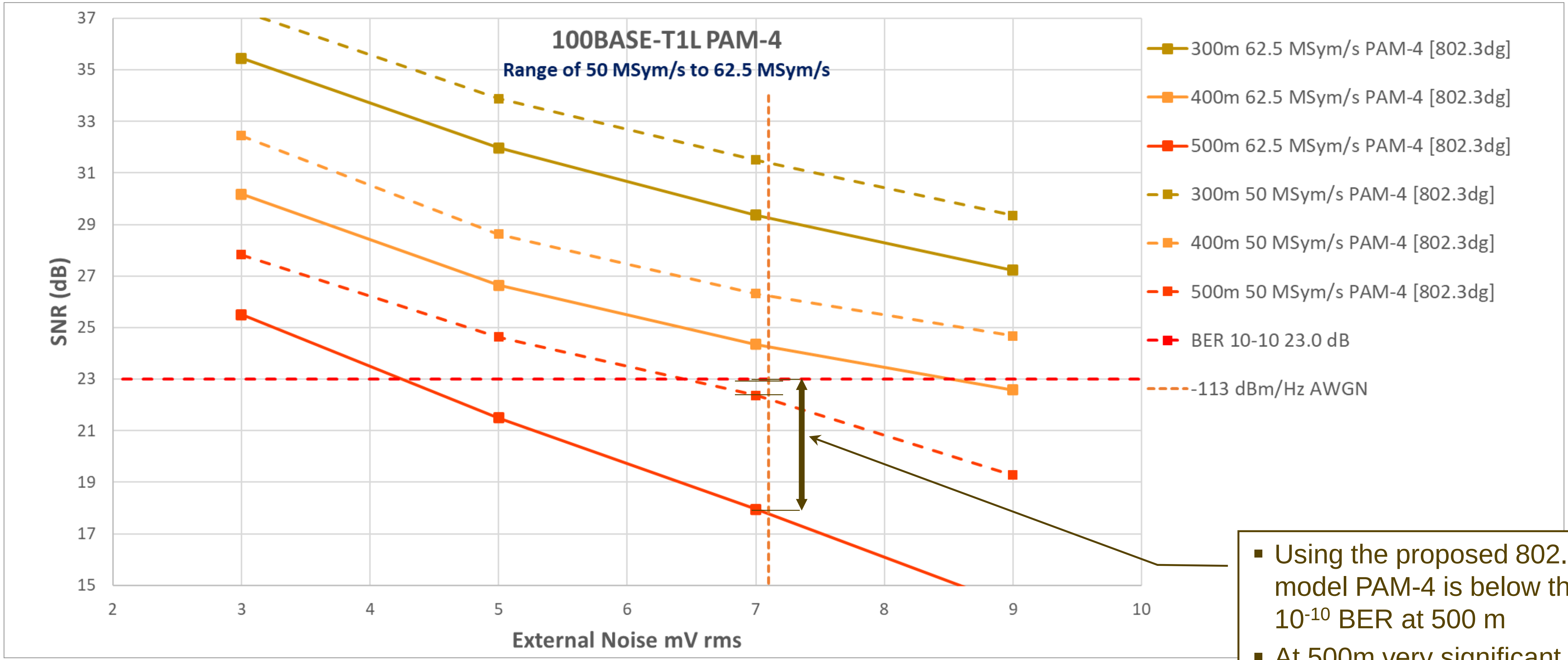
100BASE-T1L 66.66 & 75 MSym/s PAM-3: SNR versus External Noise – 2.4V Tx Amplitude



- Using the proposed 802.3dg IL model PAM-3 is just at the limit of 10^{-10} BER at 500 m
- Small positive range of SNR to trade against symbol rate for coding gain

100BASE-T1L SNR vs Ext Noise – PAM-4 dg IL Model

100BASE-T1L 50 & 62.5 MSym/s PAM-4: SNR versus External Noise – 2.4V Tx Amplitude



- Using the proposed 802.3dg IL model PAM-4 is below the limit of 10^{-10} BER at 500 m
- At 500m very significant SNR to be recovered by coding gain

100BASE-T1L SNR vs Ext Noise – PAM-3 cg IL Model

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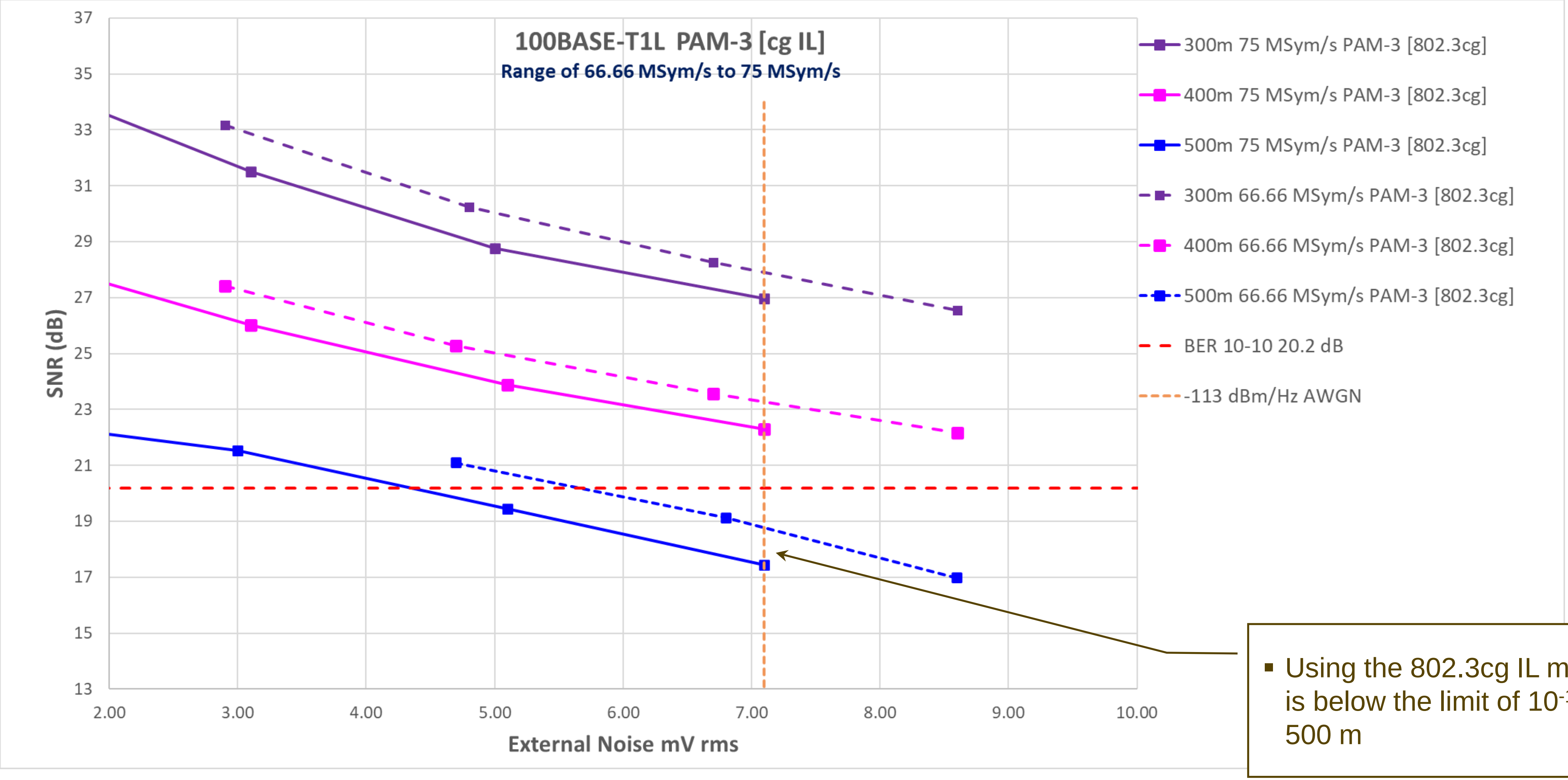
100BASE-T1L 66.66 & 75 MSym/s PAM-3: SNR versus External Noise – 2.4V Tx Amplitude



- Using the 802.3cg IL model PAM-3 is below the limit of 10^{-10} BER at 500 m

100BASE-T1L SNR vs Ext Noise – PAM-4 cg IL Model

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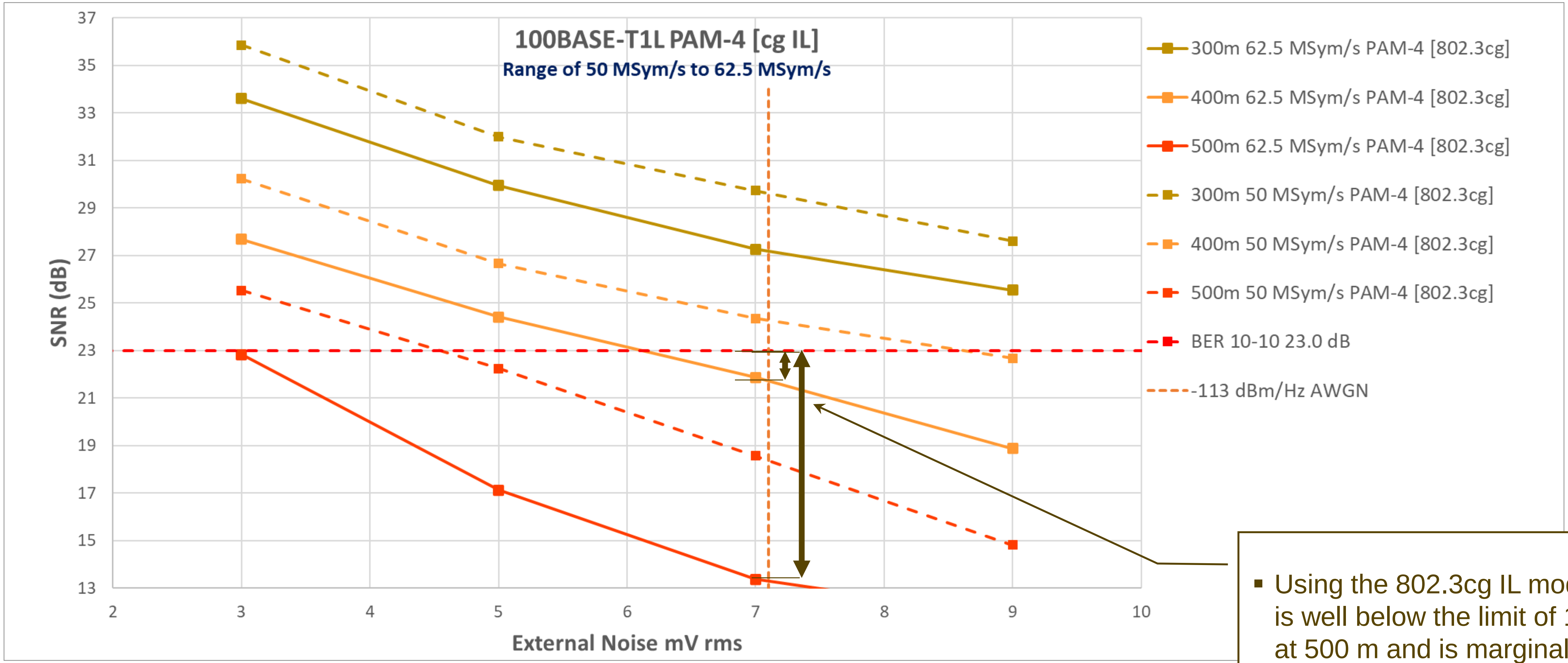
100BASE-T1L 50 & 62.5 MSym/s PAM-4: SNR versus External Noise – 2.4V Tx Amplitude



- Using the 802.3cg IL model PAM-4 is well below the limit of 10^{-10} BER at 500 m and is marginal at 400 m

Comparison of 100BASE-T1L PAM-3 and PAM-4

- A 100BASE-T1L PHY has to cope with an Industrial Ethernet noise environment which has significant AWGN noise due to cross-talk and has non Gaussian impulse noise sources due to EFT
- Comparing PAM-3 and PAM-4 with running disparity at the higher noise level of -113 dBm/Hz shows PAM-4 to have an even greater disadvantage
- PAM-3 inherently has better performance for non-Gaussian impulse noise sources typical in Industrial Ethernet
  - The wider spacing of decision levels is a benefit for every type of noise
- It may be possible to use RS-Coding or other FEC to correct burst errors induced by impulse noise sources at the cost of much higher latency
  - This is only advantageous if the RS-Code can correct the length of errors corresponding to the duration of burst noise induced in the cable and can also cope with the AWGN at the same time
  - And is only necessary if the burst noise induced in the cable is greater than the PAM decision level
  - It has been shown in previous IEEE standards RS-Coding is just as applicable to PAM-3 as PAM-4

Summary

- PAM-3 coding meets the reach requirements of 500 m on the proposed link segment specifications with some SNR margin
- PAM-3 coding schemes can be implemented with low latency by adopting similar approaches to other low speed PHYs like 10BASE-T1L and embed the control codes in the constellation
- PAM-3 has the advantage of wider spacing of decision thresholds which gives the greatest immunity to impulsive noise

Questions ?

Back-up Notes on Using Constellation Control Codes

- In a few presentations I have referred to using constellation control codes as used in lower speed PHYs like 10BASE-T1L and 1000BASE-T compared to block codes like 8B10B, 64B65B, 80B81B used in higher speed PHYs like 10G and the Automotive PHYs
- Here is a (very brief) description of the control codes used in 1000BASE-T to illustrate the concept of constellation control codes
- Firstly, PAM-4 scheme map to nice power of 2 and can be used very efficiently to code binary data
  - However, they have the disadvantage that there are no spare control codes
  - For a higher speed PHY where the block code latency is much lower portion of the overall latency this is not a problem
    - But at 100M a 64B65B block code adding 640 ns of latency – that is very significant

1000BASE-T PCS and Control Codes

- 1000BASE-T used a 4D PAM-5 code and has $5^4 = 625$ permutations
- 512 of these 625 codes are uses as two sets of 256 to encode 8-bits using a Viterbi Coding scheme to achieve 6 dB coding gain
- Leaving 113 codes unused for control codes
  - See Table 40-1 and 40-2 of 1000BASE-T; Section 40.3 Physical Coding Sublayer (PCS)
- During the data frame, the scrambler bits are XORed with the data bits to determine which of the 512 data codes is transmitted
  - At the start and end of the frame SSD and ESD codes are transmitted
  - During Idle 4 bits of the scramble choose which of 16 possible idle codes are transmitted.

g) Ability to rapidly or immediately determine if a symbol stream represents data or idle or carrier extension.

h) Robust delimiters for Start-of-Stream delimiter (SSD), End-of-Stream delimiter (ESD), and other control signals.

i) Ability to signal the status of the local receiver to the remote PHY to indicate that the local receiver is not operating reliably and requires retraining.

IEEE Std 802.3-2022, IEEE Standard for Ethernet
SECTION THREE

Table 40–1—Bit-to-symbol mapping (even subsets) *(continued)*

		$Sd_n[6:8] = [000]$	$Sd_n[6:8] = [010]$	$Sd_n[6:8] = [100]$	$Sd_n[6:8] = [110]$
Condition	$Sd_n[5:0]$	TA_n,TB_n,TC_n,TD_n	TA_n,TB_n,TC_n,TD_n	TA_n,TB_n,TC_n,TD_n	TA_n,TB_n,TC_n,TD_n
Normal	111111	–2,–2,–2,+2	–1,–1,–2,+2	–2,–1,–1,+2	–1,–2,–1,+2
xmt_err	XXXXXX	0,+2,+2,0	+1,+1,+2,+2	+2,+1,+1,+2	+2,+1,+2,+1
CSExtend_Err	XXXXXX	–2,+2,+2,–2	–1,–1,+2,+2	+2,–1,–1,+2	+2,–1,+2,–1
CSExtend	XXXXXX	+2, 0, 0,+2	+2,+2,+1,+1	+1,+2,+2,+1	+1,+2,+1,+2
CSReset	XXXXXX	+2,–2,–2,+2	+2,+2,–1,–1	–1,+2,+2,–1	–1,+2,–1,+2
SSD1	XXXXXX	+2,+2,+2,+2	—	—	—
SSD2	XXXXXX	+2,+2,+2,–2	—	—	—
ESD1	XXXXXX	+2,+2,+2,+2	—	—	—
ESD2_Ext_0	XXXXXX	+2,+2,+2,–2	—	—	—
ESD2_Ext_1	XXXXXX	+2,+2, –2,+2	—	—	—
ESD2_Ext_2	XXXXXX	+2,–2,+2,+2	—	—	—
ESD_Ext_Err	XXXXXX	–2,+2,+2,+2	—	—	—
Idle/Carrier Extension	000000	0, 0, 0, 0	—	—	—
Idle/Carrier Extension	000001	–2, 0, 0, 0	—	—	—
Idle/Carrier Extension	000010	0,–2, 0, 0	—	—	—
Idle/Carrier Extension	000011	–2,–2, 0, 0	—	—	—
Idle/Carrier	000100	0, 0,–2, 0			

Example of a PAM-3 Line code with Control Codes

- So for example, a PAM-3 line code like 7B5T has $5^3 = 243$ permutation of ternary symbols and allowing for running disparity we can encode 7 bits – hence 7B5T
  - Running disparity is achieved by pairing up the codes with positive or negative disparity
    - Code with zero disparity don’t need to be paired up
  - Leaving 25 code unused, including the COMMA code of 5 zeros