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IEEE P802.3dg 100BASE-T1L PHY PAM-3 Time Domain Simulations

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Introduction

- ▶ **The presentation compares time domain results of a 100BASE-T1L PHY architecture for PAM-3 using 4B3T and 8B6T coding**
  - 100BASE-T1L results under the same conditions for PAM-3 4B3T and 8B6T with running disparity
  - Under the same conditions of cross-talk modelled with AWGN

- ▶ **8B6T has a larger codebook of symbols which allows the selection of the set of code group symbols to improve the properties of the line code**
  - 8B6T has 729 possible code groups, each of 6T symbols
    - It is easy to select 6T symbols with a disparity of 0 or pairs of 6T symbols with balanced disparity
    - 256 6T symbols or pairs of 6T symbols are required to represent 8 bits
  - A much larger code space is available than required just for running disparity leaving plenty of spare code groups for control codes like SSD,ESD
  - Greater flexibility in the code space to allows improved distance properties

- ▶ **The results are compared using the AWGN Noise models for PHY Evaluation**
  - _zimmerman_3dgah_01b_01292024.pdf_
  - This approximates to a flat AWGN Noise source at -113 dBm/Hz over 0 to 100 MHz for a 75 MSym/s baud rate which is 7 mV rms

Industrial Ethernet Noise Environment

► A 100BASE-T1L PHY has to cope with an Industrial Ethernet noise environment which has significant AWGN noise due to cross-talk which we model as -113 dBm/Hz which is 7.1 mV rms of noise

  ▪ Simulations have shown that with any modulation scheme so far considered, dealing with this noise is a very significant challenge at 500m

► The 100BASE-T1L PHY also has to cope with impulse noise originating from sources of Electrical Fast Transients

  ▪ Results have been presented (Brychta_3dg_update_B_2024-Mar-09) that show that the amplitude of these impulse noise sources at the ADC in the PHY is at a level that errors will result at the slicer unless we can maximise the distance between the decision levels

  ▪ The combination of moderate amounts of AWGN and impulse noise is an even bigger challenge

► PAM-3 maximizes the spacing of the decisions at the slicer to best deal with the combination of noise sources typical in Industrial Ethernet to minimize errors

  ▪ The selection of the PAM-3 line code and the selection of the code group symbols within the code group space can be used to further improve the performance in the Industrial Ethernet noise environment

► PAM-4 modulation operates at a higher bit to symbol ratio, which allows error correction bits to be used by a FEC to correct decoded symbol errors

  ▪ However, as PAM-4 reduces the spacing of the decisions at the slicer more errors occur than the FEC can correct

100BASE-T1L and Running Disparity

▶ **Running disparity is an important advantage for 10 and 100BASE-T1L**

- Running disparity is important to support Intrinsic Safety systems

- Running disparity is important to limit the cost of external components in SPoE

- Running disparity limits Base Line Wander which reduces the peak to mean at the ADC and improves the performance of the DFE

▶ **The transmitter can use running disparity to control the properties of the transmit signal without adding any transmit analog complexity**

PAM-3 Modulation Schemes and Bits/Symbol

▶ The theoretical limit of PAM-3 is 1.58 bits/symbol (without running disparity) which corresponds to 63 MSym/s at 100Mb/s

- Many PAM-3 modulation schemes support running disparity at bits/symbol rates closer to the theoretical limit than the simple 4B3T scheme used in 10BASE-T1L

PAM-3 Modulation	Bits/Symbol	100Mb/s Symbol Rate (M)	2^n	Available Code Groups	Ratio CG/2^n	Running Disparity Bound
3B2T	1.50	66.66	8	9	1.1	No
4B3T	1.33	75.00	16	27	1.7	Yes ±1.5
7B5T	1.40	71.43	128	243	1.9	Yes ±1.5
8B6T	1.33	75.00	256	729	2.8	Yes ±1.0
9B6T	1.50	66.66	512	729	1.4	No
10B7T	1.43	71.43	1024	2187	2.1	Yes ±1.5
13B9T	1.44	69.23	8192	19683	2.4	Yes ±1.0
15B10T	1.50	66.66	32768	59047	1.8	Yes ±2.5

- Operating at a higher bit/symbol ratio lowers the symbol rate and uses a better frequency range of the channel
- Choosing a line code with a greater ratio of available code groups gives greater flexibility in choosing codes
  - And there are many additional code groups available for control codes

Challenge of Achieving Coding Gain

▶ The big challenge of 100BASE-T1L is how to achieve sufficient performance margin at 500m in the Industrial Ethernet noise environment to meet a 10^{-10} bit error rate

- Simulations have shown that the SNR margin using a standard DFE is not sufficient and some performance gain is required to have margin to the 10^{-10} bit error rate requirement

- Choosing code groups with greater spacing between the code groups in the 6T code space results in a performance gain that can be used to achieve better bit error rate performance

Advantages of 8B6T Coding Scheme

▶ Using a PAM-3 modulation scheme with a higher number of symbols in the code group allows the design of a code to address these challenges

▶ A large ratio of available code groups to required code groups allows codes to be chosen to achieve particular desired properties of a code

  ▪ For example, this can be used to achieve greater distance spacing between codes

▶ Some PAM-3 line codes like 10B7T, 13B9T and 15B10T have higher bits/symbol ratios than 4B3T, support running disparity and also can have greater spacing between the chosen code groups to achieve performance gain

▶ The 8B6T line code has a very high ratio of available codes to required codes giving a large space to choose code groups with a greater distance spacing between codes

  ▪ We have considered 8B6T first as it has the highest ration of available codes to required codes

PAM-3 8B6T Line Code

▶ We constructed the a PAM-3 8B6T line code using the following set of 425 code groups chosen from the 729 available codes

8B6T Code Groups	Running Disparity	Number of Codes	Code Pairs
Set 0	0	87	87
Set 1	1	79	79
Set 2	2	58	58
Set 3	3	32	32
Set 1neg	-1	79	
Set 2neg	-2	58	
Set 3neg	-3	32	
Total Number of Codes		**425**	**256**

Example of first 10 rows of the table

										Change	
PAM3_8B6T											
Index	CG Row	Base_3	TA_n	TB_n	TC_n	TD_n	TE_n	TF_n		Pattern	RD+/-
0	222	022020	-1	1	1	-1	1	-1		- + + - + -	0
1	506	200202	1	-1	-1	1	-1	1		+ - - + - +	0
2	510	200220	1	-1	-1	1	1	-1		+ - - + + -	0
3	542	202002	1	-1	1	-1	-1	1		+ - + - - +	0
4	546	202020	1	-1	1	-1	1	-1		+ - + - + -	0
5	344	110202	0	0	-1	1	-1	1		0 0 - + - +	0
6	348	110220	0	0	-1	1	1	-1		0 0 - + + -	0
7	380	112002	0	0	1	-1	-1	1		0 0 + - - +	0
8	384	112020	0	0	1	-1	1	-1		0 0 + - + -	0
9	290	101202	0	-1	0	1	-1	1		0 - 0 + - +	0
10	294	101220	0	-1	0	1	1	-1		0 - 0 + + -	0

▶ The PAM-3 8B6T line code shown here is an example using a relatively small code space of 729 codes

- We would not propose using 8B6T line code in 100BASE-T1L, but would propose using a similar approach with a higher order code like 10B7T, 13B9T and 15B10T to achieve a greater bits/symbol efficiency
- 8B6T is used as an example to illustrate the concepts

100BASE-T1L PAM-3 Time Domain Simulation

▶ Compare 100BASE-T1L PAM-3 4B3T and 8B6T under the same conditions

▶ Generic 100BASE-T1L Architecture with following parameters

- PAM-3 using 802.3cg Scrambler and 802.3cg 4B3T PCS with running disparity at 75 MSym/s
- PAM-3 using 802.3cg Scrambler and 8B6T PCS with running disparity at 75 MSym/s
- Ideal DAC & line driver, 2.4V Tx, 12-bit ADC
- DFE using 48 feed forward taps and 64 feedback taps, ideal data path

▶ 802.3cg and 802.3dg Insertion Loss model

802.3dg IL	$IL(f) \leq \left(5.42 \times \sqrt{f} + 0.044 \times f + \dfrac{1.76}{\sqrt{f}}\right) + 5 \times 0.02 \times \sqrt{f}$ (dB)
802.3cg IL	$IL(f) \leq 10\left(1.23 \times \sqrt{f} + 0.01 \times f + \dfrac{0.2}{\sqrt{f}}\right) + 10 \times 0.02 \times \sqrt{f}$ (dB)

▶ External Noise Model proposed in

- Noise with a Gaussian distribution and magnitude of **–113 dBm/Hz**
- 7 mV rms over a flat 100 MHz

Figure 146–24—Alien crosstalk noise rejection test set-up

100BASE-T1L SNR vs Ext Noise
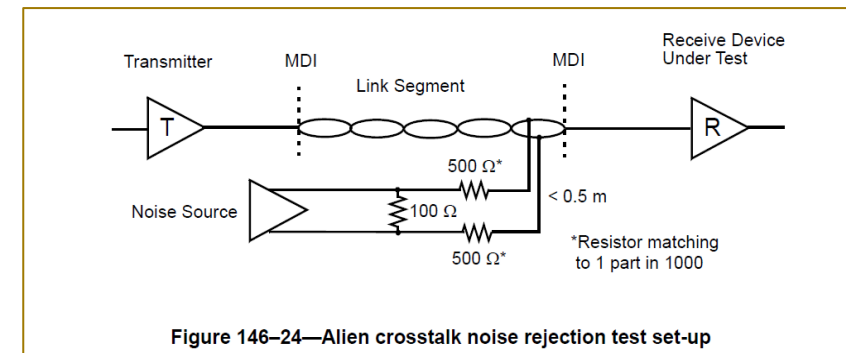
▶ Plot SNR versus external Gaussian noise

- For values of 3, 5, 7 and 9 mV rms
- For cable lengths 300, 400, 500 m
- For Insertion Loss cable model proposed for 802.3dg and IL model used in 802.3cg
- At 2.4V transmit level
- After 1546K symbols of start-up, idle and data (~ 20000 µs)
  - Enter data after 240K symbols

▶ Compare 100BASE-T1L PAM-3 4B3T with 8B6T with running disparity

- 75 MSym/s PAM-3 4B3T
- 75 MSym/s PAM-3 8B6T

Generic 100BASE-T1L PHY Architecture

► Generic block diagram of a BASE-T PHY architecture
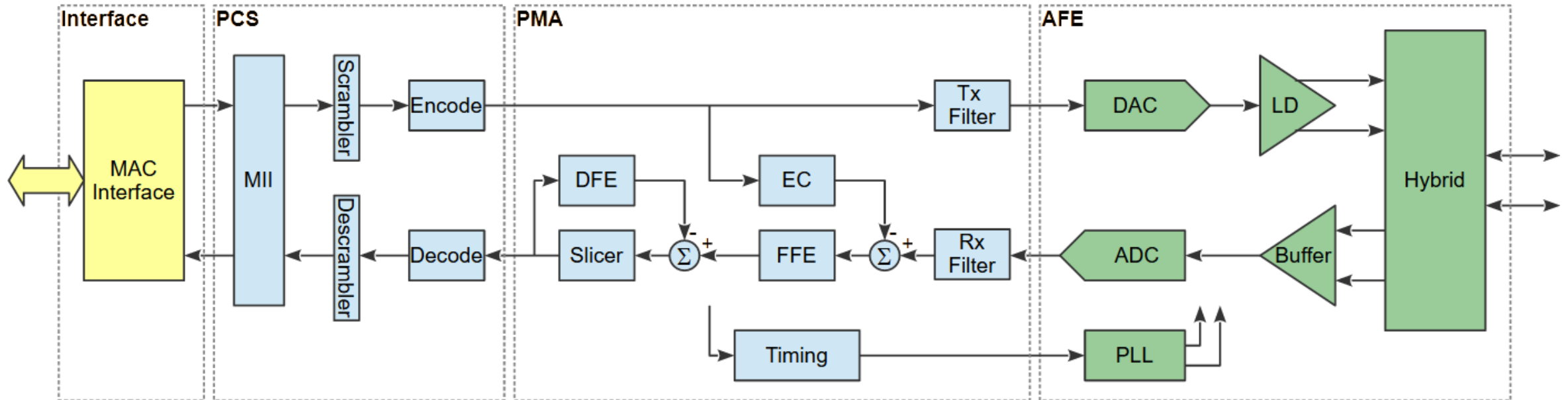
► A time domain simulation is run for a range of cable lengths / noise to determine SNR margin verses reach

Other example PHY architecture diagrams
10BASE-T1L .cg Jan 2017 Graber_10SPE_10_0117.pdf

SNR verses BER or Packet Error Rate

▶ **802.3dg standard mandates a BER ≤ 10^{-10}**

- PAM-3 4B3T coding has a symbol power of 0.64422 and requires an SNR of 20.2 dB for a BER ≤ 10^{-10}

- PAM-4 4B2T coding has a symbol power of 0.55555 and requires an SNR of 23.0 dB for a BER ≤ 10^{-10}
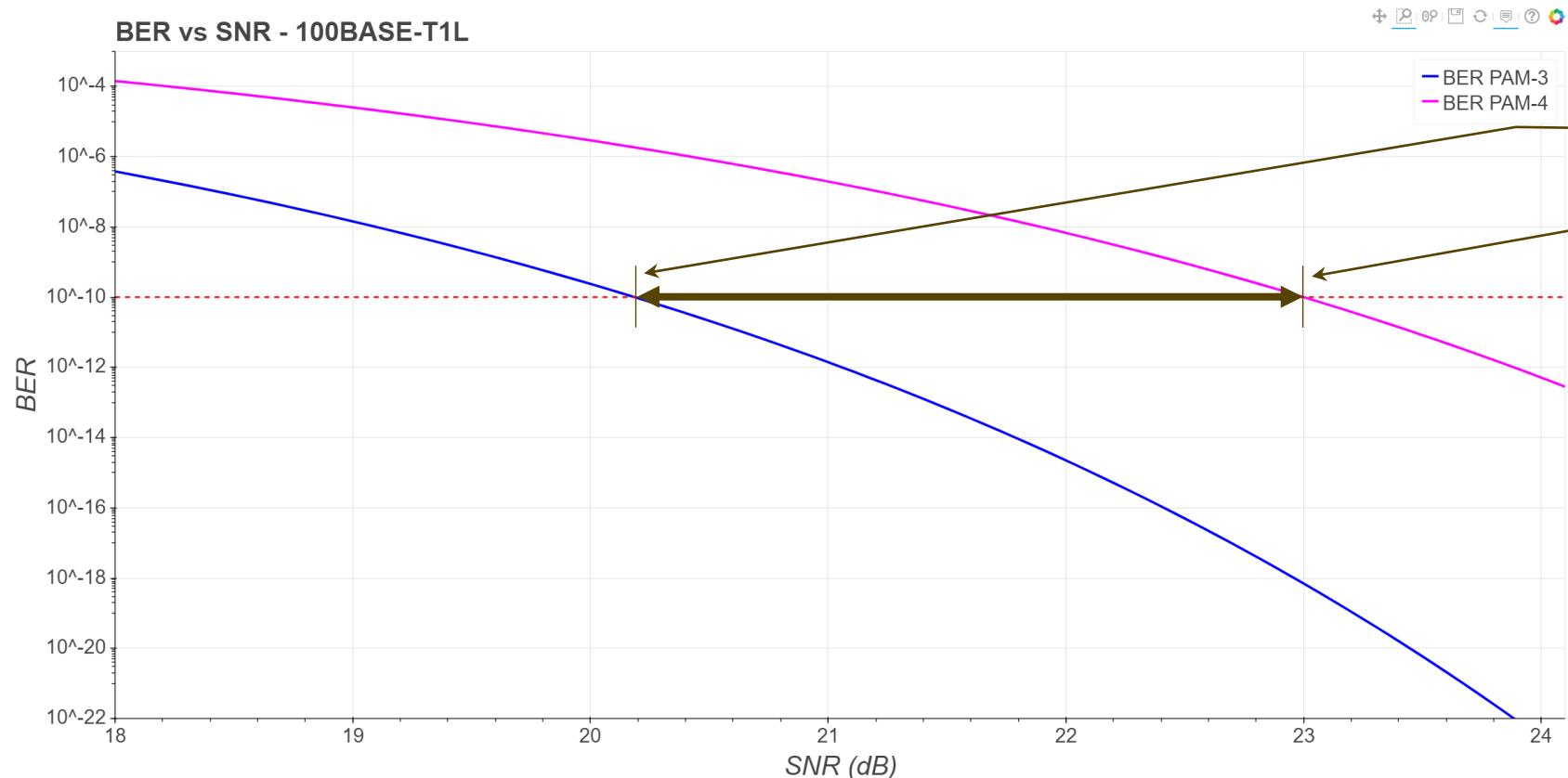
10^{-10} BER
- PAM-3 requires 20.2 dB
- PAM-4 requires 23.0 dB

100BASE-T1L PAM-3 8B6T 802.3dg IL – 400m / 5 mV rms Noise

Start-up Eye Diagram

SNR Convergence 0 – 20 ms

25dB →

PAM-3 Eye Diagram During Data

Time Domain Waveforms during Data
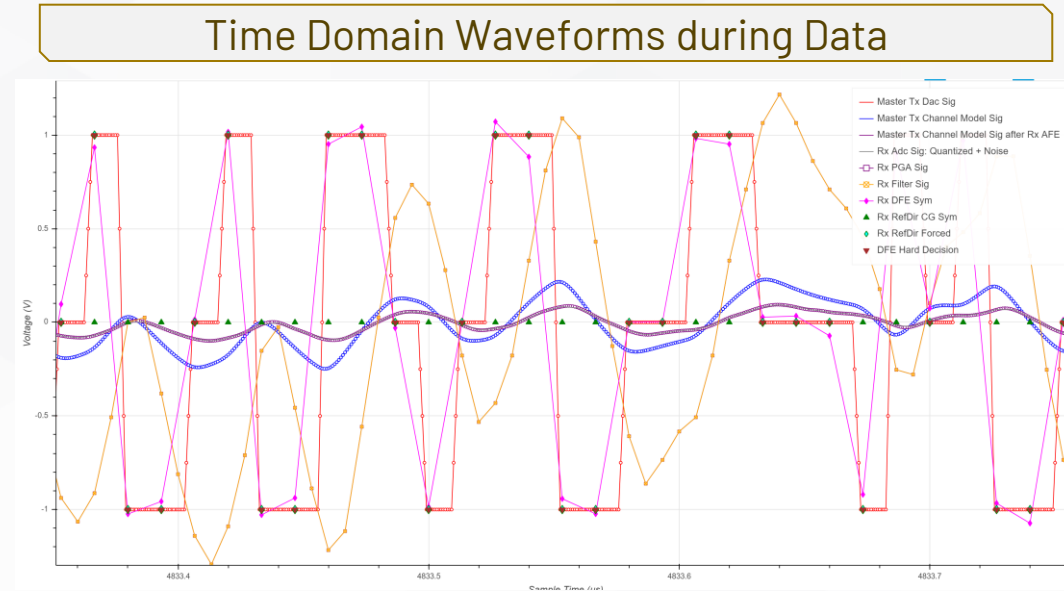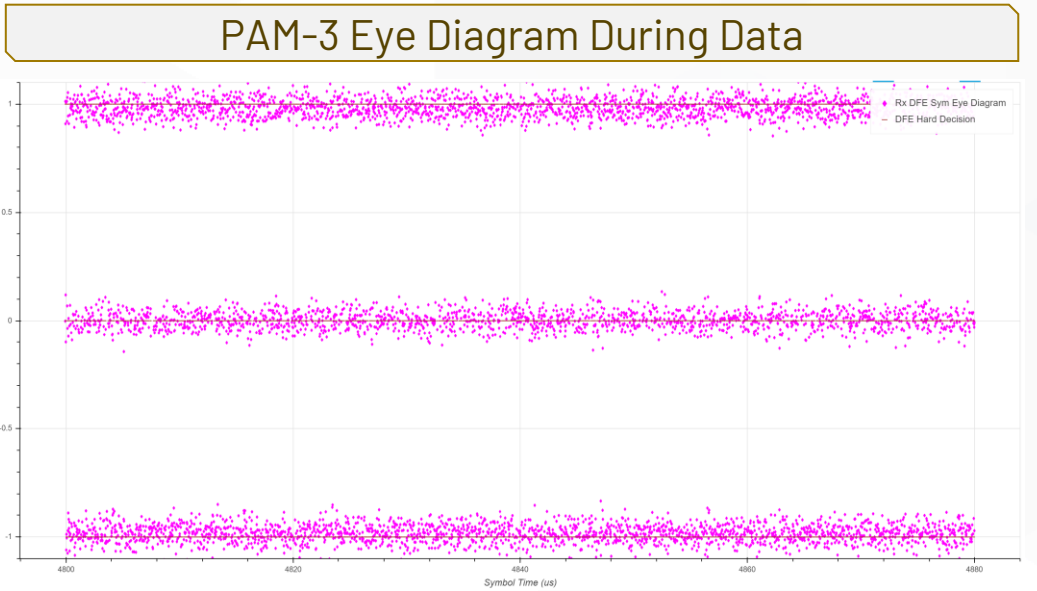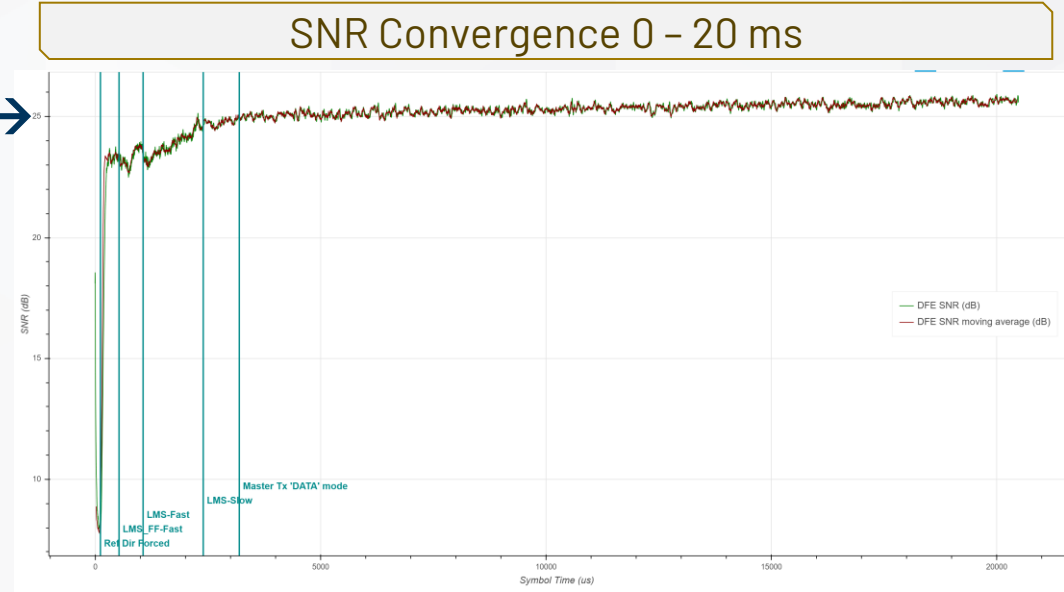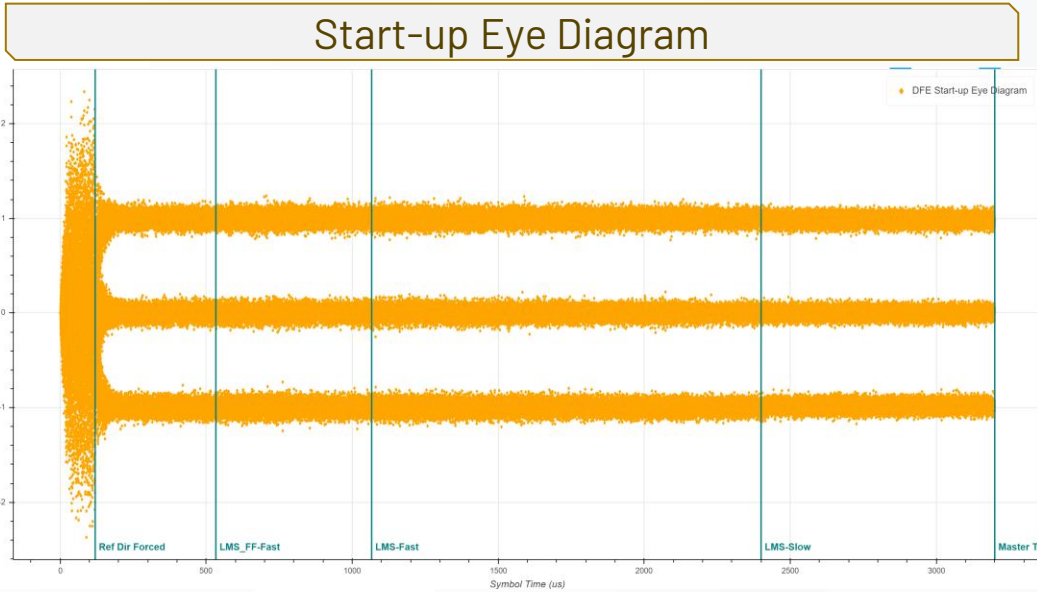
100BASE-T1L PAM-3 8B6T 802.3dg IL – 500m / 9 mV rms Noise

Start-up Eye Diagram
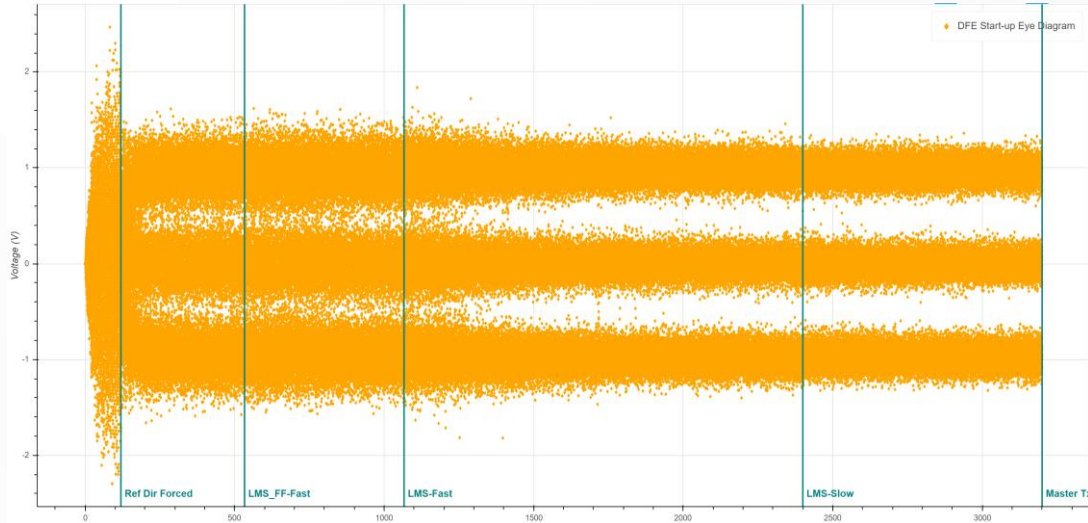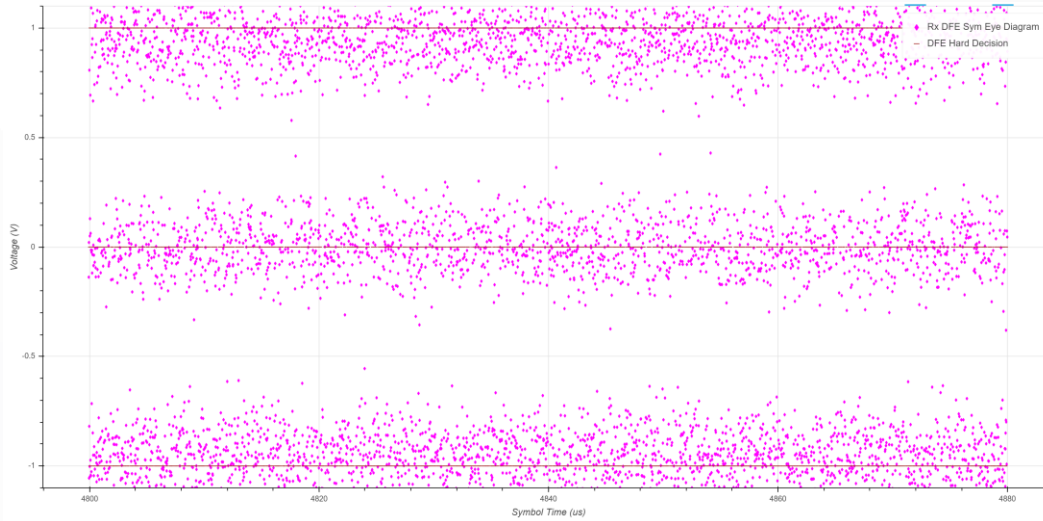

SNR Convergence 0 – 20 ms
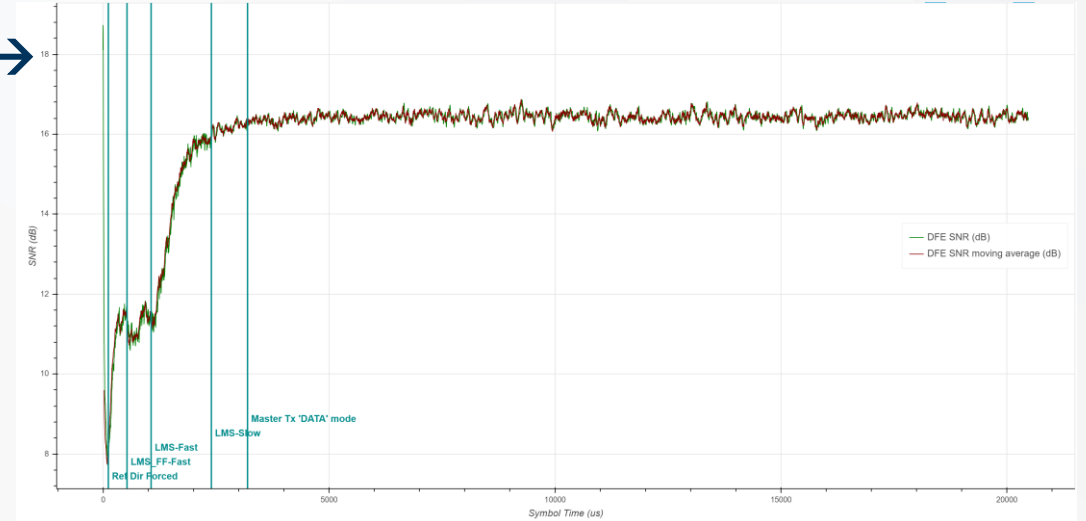
18dB →
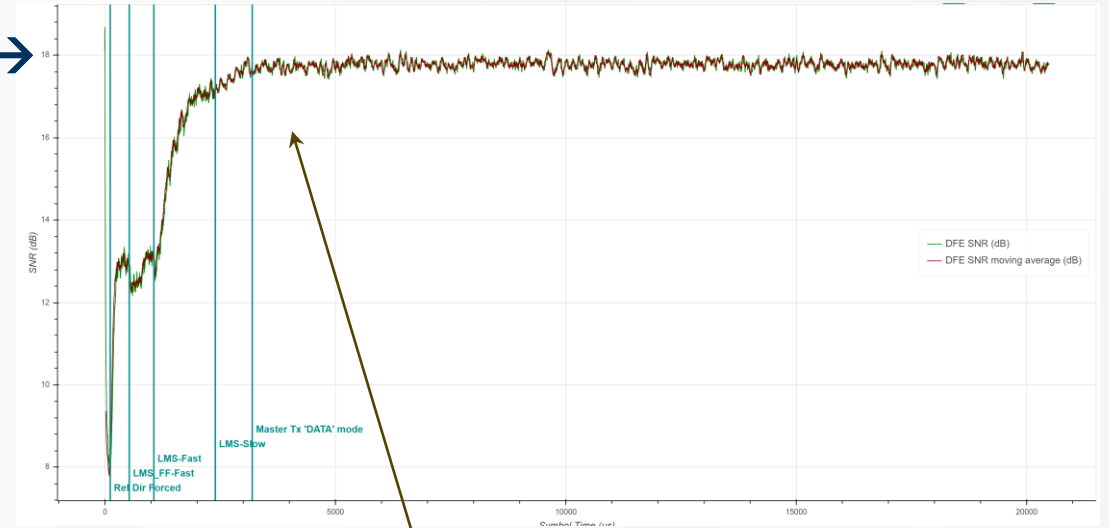
PAM-3 Eye Diagram During Data
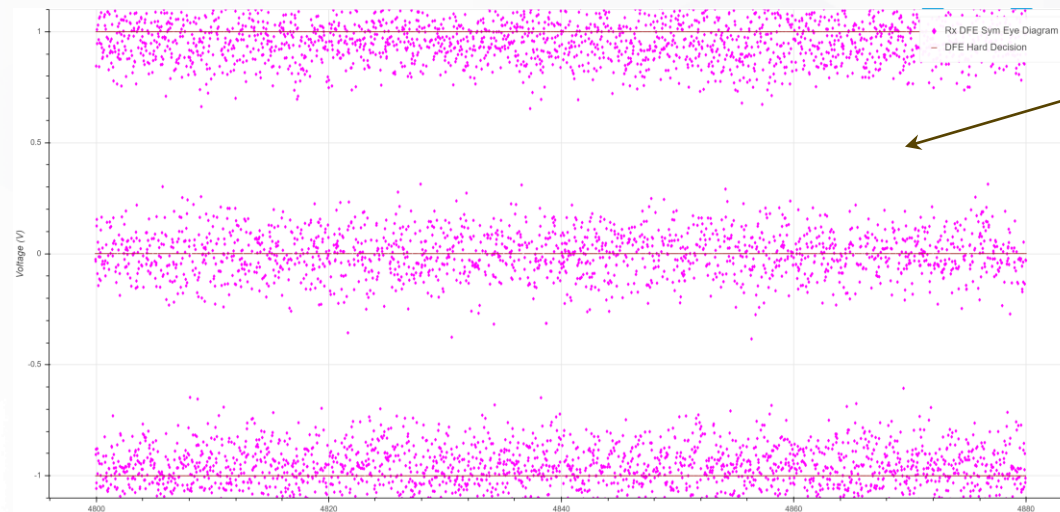
- At 500m and 9 mV of noise we are into the region of negative margin to the 10^{-10} BER threshold
- However, the DFE is still very well behaved but with a poor error rate
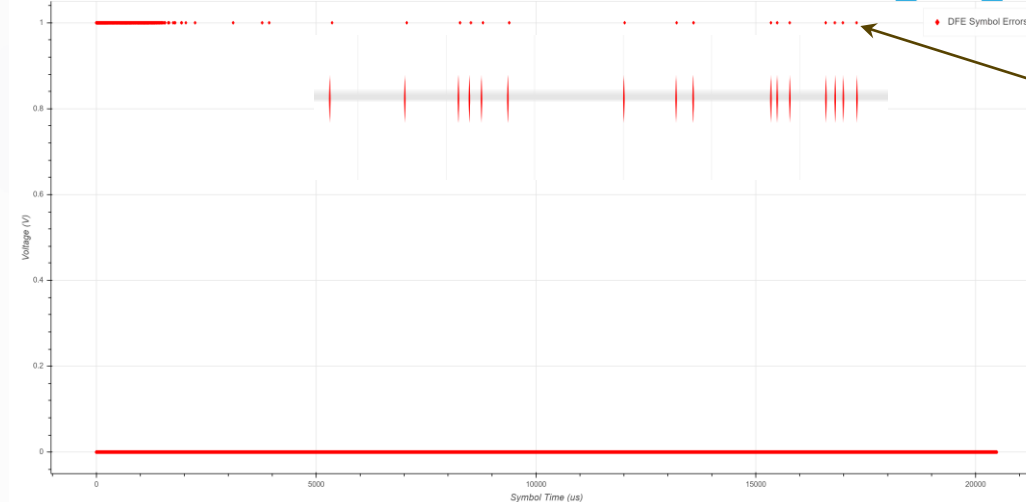
PAM-3 Eye Diagram During Data

SNR Convergence 0 – 20 ms

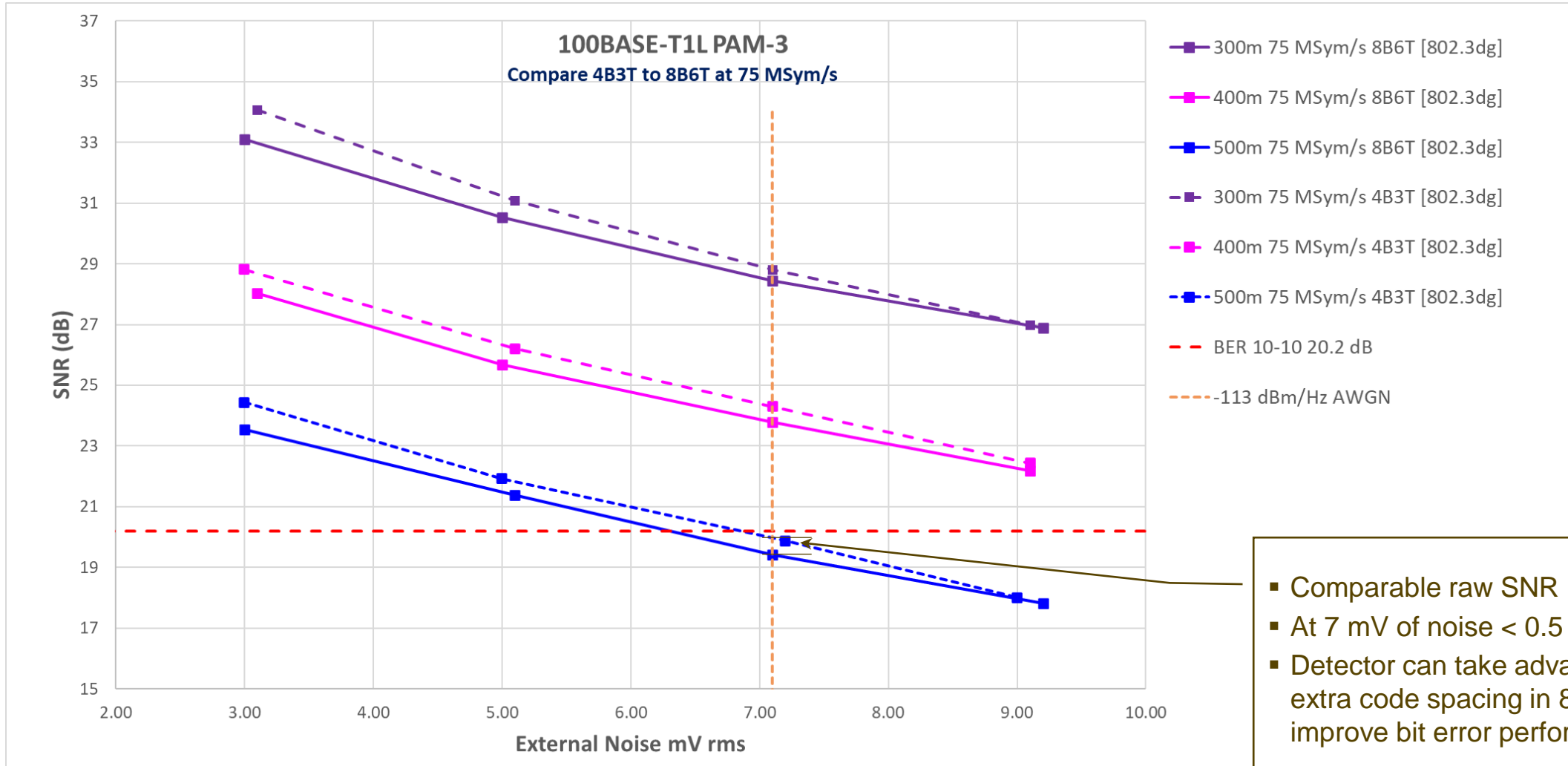**18dB →**

DFE Symbol Errors During Data

- However, at 500m and 7 mV of noise with an 802.3cg cable model we are well into the region of negative margin
- The DFE is holding up but even in a short simulation we see errors
- We are close to the point of collapse

100BASE-T1L 75 MSym/s PAM-3 4B3T and 8B6T: SNR versus External Noise – 2.4V Tx Amplitude
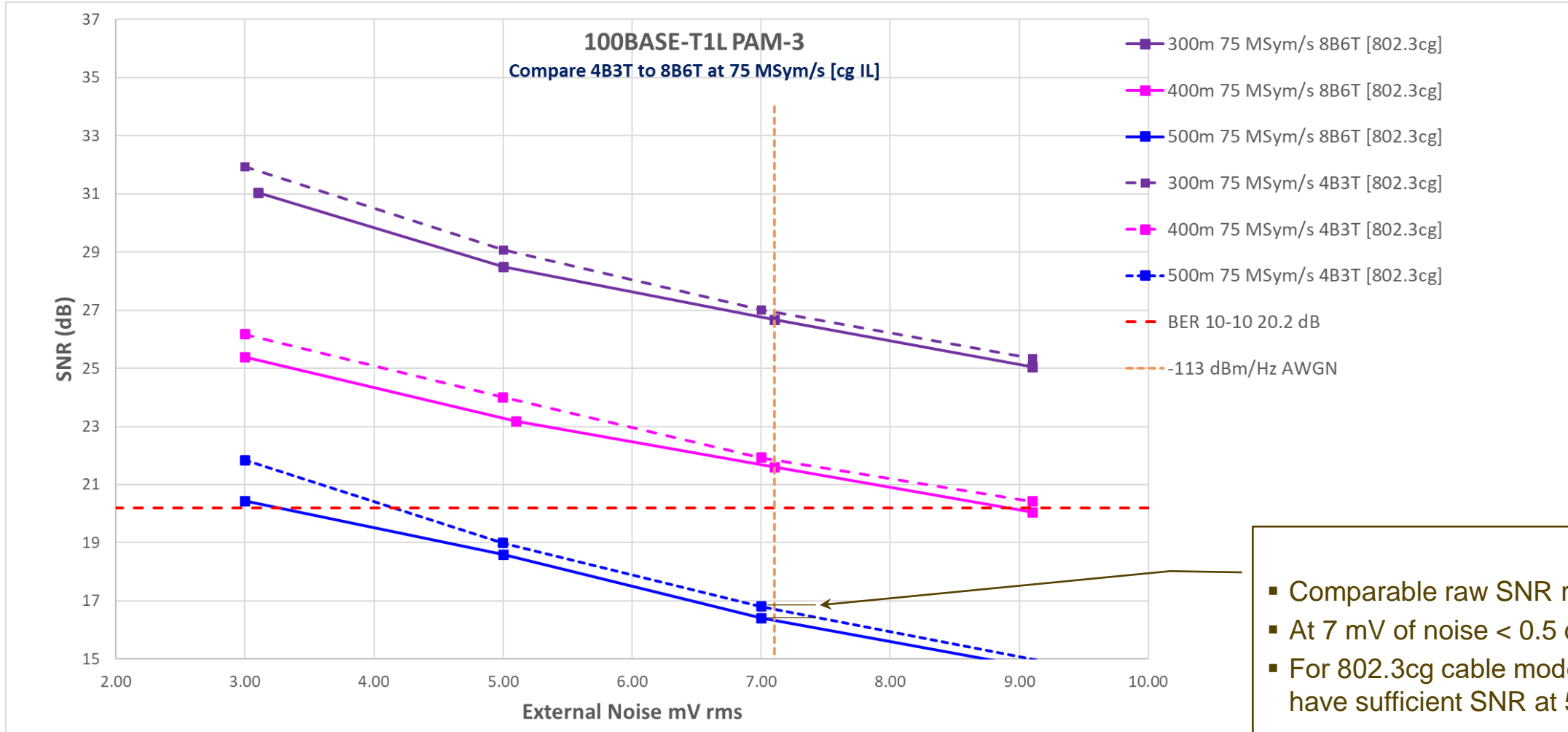

- Comparable raw SNR results
- At 7 mV of noise < 0.5 dB difference
- Detector can take advantage of the extra code spacing in 8B6T to improve bit error performance

100BASE-T1L 75 MSym/s PAM-3 4B3T and 8B6T: SNR versus External Noise – 2.4V Tx Amplitude

- Comparable raw SNR results
- At 7 mV of noise < 0.5 dB difference
- For 802.3cg cable model we don't have sufficient SNR at 500m

Summary

▶ PAM-3 coding meets the reach requirements of 500 m on the proposed link segment specifications with some SNR margin

▶ PAM-3 has the advantage of wider spacing of decision thresholds which gives the greatest immunity to impulse noise

▶ PAM-3 coding with higher order codes can give higher bit/symbol efficiency and performance gain due to greater spacing between the chosen code groups

▶ PAM-3 coding schemes can be implemented with low latency by adopting similar approaches to other low speed PHYs like 10BASE-T1L and embed the control codes in the constellation

Questions ?