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IEEE P802.3dg 100BASE-T1L PHY Time Domain Simulations

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Introduction

- This presentation covers some considerations for the definition of the PHY line coding for 100BASE-T1L; continues from Murray_3dg_01a_07102023
- The presentation gives some example time domain results of a generic BASE-T1L PHY architecture
  - Example 10BASE-T1L results verses 10BASE-T1L silicon measurements
  - Example 100BASE-T1L results under the same conditions
- Results continue to show that we can use PAM-3 or PAM-4 or PAM-5
- The presentation outlines test bench (channel, noise model) that we need to agree on, to use to evaluate time domain simulation results
  - We have some clarity on the channel model from the adopted Link Segment (as of 9/7/23)
  - Work still to be done to agree a noise model
- This will allow us to compare PAM-3, PAM-4, PAM-5 modulation

Recap - Analysis Required to make PHY Line Code Decisions

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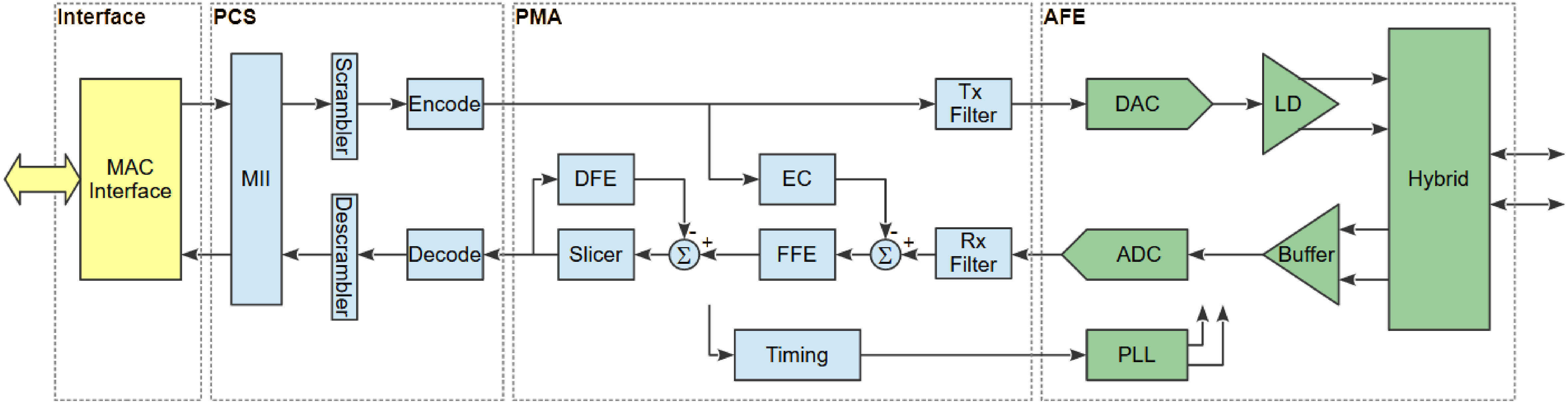
- How do we decide on the line coding?
  - PAM-3 or PAM-4 or PAM-5 and PCS encoding
- What work / analysis do we need to do?
  - What methodologies do we employ for that work?
- What results do we need to enable the Task Force to decide

What are the Trade-Offs

- Reach v Performance
  - BER and SNR margin over 0 to 500 m
  - In presence of AWGN and EFT
- Cost/Complexity: PHY power, analog performance needed, digital gates
- Impact on SPoE: External component cost

Recap - Standard BASE-T PHY Architecture

- Generic block diagram of a BASE-T PHY architecture



- A time domain simulation is run for a range of cable lengths / noise to determine SNR margin verses reach

Other example PHY architecture diagrams
10BASE-T1L .cg Jan 2017 Graber_10SPE_10_0117.pdf

BASE-T1L Time Domain Simulation

- The following is the basis for these results comparing 10 and 100 BASE-T1L
- Generic BASE-T1L Architecture with following parameters
  - PAM-3 using 802.3cg 4B3T PCS and Scrambler
  - Ideal DAC and line driver
  - 12-bit ADC with 50 dB Gaussian noise to allow for datapath, non idealities, etc.
  - DFE using 48 feed forward taps and 64 feedback taps, ideal data path
- 802.3cg Insertion Loss model (Clause 146.7.1.1.1)

$$\text{Insertion loss}(f) \le 10\left(1.23 \times \sqrt{f} + 0.01 \times f + \frac{0.2}{\sqrt{f}}\right) + 10 \times 0.02 \times \sqrt{f} \quad (\text{dB})$$

- 802.3cg External Noise Model
  - Noise with a Gaussian distribution, bandwidth of 10 MHz, and magnitude of –106 dBm/Hz
  - ~ 5mV rms
  - Use 5mV rms over 10 or 100MHz

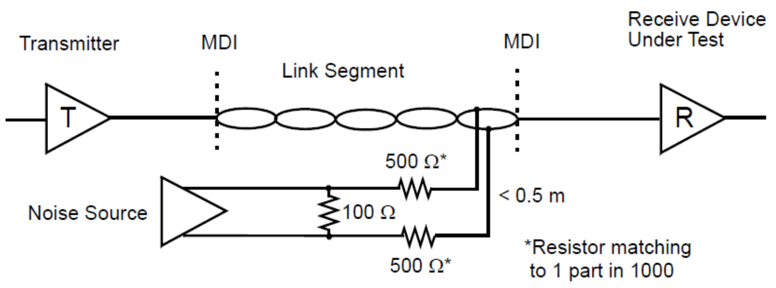
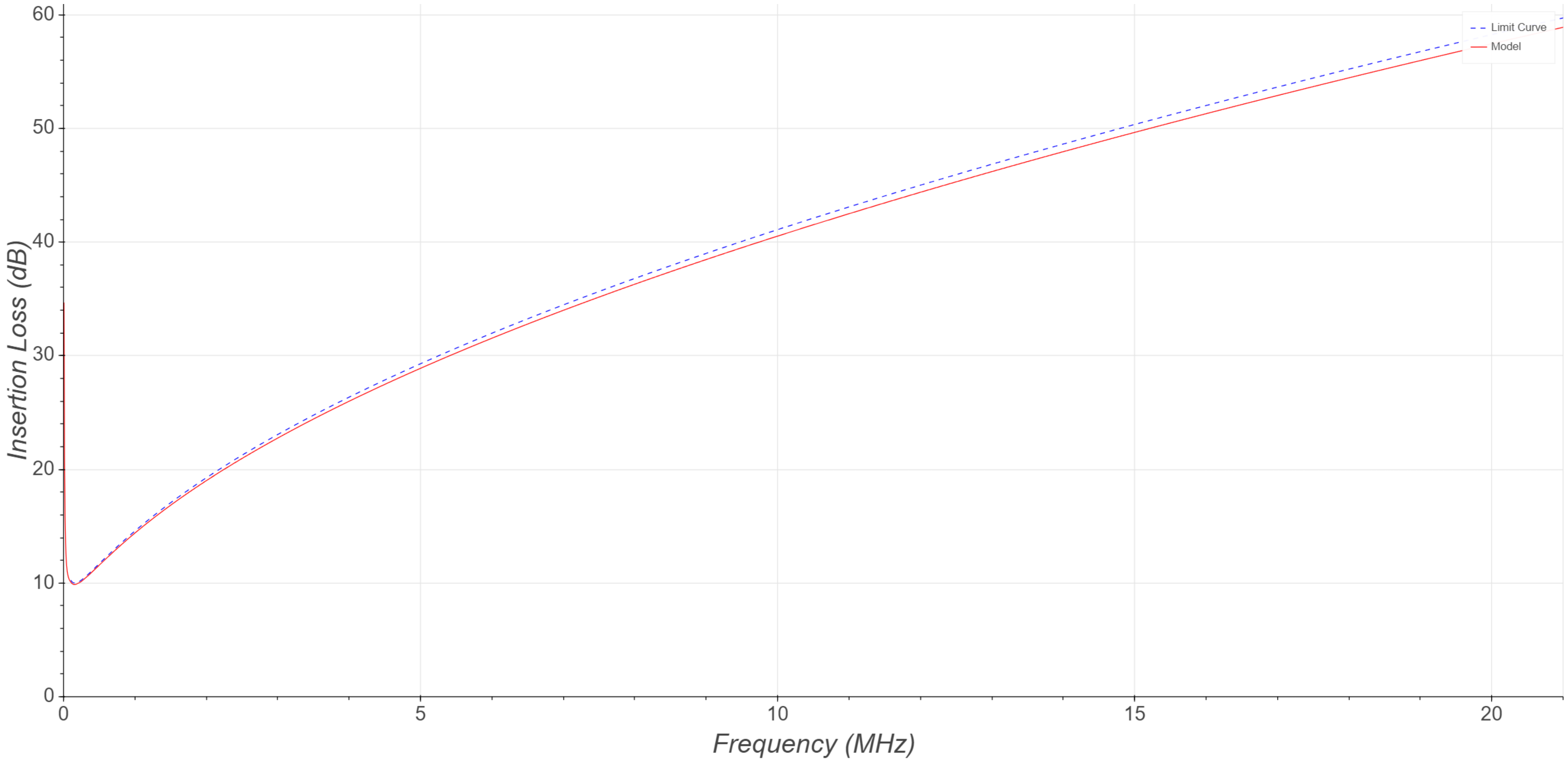


Figure 146–24—Alien crosstalk noise rejection test set-up

This is overkill – but focus is on Channel & Noise

- For these example results compare 10BASE-T1 & 100 BASE-T1L under the same conditions
- Use 802.3cg as initial reference point

Insertion Loss 1000m – 802.3cg



Example 10BASE-T1L 1000m with 5 mV rms Noise

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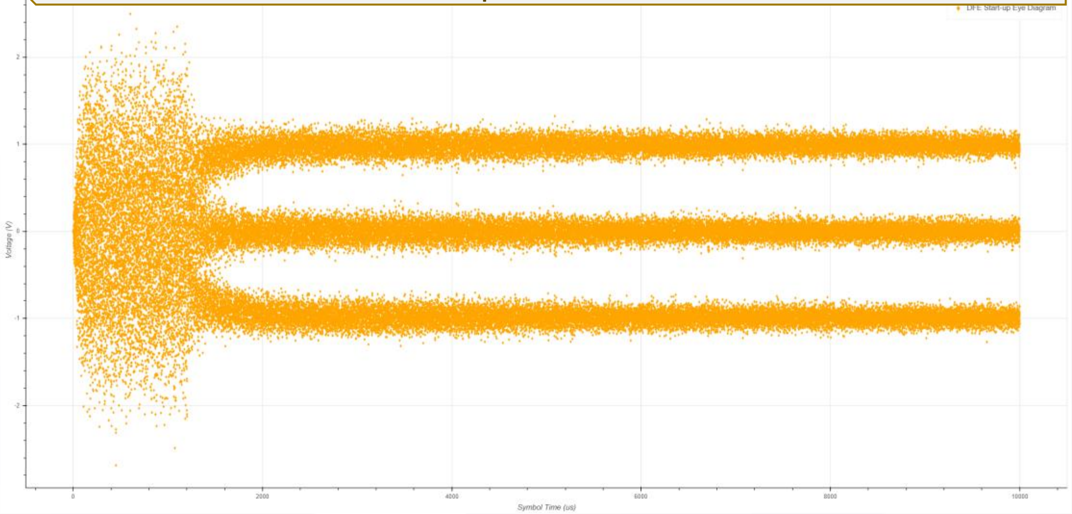
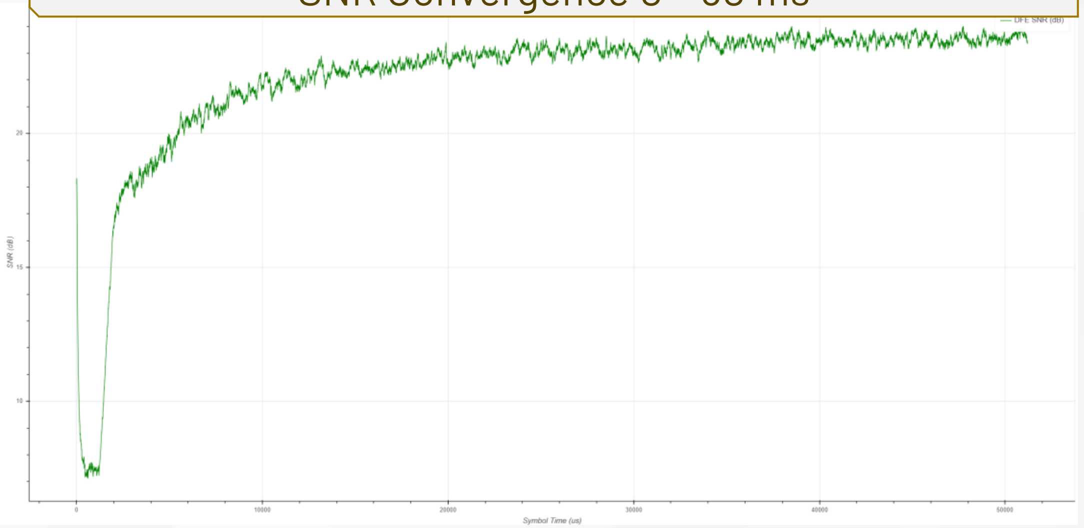
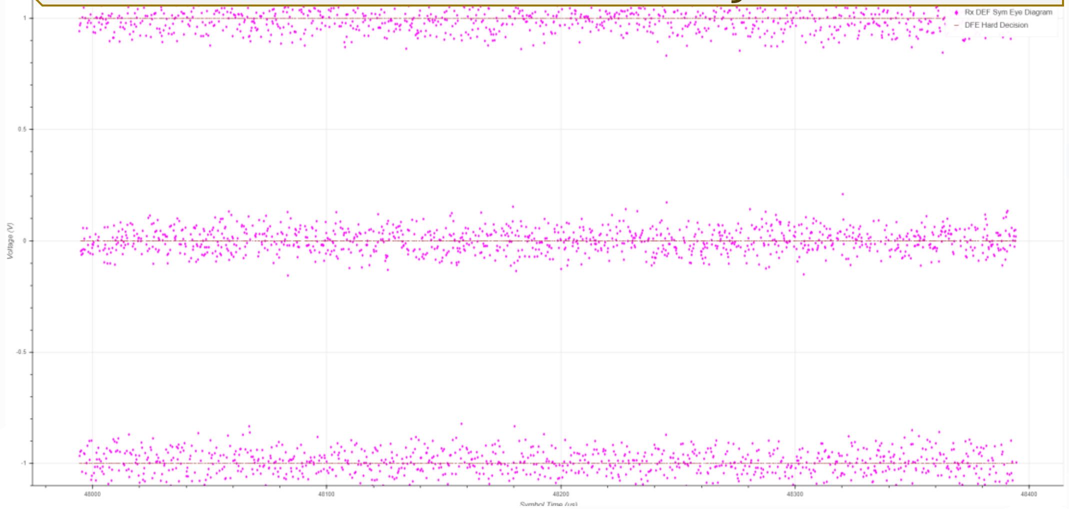
Start-up Data Pattern



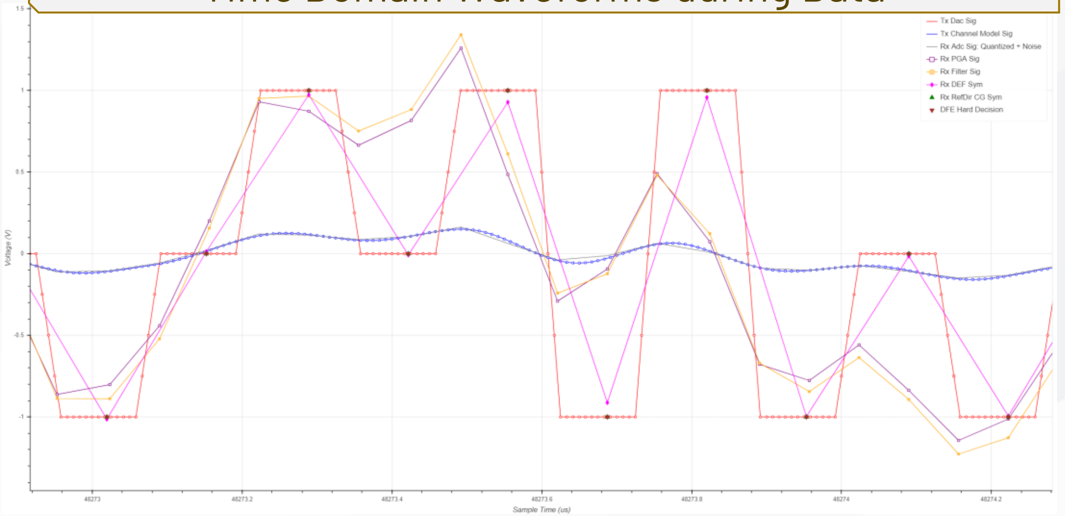
SNR Convergence 0 – 50 ms



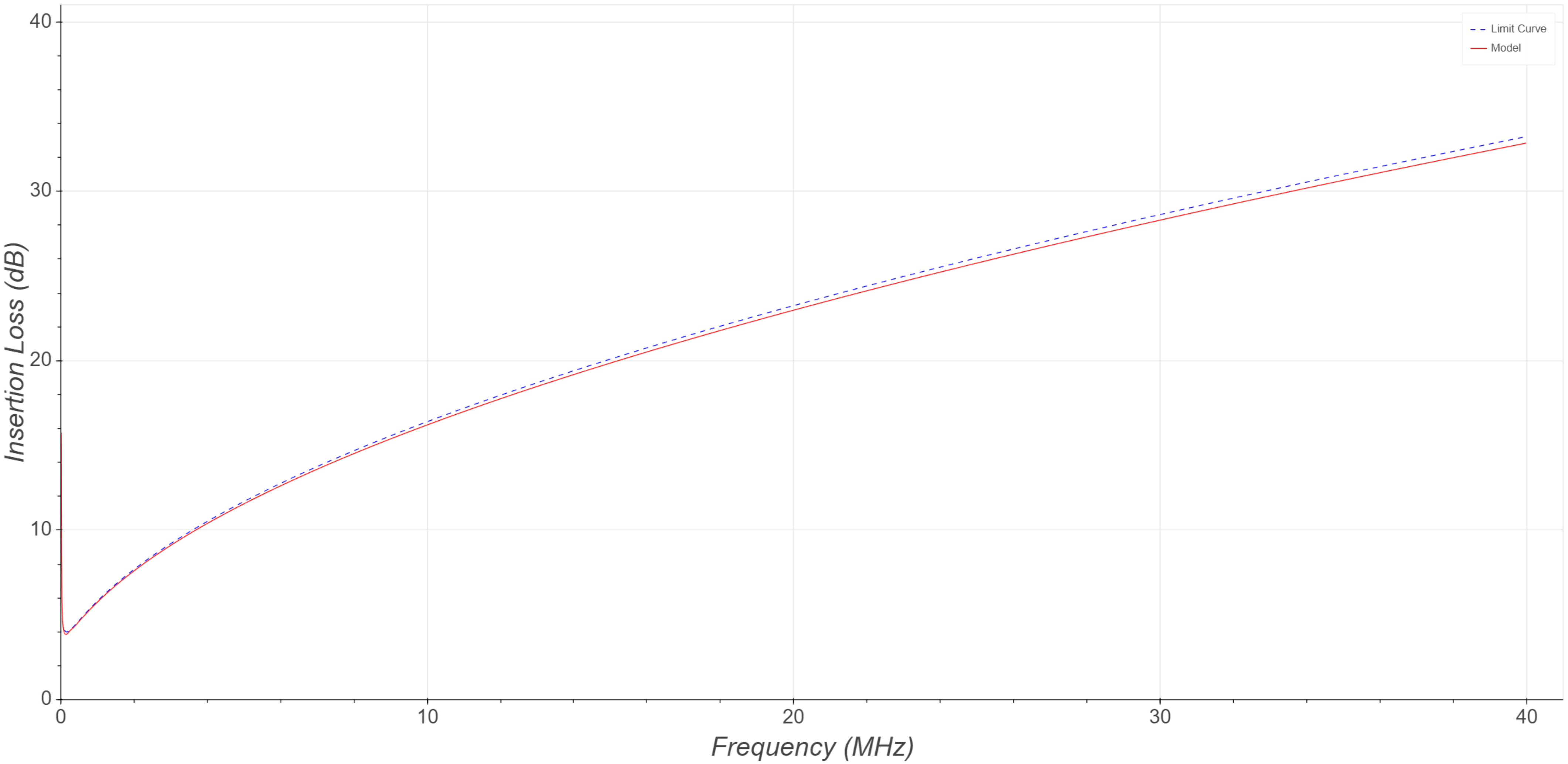
PAM-3 Data Pattern During Data



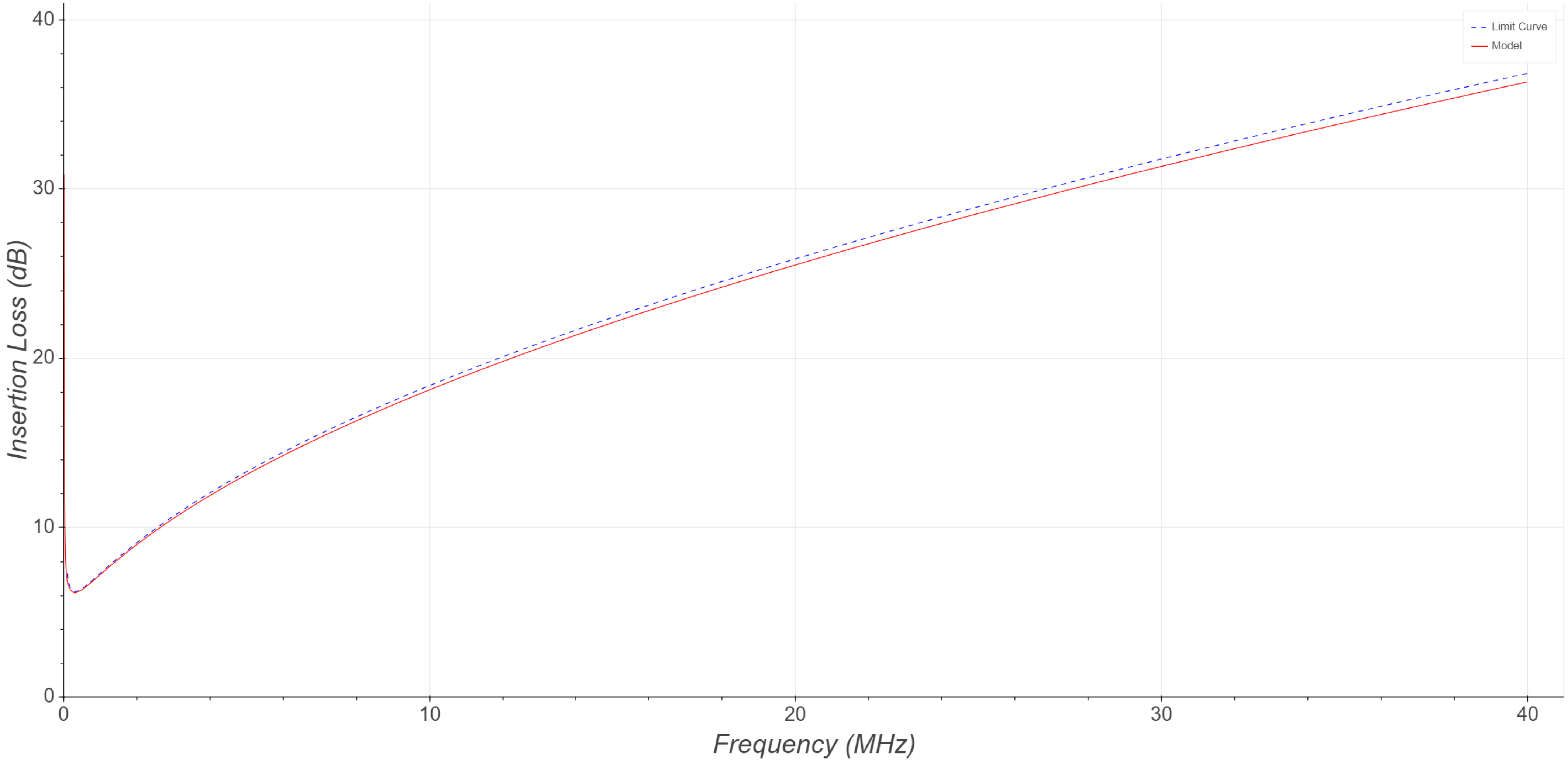
Time Domain Waveforms during Data



Insertion Loss 400m – 802.3cg Extended to 40 MHz

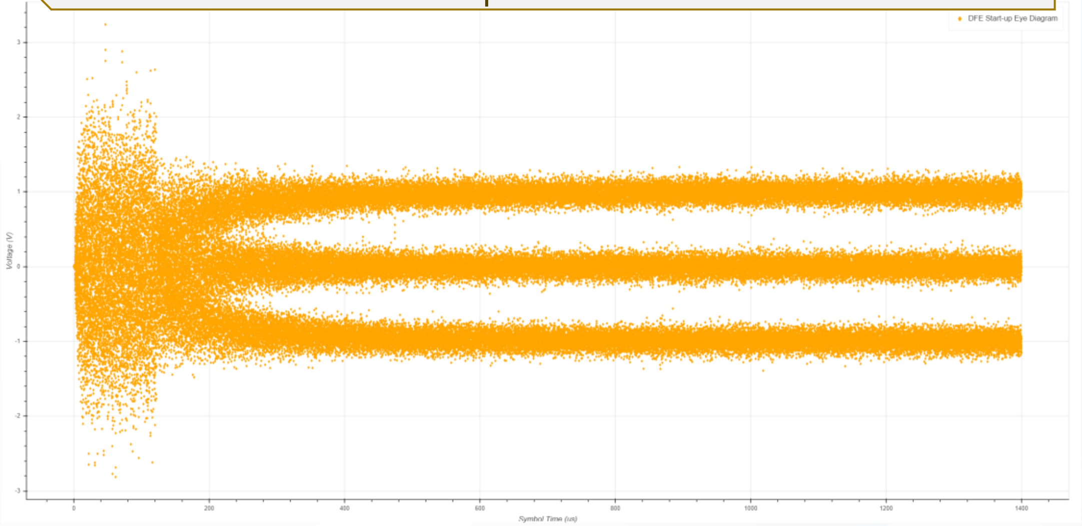


Insertion Loss 500m – 802.3dg Extended to 40 MHz

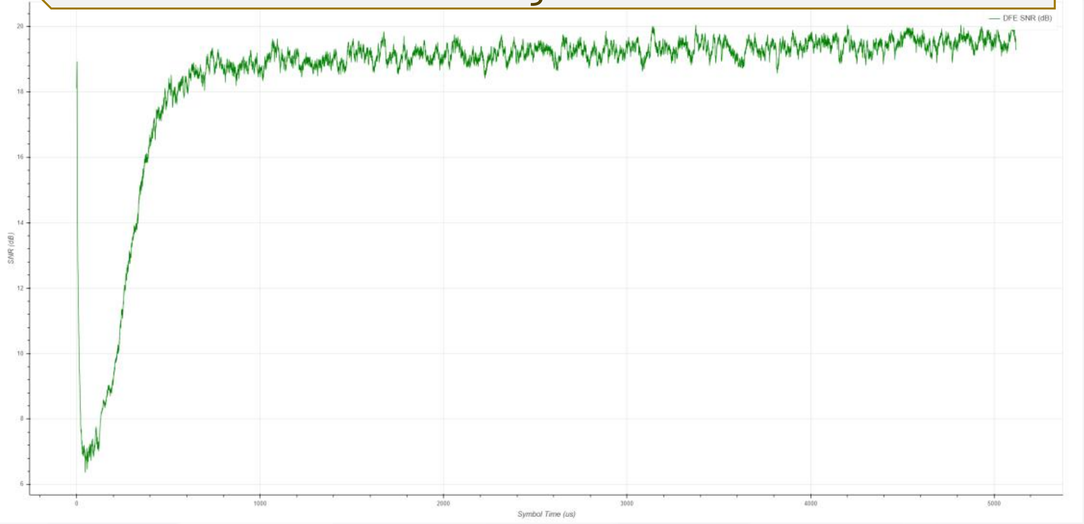


Example 100BASE-T1L 400m with 5 mV rms Noise

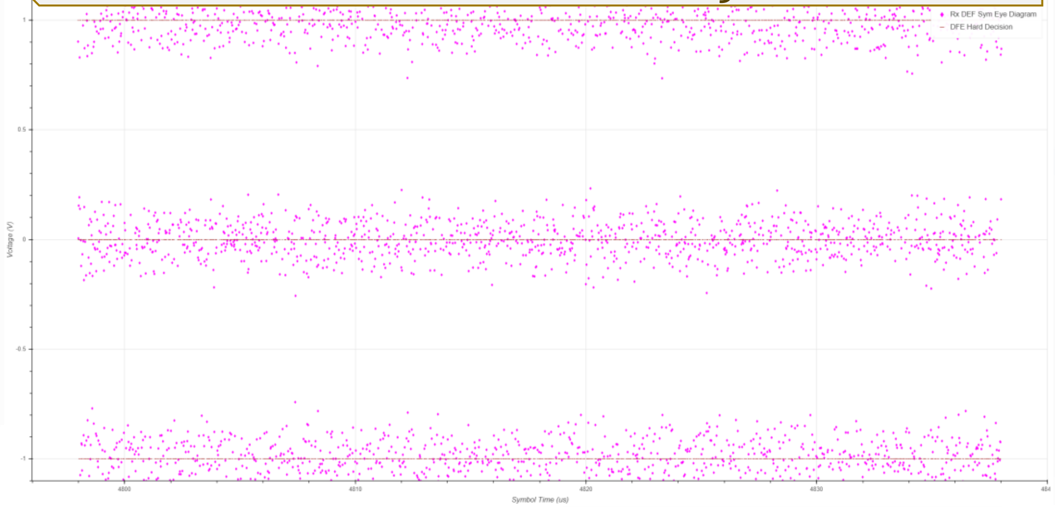
Start-up Data Pattern



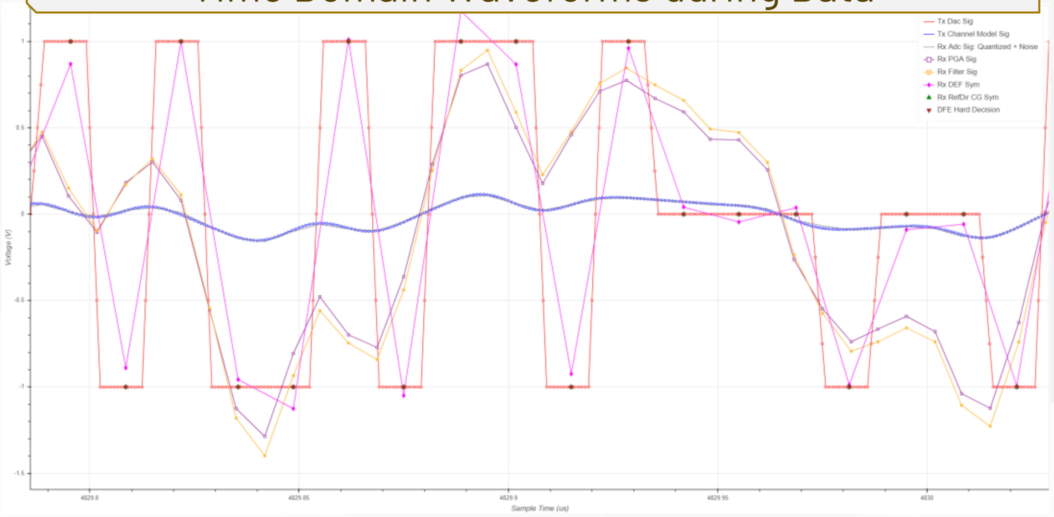
SNR Convergence 0 – 5 ms



PAM-3 Data Pattern During Data



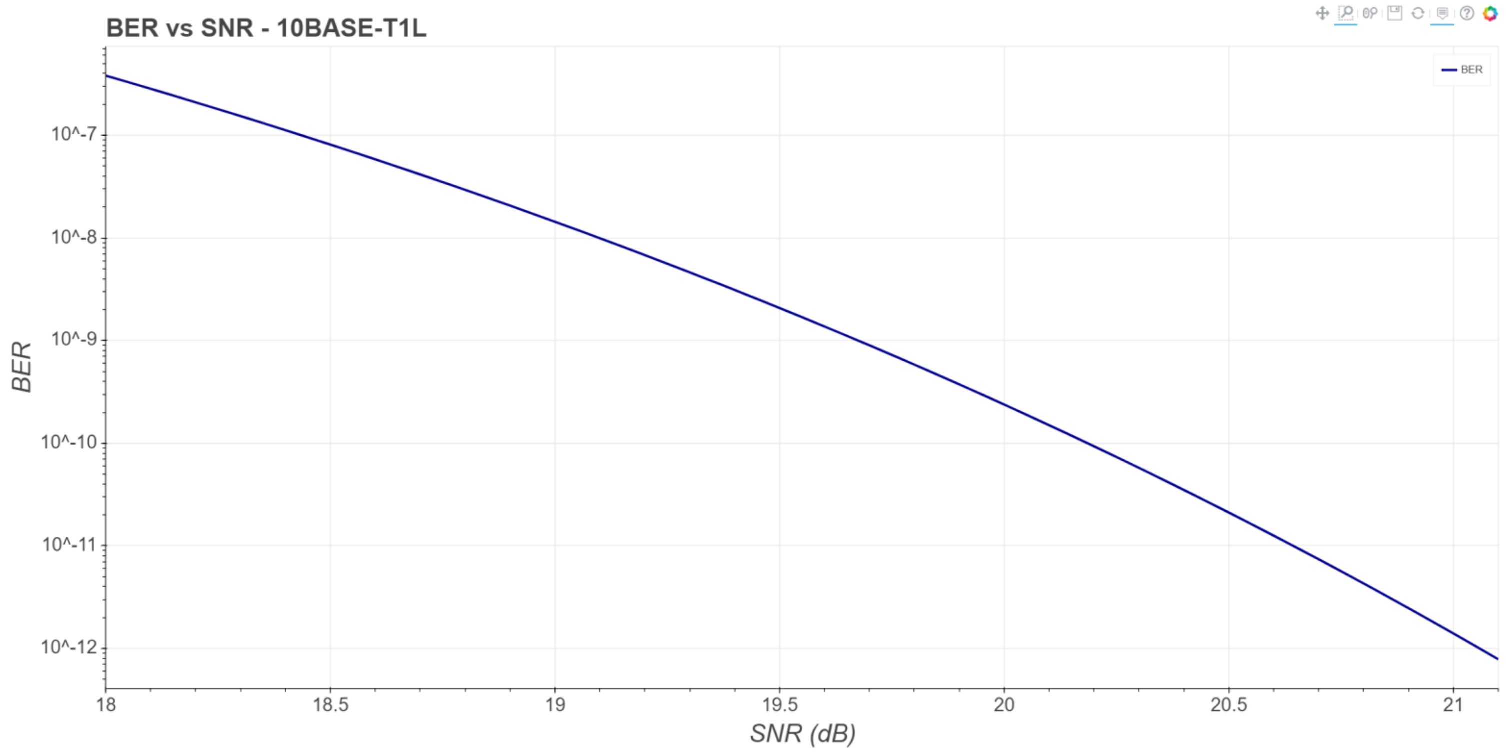
Time Domain Waveforms during Data



SNR verses BER or Packet Error Rate

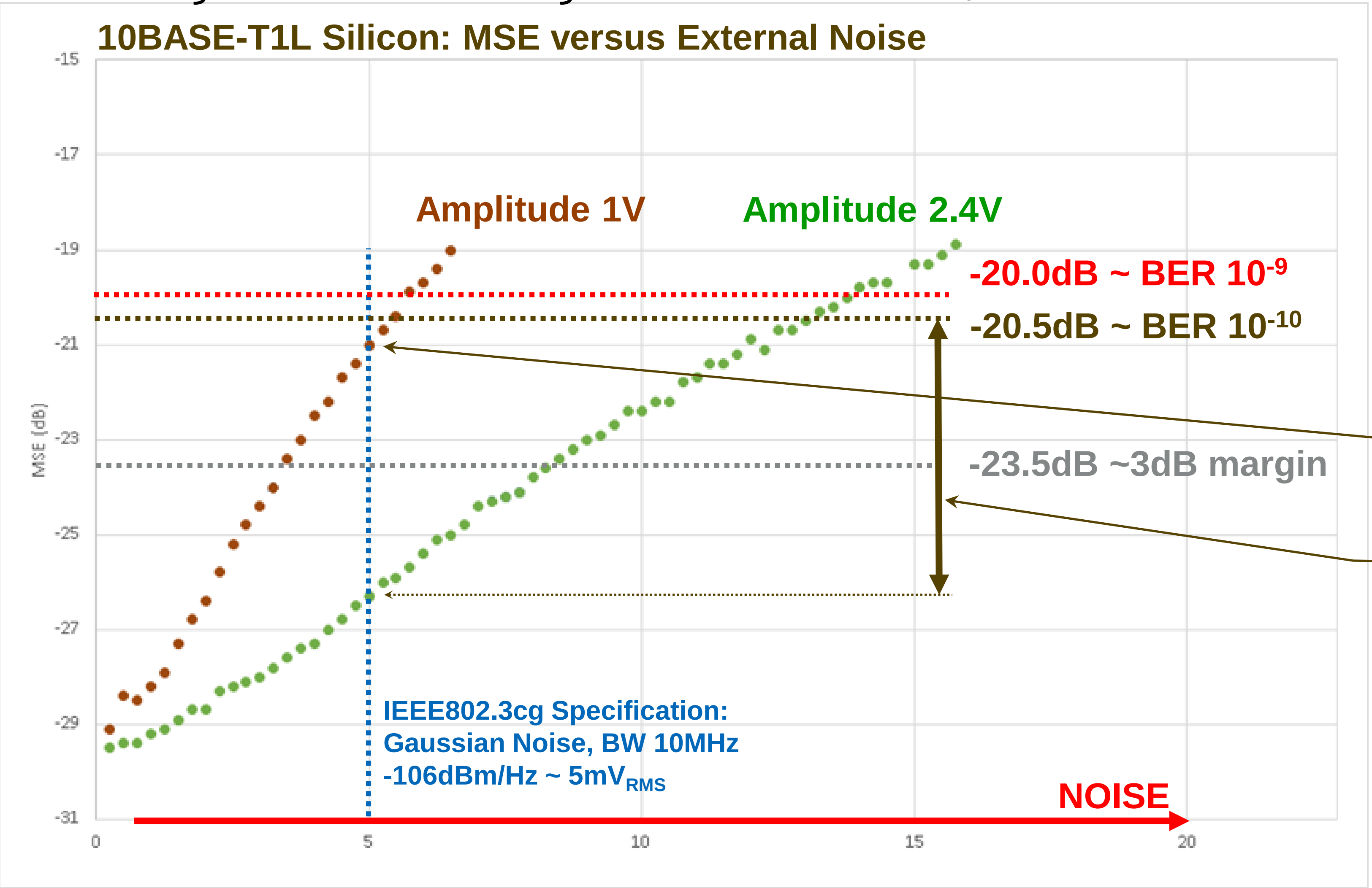
- The 802.3cg standard mandates BER ≤ 10^{-9}
  - 10^{-9} ~ 1 error in 100 seconds
  - 10^{-14} ~ 1 error in 3 months
  - All this is theoretical, based on Gaussian noise
- Require SNR better than ~ 19.7 dB

- Need a few dB margin to theoretical limit
  - Ensure the system robust with the worst-case cables
- 802.3dg standard mandates BER ≤ 10^{-10}
  - This is in line with most other Ethernet standards and is necessary for 100M speeds
- Requires SNR of about 20.2 dB



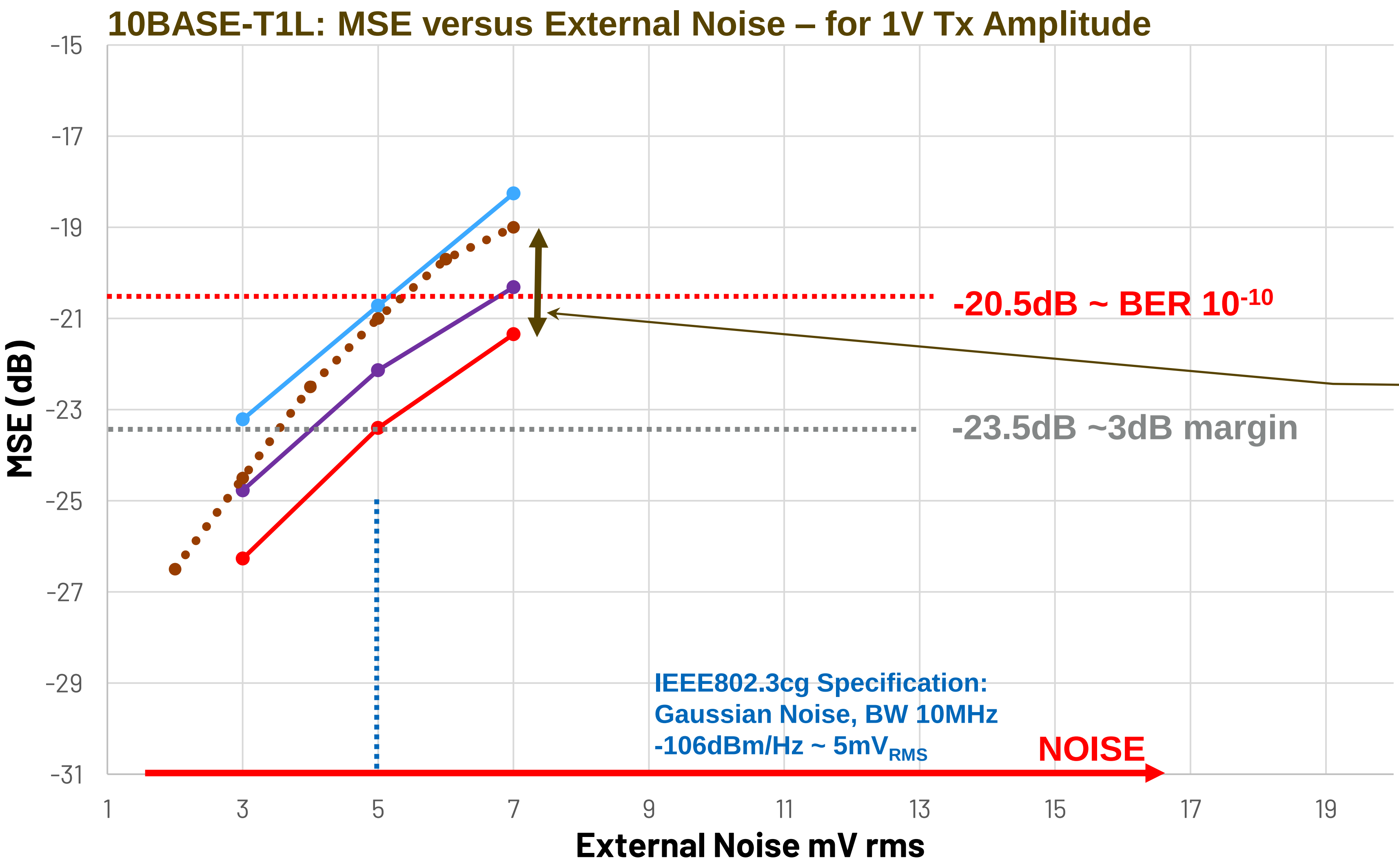
10BASE-T1L Silicon Measurements on 1000m Cable

- **1000m** cables combined to be close to specification limit (IEEE802.3cg 146.7.1.1.1 Link Segment Insertion Loss)



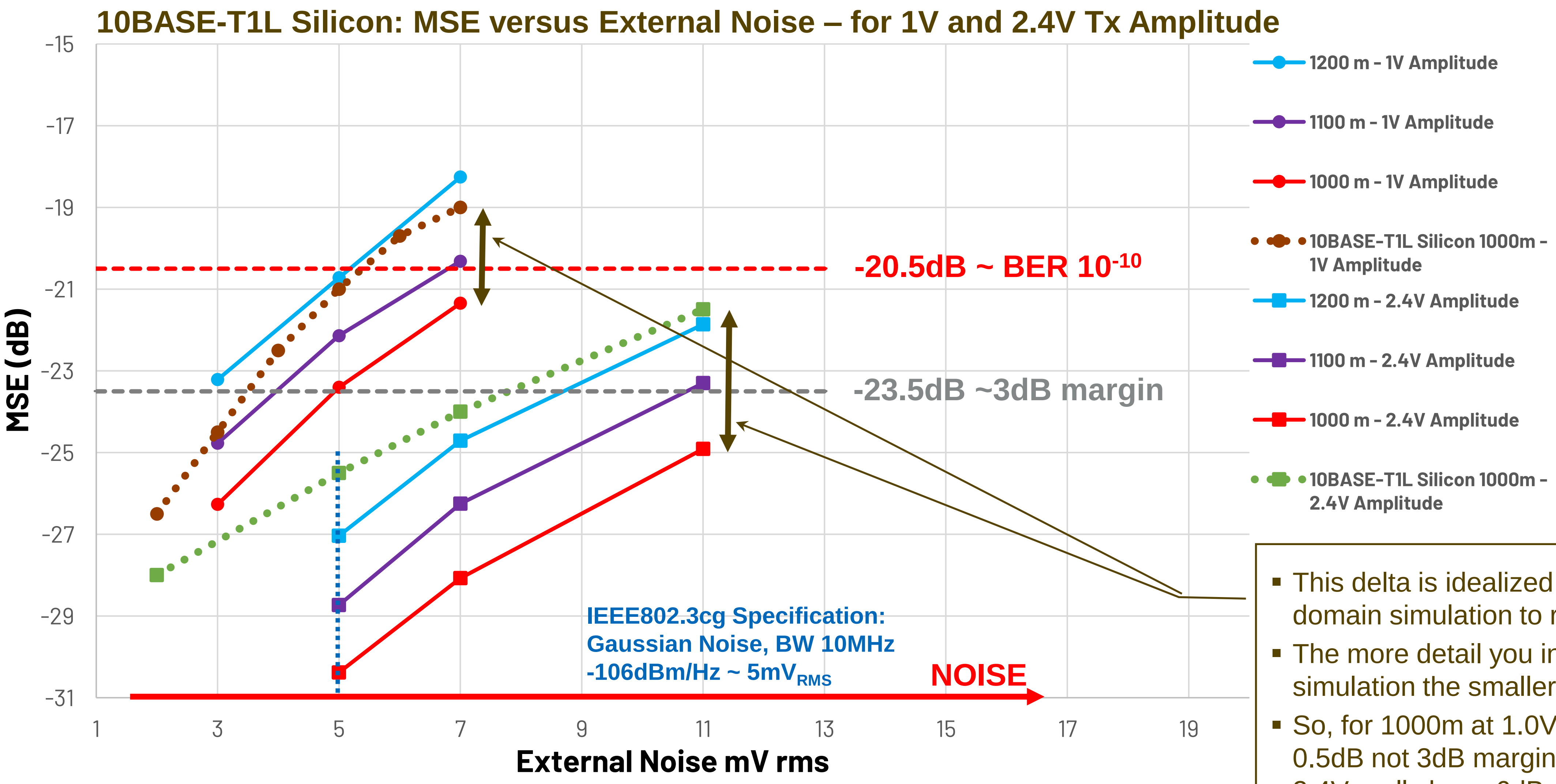
- For 1000m and 5 mV noise with 1.0V transmit only have ~ 0.5dB SNR margin
- But transmitting at 2.4V have almost 6dB of margin

Example 10BASE-T1L Time Domain Results



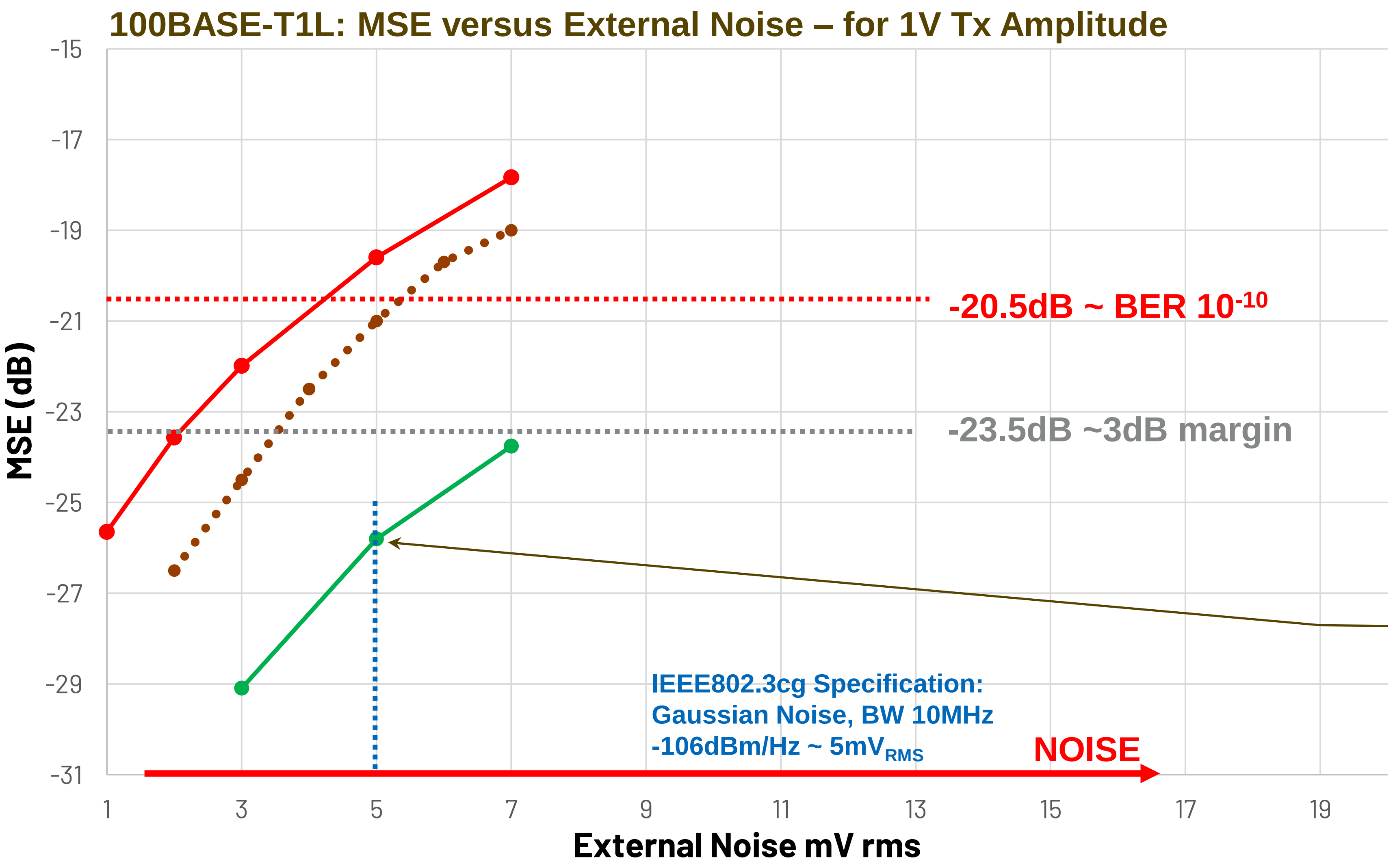
- This delta is idealized time domain simulation to real silicon
- The more detail you include in the simulation the smaller the delta

Example 10BASE-T1L Time Domain Results



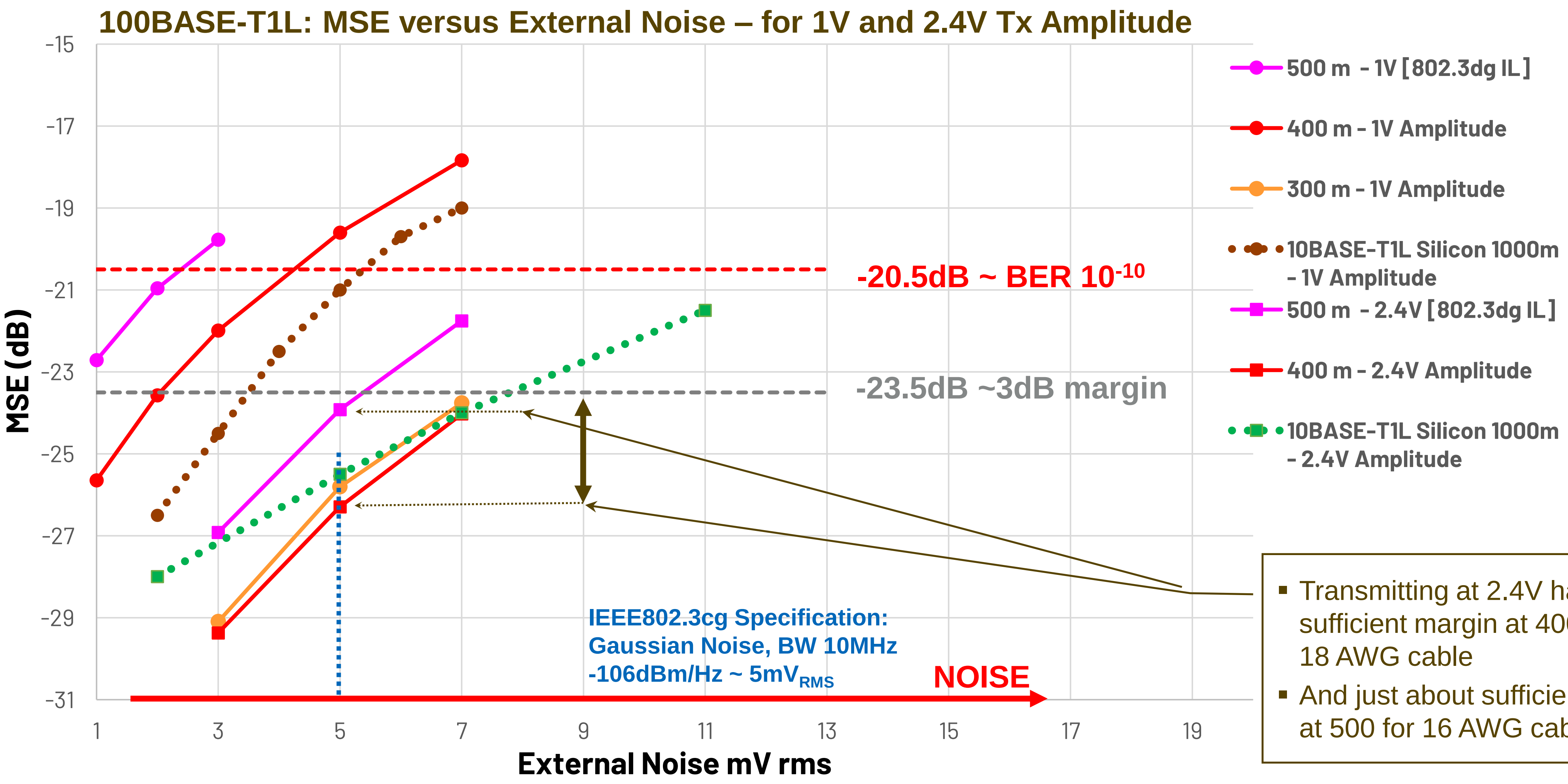
- This delta is idealized time domain simulation to real silicon
- The more detail you include in the simulation the smaller the delta
- So, for 1000m at 1.0V really have 0.5dB not 3dB margin; and at 2.4V really have 6dB not 10dB

Example 100BASE-T1L Time Domain Results



- Transmitting at 1.0V has good margin at 300 m for 18 AWG cable (802.3cg IL model)

Example 100BASE-T1L Time Domain Results



- Transmitting at 2.4V has sufficient margin at 400 m for 18 AWG cable
- And just about sufficient margin at 500 for 16 AWG cable

Time Domain Simulation Test Bench Conditions

- To compare modulations schemes we need to agree test conditions
- Proposed test conditions that we should use to evaluate time domain simulation results
  - The two most important factors that limit reach and SNR margin (for an optimum PHY design) are the **Insertion Loss** of the cable and the **External Noise** to be tolerated
    - We have an adopted Link Segment as of 9/7/23 (link_segment_090723) – so include this
    - There is also value in showing comparison with 802.3cg IL model
- Insertion Loss models

802.3dg IL	$IL(f) \leq \left(5.42 \times \sqrt{f} + 0.044 \times f + \frac{1.76}{\sqrt{f}}\right) + 5 \times 0.02 \times \sqrt{f} \quad \text{(dB)}$
802.3cg IL	$IL(f) \leq 10\left(1.23 \times \sqrt{f} + 0.01 \times f + \frac{0.2}{\sqrt{f}}\right) + 10 \times 0.02 \times \sqrt{f} \quad \text{(dB)}$

- Extrapolate Noise Model to wider bandwidth for 100BASE-T1L
  - Clause 146.5.5.3 of 802.3cg defines the receiver's tolerance to alien crosstalk noise.
  - Noise with a Gaussian distribution, bandwidth of 10 MHz, and magnitude of –106 dBm/Hz

Some Take Aways from Initial Results

- First – is until we run on an agreed set of test conditions, in particular an agreed noise model we have to be very careful about any inference from results
  - Even then it is an agreed noise model and cable model – not real noise
  - However, experience tells us that we can and have made good architectural choices based on appropriately designed simulations
- The early results appear to indicate that we can achieve 500m reach using PAM-3 modulation – which is a very useful data point
  - A straw man result of 10 x 10BASE-T1L was always going to be a useful reference point
  - However, we can't infer anything until we compare that reference point to other modulation points
- PAM-3, PAM-4 and PAM-5 are all good options to consider
  - There are important trade-offs between noise, level spacing and coding gain
  - In particular, impulse noise like EFT is likely to benefit from greater level spacing
- Block Coding or Convolution Coding can be combined with a modulation scheme to provide coding gain

100BASE-T1L Transmit Voltage Levels

- 802.3cg supported two transmit voltage levels
  - 2.4V pk-pk for longer reach
  - 1.0V pk-pk for Intrinsically Safe applications (which are shorter reach)
- A larger transmit voltage is a clear advantage for alien noise, e.g. EFT
  - At 10M speeds its relatively easy to generate the higher transmit voltage
  - 2.4V pk-pk provides a 7.6 dB advantage over 1.0V pk-pk
    - In 10BASE-T1L this is at the cost of higher power dissipation (about 2 x) and a higher supply voltage (3.3V)
- In 100BASE-T1L transmitting at 2.4V at a higher symbol rate will also be at the cost of complexity and higher emissions
  - 100BASE-TX, 1000BASE-T, 10GBASE-T all support a 2.0V pk-pk transmit voltage
  - So it is known and understood how to transmit at this voltage level and speed
- Consideration should be given to the noise margin at 2.0V verses 2.4V

Key PHY Questions Still to Consider

- A time domain simulation will provide more accurate results for reach verses SNR margin for different modulation schemes
  - Need to analyse these to decide on the trade-offs
- What transmit voltage levels should be supported
- Do we include FEC
  - What latency is acceptable to achieve long reach and greater immunity to noise

Summary

- We have made progress in the task force on the first level of analysis on the PHY line coding and channel specification and have a reasonable bound on good options to be considered
- Example time domain simulation results have compared 10BASE-T1L and 100BASE-T1L under similar conditions
- With agreed test bench conditions time domain simulations will allow us to compare different modulation schemes for reach verses SNR margin
- This will give us the data that the task force requires to analyse the trade-offs of the different approaches

Questions ?