The bridge to possible

Ethernet MII Interfaces

Refinement of Previous Proposals

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Motivation

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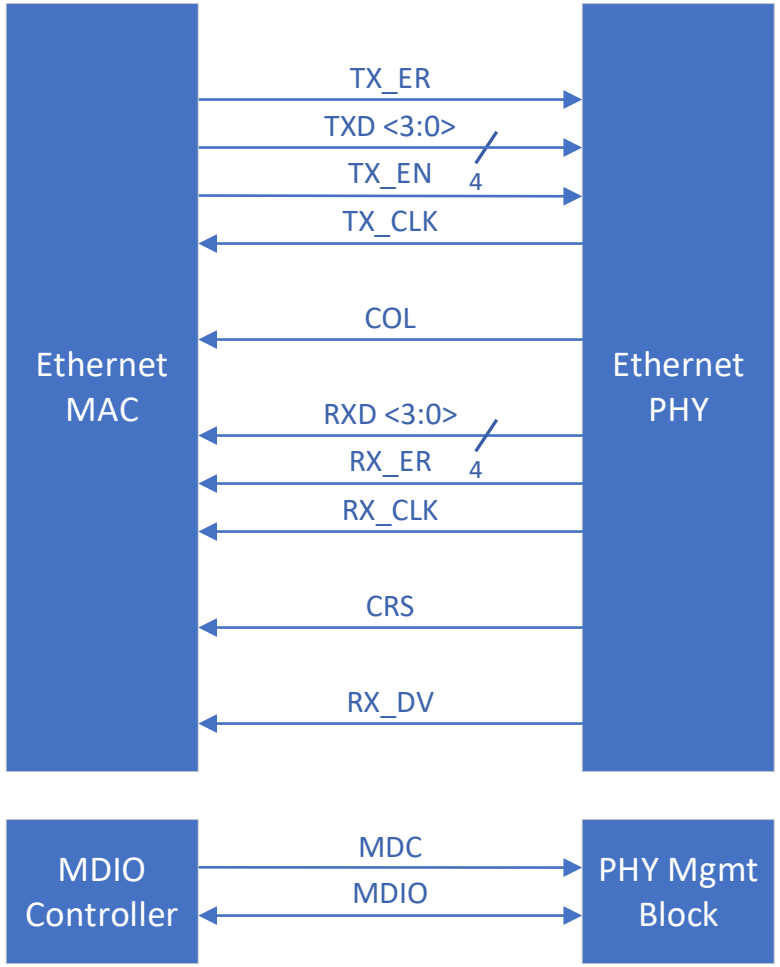
- 802.3dg wants a new MII
  - Needs to provide a modern single-port solution for 100 mbit/s data rates
  - Also need to solve multi-port applications to enable switch density
- 802.3da also wants a new MII
  - PLCA over MII presents challenges
- We need consensus on the right place to do this work

Quick Review of Past MIIs

IEEE 802.3
Clause 22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

MII Score Card	
Max Data Rate	100 Mbit/s
Signal Count	16 Data + 2 Mgmt
Bus Max Clock Rate	25 MHz
Clock Scheme	PHY Synchronous
Command Space	4-bit
Commands Assigned	Tx - 4/16, Rx - 5/16
PLCA Support	Yes, Beacon and Commit



MII Commands

- Cause Transmission or Indicate Reception of something other than valid data bytes on the wire
- Uses TX_EN / TX_ER / RX_En / RX_ER to create address space
- Currently Defined in 802.3 Clause 22
  - Assert LPI
  - PLCA Beacon Request / Indication
  - PLCA Commit Request / Indication
  - False Carrier Indication

Table 22–1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Reserved
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON request
0	1	0011	PLCA COMMIT request
0	1	0100 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

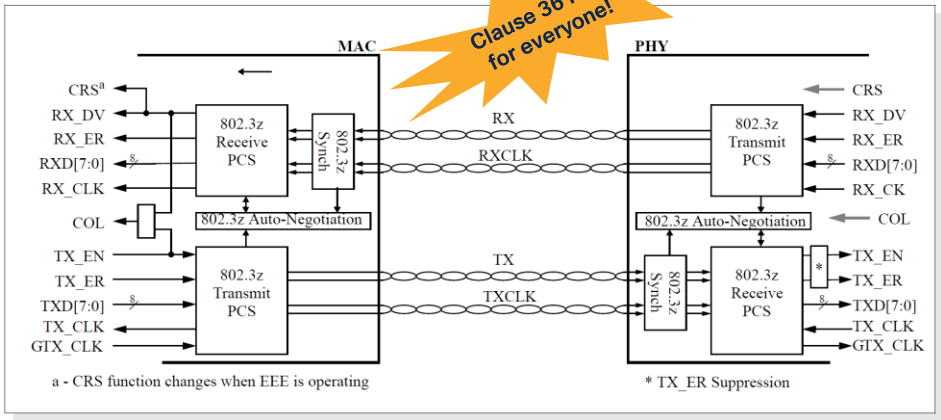
Table 22–2—Permissible encoding of RXD<3:0>, RX_ER, and RX_DV

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON indication
0	1	0011	PLCA COMMIT indication
0	1	0100 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

Cisco Specification
Serial-GMII (aka SGMII)

MII Score Card	
Max Data Rate	1000 Mbit/s
Signal Count	4/port + 2 Mgmt
SerDes Max Rate	1.25 Gb/s
Clock Scheme	SerDes or Source Sync
Command Space	Large – Ordered Sets
Commands Assigned	8 Non-Idle Sets Defined
PLCA Support	No

System Diagrams (SGMII Spec)



PCS Scheme (Clause 36)

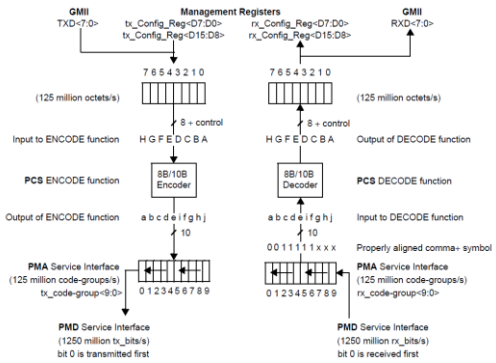


Figure 36–3—PCS reference diagram

Commands (Clause 36)

Table 36–3—Defined ordered sets

Code	Ordered Set	Number of Code-Groups	Encoding
/C/	**Configuration**		Alternating /C1/ and /C2/
/C1/	Configuration 1	4	/K28.5/D21.5/Config_Reg[a]
/C2/	Configuration 2	4	/K28.5/D2.2/Config_Reg[a]
/I/	**IDLE**		Correcting /I1/, Preserving /I2/
/I1/	IDLE 1	2	/K28.5/D5.6/
/I2/	IDLE 2	2	/K28.5/D16.2/
	Encapsulation		
/R/	Carrier_Extend	1	/K23.7/
/S/	Start_of_Packet	1	/K27.7/
/T/	End_of_Packet	1	/K29.7/
/V/	Error_Propagation	1	/K30.7/
/LI/	**LPI**		Correcting /LI1/, Preserving /LI2/
/LI1/	LPI 1	2	/K28.5/D6.5/
/LI2/	LPI 2	2	/K28.5/D26.4/

[a]Two data code-groups representing the Config_Reg value.

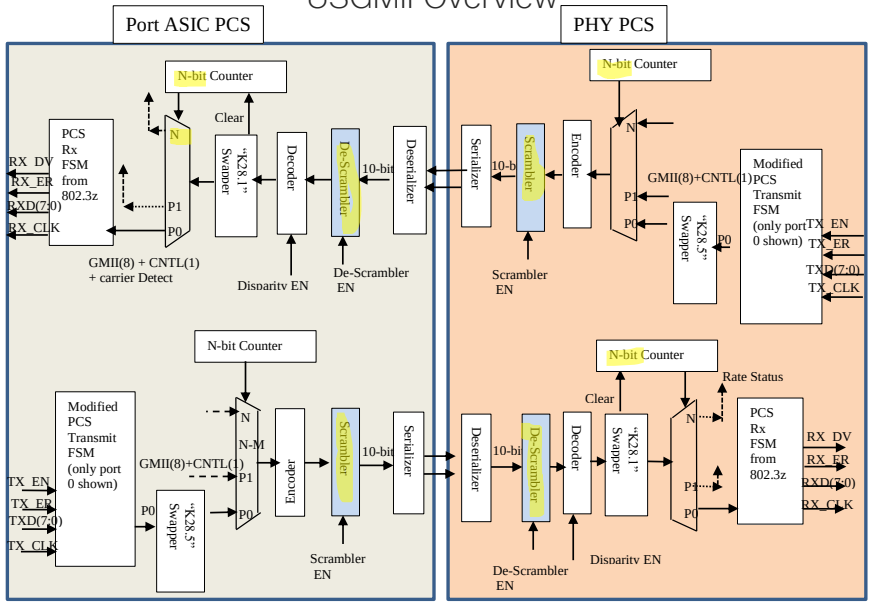
One to Rule Them All!

We're tired of doing these!

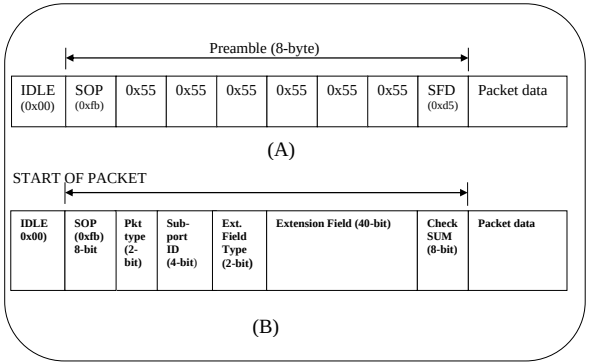
Cisco Specification
Universal Serial GMII (aka USGMII)

MII Score Card	
Max Data Rate	1000 Mbit/s, with 8, 4, and 1 Port Modes
Signal Count	4/Octal PHY + 2 Mgmt
SerDes Max Rate	10.0, 5.0, 1.25 Gb/s
Clock Scheme	SerDes
Command Space	Large – Ordered Sets Packet Control Header
Commands Assigned	K28.1 Reserved 8 Non-Idle Sets Defined PCH Packet Types
PLCA Support	No

USGMII Overview



Packet Control Header



PCH Packet Types

00: Ethernet Packet with PCH
01: Ethernet packet, without PCH (packet information)
10: Idle Packet – Contains status data for a port – no packet data
11: Preemption Frame, aka Interspersing Express Traffic (IET) frame

In-Band PTP Timestamps via Extension Field

Next-Gen MII
A Refined Proposal

Issue 1 – PLCA RS

- In theory, the Reconciliation Sublayer (RS) controls the PHY's PLCA-related actions from the host side of the MII
- In practice, backwards compatibility with non-PLCA MCUs in the market has driven PLCA into the PHY
- The success of PLCA-aware PHYs diminishes the market demand for PLCA signaling across the MII
- Standardized registers to mange PLCA-aware PHYs could be of value as part of the 802.3 standard

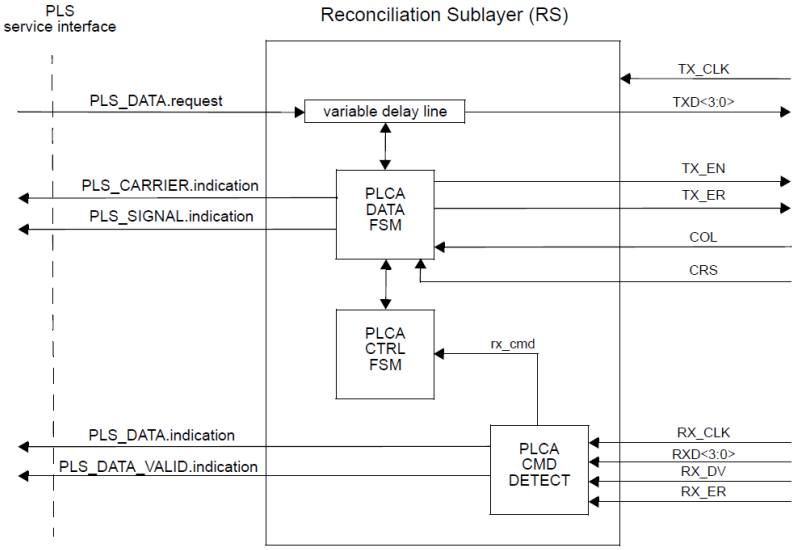
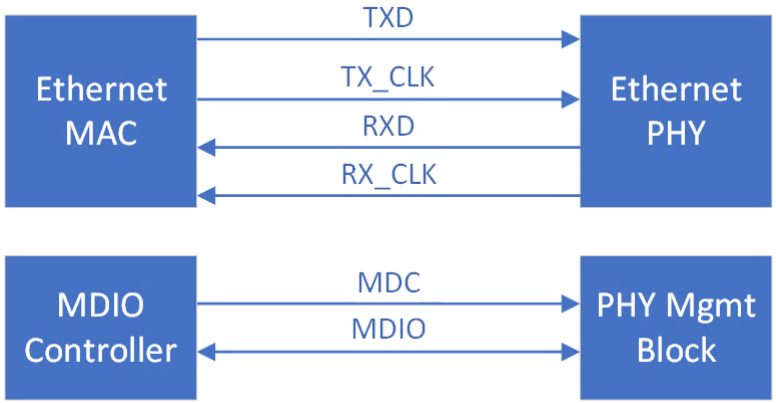


Figure 148–2—PLCA functions within the Reconciliation Sublayer (RS)

Issue 2 – Single Port Interfaces

- Single Port Reduced Pin Interface
  - Competes with Open Alliance
    - SPI MAC/PHY Serial Interface
    - Three-Pin PMD Interface
  - More useful in 802.3dg than 802.3da due to ease of integration of a 10Base-T1S PHY in an MCU with external PMD
  - Could be useful for 4-pair 10/100 PHYs as well

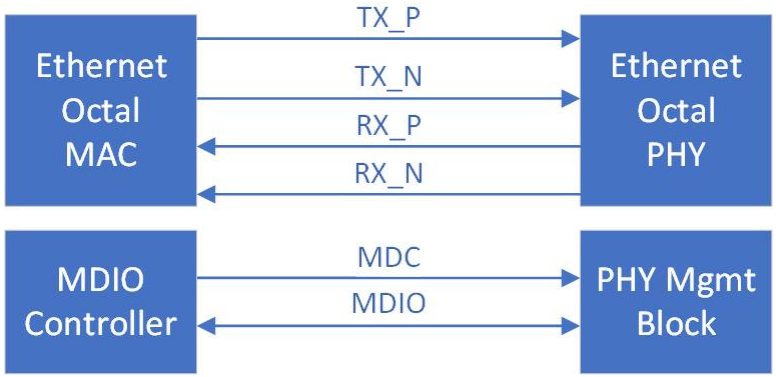
Single-Port Configuration



Issue 3 – Multi-Port Interfaces

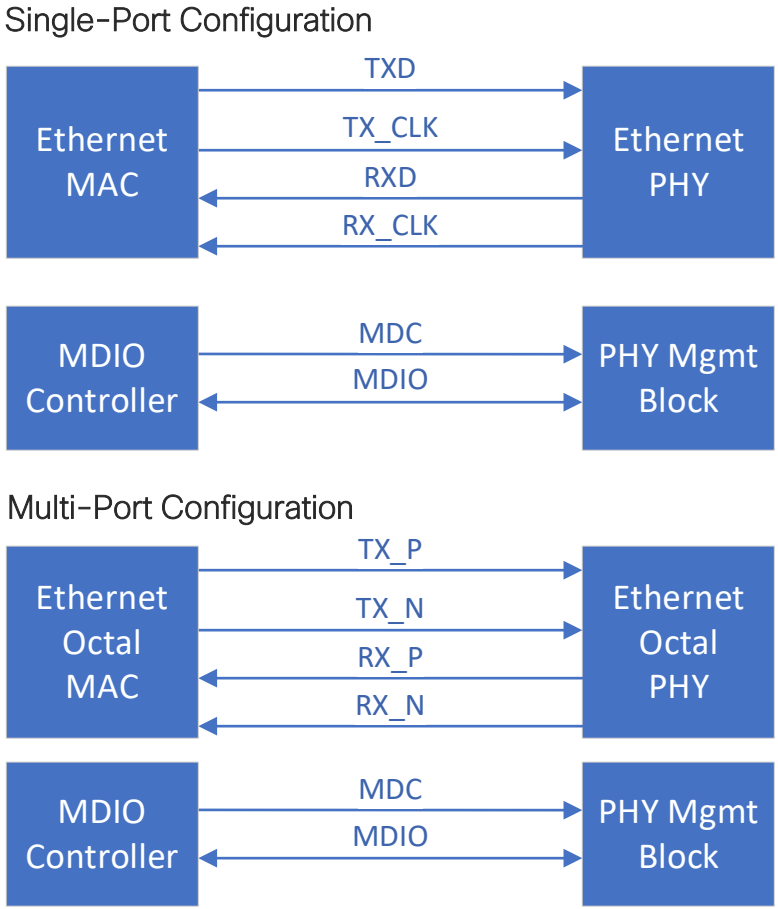
- Features to Consider
  - Slow SerDes / No SerDes
  - Variable Mux Ratio
    - 1-8 Ports / Interface
  - Embedded MDIO
  - Ordered Sets for Control
    - PLCA, LPI, Faults, Collisions, etc.
  - PTP Timestamping
  - Collision Notification
  - Preemption

Multi-Port Configuration



Issue 4 – One Solution or Two?

- Should we have a single logical solution that scales from single to multi-port?
- Should we allow multiple electrical interfaces to enable hardware optimization?
- See following slides for an example of a single logical solution…



Supported Configurations Proposal A

Number of Data ports	Data Speed per port	Number of Parts	Maximum MII Data Rate (Mbps)	Comment
1-port	10M	1	12.5	One Port, 10 Mbit Only
10M				10 Mbps Data Payload Before 8b/10b Overhead
(USMII-Lite)				
1-port	10/100M	1	125	One Port
10/100M				100 Mbps Data Payload Before 8b/10b Overhead
(USMII)				
4-port	10/100M	4	500	Maximum of 4 ports
10/100M				400 Mbps Data Payload Before 8b/10b Overhead
(Q-USMII)				
8-port	10/100M	8	1000	Maximum of 8 ports
10/100M				800 Mbps Data Payload Before 8b/10b Overhead
(O-USMII)				

No In-Band Control Bandwidth Reservation

Supported Configurations Proposal B

Number of Data ports	Data Speed per port	Number of Parts	Maximum MII Data Rate (Mbps)	Comment
1-port	10M	1	15.625	One Port, 10 Mbit Only
10M				10 Mbps Data Payload Before 8b/10b Overhead
(USMII-Lite)				2.5 Mbps In-Band Control Bandwidth Reserved
1-port	10/100M	1	156.25	One Port
10/100M				100 Mbps Data Payload Before 8b/10b Overhead
(USMII)				25 Mbps In-Band Control Bandwidth Reserved
4-port	10/100M	4	625	Maximum of 4 ports
10/100M				400 Mbps Data Payload Before 8b/10b Overhead
(Q-USMII)				100 Mbps In-Band Control Bandwidth Reserved
8-port	10/100M	8	1250	Maximum of 8 ports
10/100M				800 Mbps Data Payload Before 8b/10b Overhead
(O-USMII)				200 Mbps In-Band Control Bandwidth Reserved

Includes In-Band Control Bandwidth Reservation

Discussion and Straw Polls

Feature Requirement Straw Poll Summary

Features	Support in Single-Port?	Support in Multi-Port?
Control Bandwidth Reservation	?	?
Embedded MDIO	?	?
PTP Timestamping	?	?
Frame Preemption (802.1Q IET)	?	?
Energy Efficient Ethernet (LPI)	?	?
Four-Pair 10/100 PHY Compatibility	?	?
Half-Duplex Operation (COL)	?	?
Half-Duplex Late Collision Frame Correlation	?	?

Options: Mandatory Feature, Optional Feature, Omit Feature

Straw Poll Question Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation

Control Bandwidth Reservation

Should we allocate reserved bandwidth for guaranteed delivery of control messages in the MII data stream?

Options:

Yes, Mandatory Feature
Yes, Optional Feature
No, Omit Feature

Straw Poll Question Detailed Description

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Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
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Four-Pair 10/100 PHY Compatibility
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Half-Duplex Late Collision Frame Correlation

Embedded MDIO

Should we support embedding MDIO transactions in the MII data stream?

Options:

Yes, Mandatory Feature
Yes, Optional Feature
No, Omit Feature

Straw Poll Question Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation

PTP Timestamping

Should we support communicating PTP timestamps in the MII data stream?

Options:

Yes, Mandatory Feature
Yes, Optional Feature
No, Omit Feature

Straw Poll Question Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
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Frame Preemption (802.1Q IET)

Should we support communicating information necessary to manage frame preemption in the MII data stream?

Options:

Yes, Mandatory Feature
Yes, Optional Feature
No, Omit Feature

Straw Poll Question Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
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Energy Efficient Ethernet (LPI)

Should we support communicating control data necessary to enable EEE in the MII data stream?

Options:

Yes, Mandatory Feature
Yes, Optional Feature
No, Omit Feature

Straw Poll Question Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation

Four-Pair 10/100 PHY Compatibility

Should we support communicating management information necessary to support legacy 10/100 four-pair PHYs in the MII data stream?

Options:

Yes, Mandatory Feature
Yes, Optional Feature
No, Omit Feature

Straw Poll Question Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
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Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation

Half-Duplex Operation (COL)

Should we support communicating status messages necessary to manage collisions in the MII data stream?

Options:

Yes, Mandatory Feature
Yes, Optional Feature
No, Omit Feature

Straw Poll Question Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation

Half-Duplex Late Collision Frame Correlation

Should we support correlating collisions with frames to improve systems with high latency MII schemes?

Options:

Yes, Mandatory Feature
Yes, Optional Feature
No, Omit Feature

Path Forward Decisions

- What's the right construct?
  - New MII (e.g. USGMII)
  - Extender Sublayer (e.g. XAUI)
- Where should this be done?
  - IEEE 802.3 New Project
  - IEEE 820.3dg
  - Industry Specification
- Can IEEE complete this in a timely manner so as to compete with other industry standards?

The bridge to possible