Further consideration on the new MII

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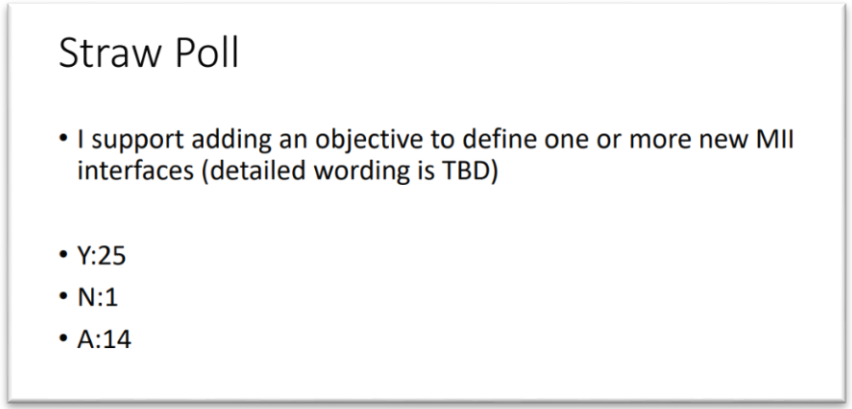
Introduction

- Reducing pin number brings many advantages (e.g. stronger CPU, easier PCB design, and higher-density interface etc.) to low-speed SPE.
- Existing solutions have one or several of the following problems:
  - slightly reduced pin number
  - non-MII interface
  - non-IEEE MII interface
  - bad signal integrity
  - high power consumption
  - high complexity
  - …



Source: Motions_01_07112023.pdf

- New MII with much less pin number while supporting the “new” IEEE features is attractive to low-speed SPE, and is welcomed by 802.3dg working group.
- This presentation discusses preliminary thoughts on the new MII supporting data, control and management information over the same channel.

Background

- Conventional MII has 18 pins in total, including 4 control pins, 8 data I/O pins, 2 pins for carrier/collision detection, 2 clock pins, and 2 management pins.
  - Combination of TX_EN, TX_ER, TXD<3:0> or RX_DV, RX_ER, RX_D<3:0> is used to represent different data and control information transmitted between MAC and PHY.
  - CRS and COL provides carrier and collision detection results for idle status and half-duplex communication.
  - SMI including MDC and MDIO is used for PHY management and configuration. The management interface of switch equipment with multiple PHY requires CPLD/MCU along with the logic/driver develop, leading to additional cost.

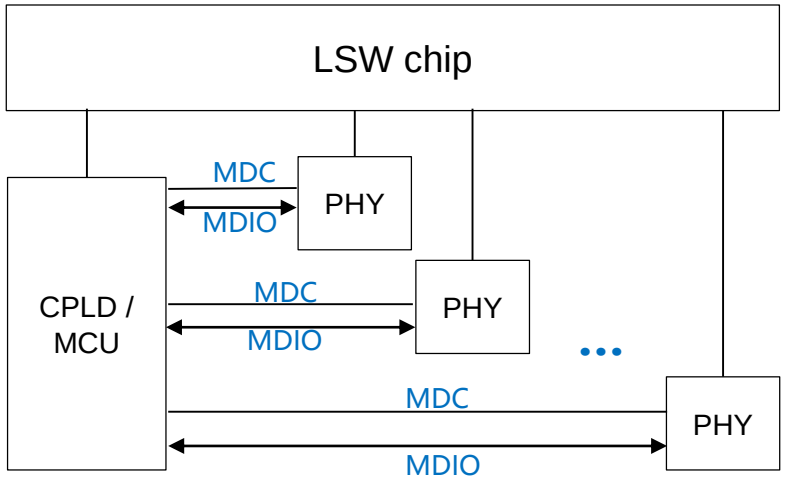
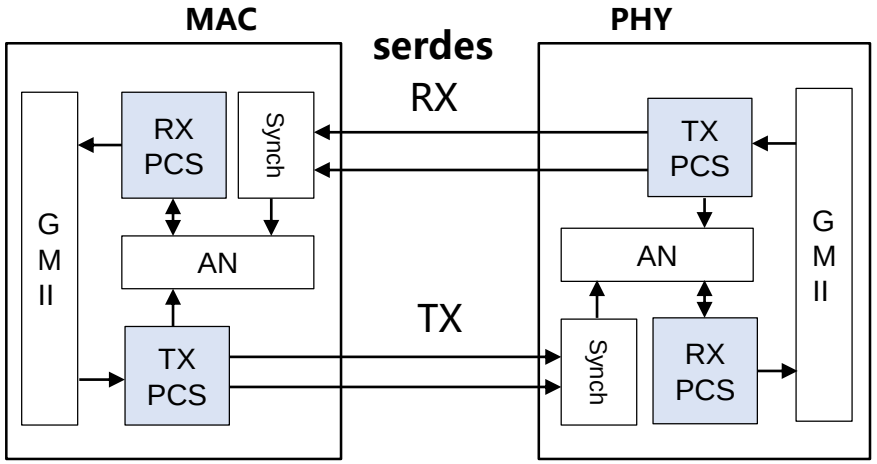


Table 22–1—Permissible encodings of TXD<3:0>, TX_EN, and TX_ER

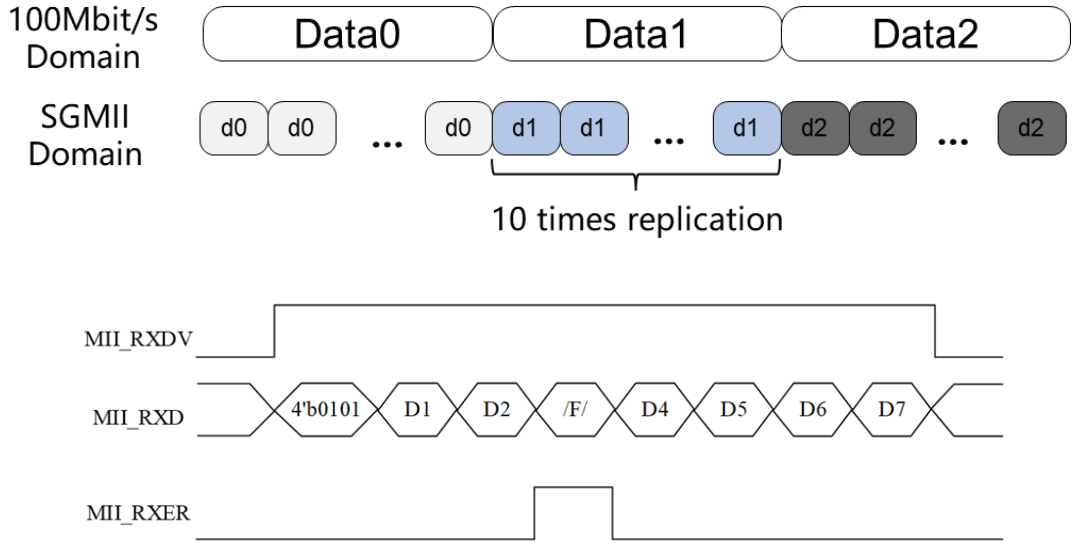
TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Reserved
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON request
0	1	0011	PLCA COMMIT request
0	1	0100 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

Considerations are needed for SGMII on low-speed SPE

- It is obvious that serial interface achieves the lowest number of pins. SGMII utilizes only 4 pins to transmit and receive serial differential signal, and supports low-speed 10M/100M PHY.
  - High power consumption presents challenge for its application to the end nodes in the field.
  - 8B/10B has not considered the transmit/receive error for odd TX_CLK periods with 4-bit width.
  - Separate management interface is also required.

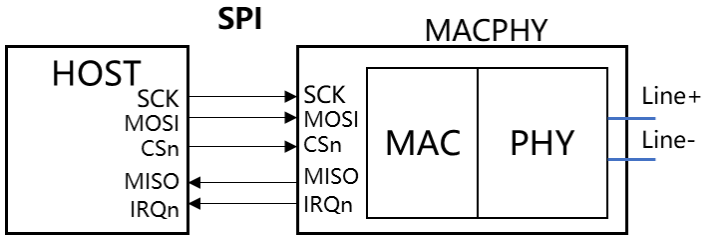


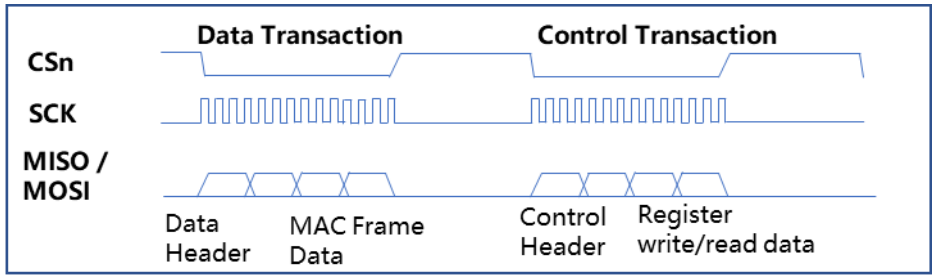
Block diagram of SGMII



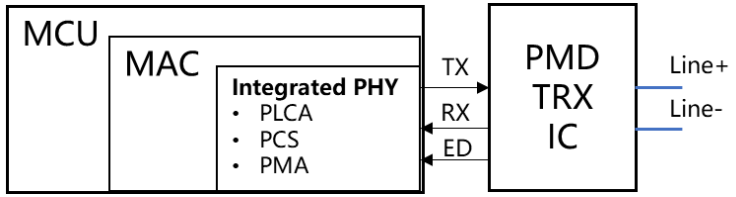
No dedicated management interface is feasible

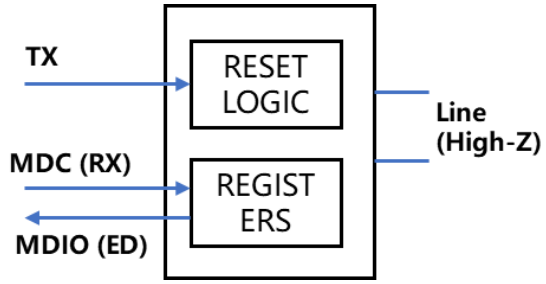
- **MACPHY SPI** supports both data and control transaction. Data transaction is used for Ethernet frame. Control transaction is actually utilized for register read/write. Control commands are employed by the SPI host to read and write registers within the MAC-PHY, similar to MDIO of 802.3.
- **PMD transceiver interface**: When the PMD transceiver is set to configuration mode, the RX pin functionalizes as the MDC input of the management interface and the ED pin becomes the bidirectional MDIO. The specification of the MII management interface complies with Clause 22.2.4.5 of 802.3.





Source: OPEN Alliance 10BASE-T1x MAC-PHY SPI



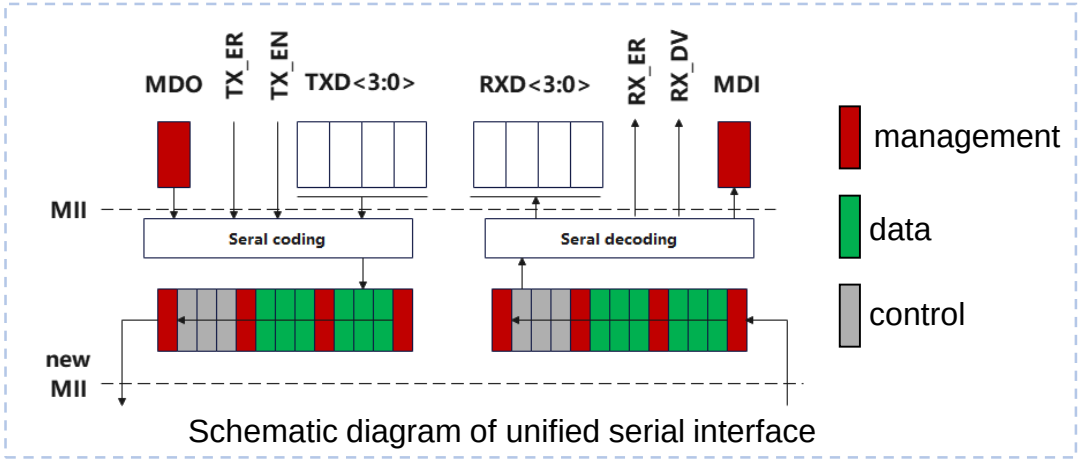


Transceiver function during configuration mode

Source: OPEN Alliance 10BASE-T1S PMD Transceiver Interface

Unified serial interface for data, control, and management

- A serial new MII supporting data, control, and management information over the same channel is appealing due to the minimum pin number and reduced cost.
  - It can be realized by sending the three different types of information at different time with either the same or different block length.
- Data and control over the same channel has already been realized with block coding (e.g. 4B/5B, 8B/10B, 64B/66B etc.). To adapt to the 4-bit TXD/RXD of the MII, the coding except 4B/5B needs modification.
  - 64B/65B and 64B/66B need to take different /S/ locations ($S_{1/2/3/5/6/7}$) into account. A possible solution can be extending the block type field definition.
  - 8B/10B needs to solve the 4-bit error appeared in either the first or the second nibble of the 8-bit block.
- TX_CLK and RX_CLK can be recovered from the data path or the clock path. In terms of the former, the more transitions the coding provides, the CDR is easier. Practical implementation depends on the requirement of different applications (e.g. less pin for switch, less power and lower cost for the end nodes).



Schematic diagram of unified serial interface

Input Data	sync	Block Payload							
		type							
S0 D1 D2 D3/D4 D5 D6 D7	10	0x78	D1	D2	D3	D4	D5	D6	D7
C0 S1 D2 D3/D4 D5 D6 D7	10	0x7i1	C0	D2	D3	D4	D5	D6	D7
C0 C1 S2 D3/D4 D5 D6 D7	10	0x7i2	C0	C1	D3	D4	D5	D6	D7
C0 C1 C2 S3/D4 D5 D6 D7	10	0x7i3	C0	C1	C2	D4	D5	D6	D7
C0 C1 C2 C3/S4 D5 D6 D7	10	0x33	C0	C1	C2	C3	D5	D6	D7
C0 C1 C2 C3/C4 S5 D6 D7	10	0x3i5	C0	C1	C2	C3	C4	D6	D7
C0 C1 C2 C3/C4 C5 S6 D7	10	0x3i6	C0	C1	C2	C3	C4	C5	D7
C0 C1 C2 C3/C4 C5 C6 S7	10	0x3i7	C0	C1	C2	C3	C4	C5	C6

Unified serial interface for data, control, and management (Cont.)

- Generally, there are two methods to insert management information into the data/control channel.
- Option 1: Periodically inserting a marker to the hybrid transmission channel. Management information can be carried by allocated bits within or outside the marker.
  - Similar locking scheme as alignment marker in 100GBASE-R can be used.
  - The marker should be long enough to keep the mismatch probability low.
  - The inflated bandwidth requires dedicated mechanism for speed adaptation.
- Option 2: Coding.
  - Paired 4B/5B: the first 5-bit block obeys 4B/5B coding rule, while the following 5-bit block keeps the same code type (data or control) with 1 bit for management and 4 bit for data/control.
  - 8B/10B: Newly defined special code-group to denote the start of management information transmission.
  - 64B/65B+1: 64B/66B with one bit of the 2-bit synch header allocated for management.
  - ...

Conclusion

- Serial interface is the most efficient way to achieve less pins. Data, control, and management transaction over the same channel bypasses dedicated management channel, and brings cost and complexity reduction.
- Management information can be added to the hybrid data/control channel through marker insertion. However, it requires dedicated speed adaption and is a bit heavy for low-speed PHY, considering the locking and unlocking scheme.
- By contrast, modified coding is more attractive. Potential solutions include paired 4B/5B, 8B/10B, and “64B/65B+1”.

Thank you!