802.3dg PHY Baseline

Tingting Zhang, Dongcheng Pan, Yan Zhuang, Tong Mu

Huawei Technologies

Introduction

- Overall considerations on the PCS architecture, the associated function blocks (e.g. block coding, burst error correction requirement for FEC), and modulation formats are discussed in Tingting_3dg_02_13_09_2023.

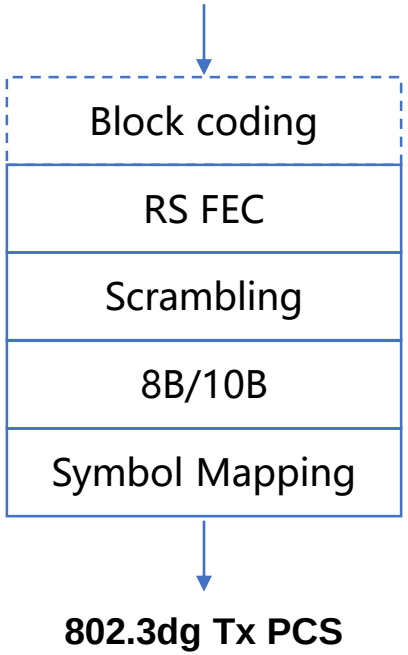
- This presentation gives suggestions on the modulation format and the PCS architecture.

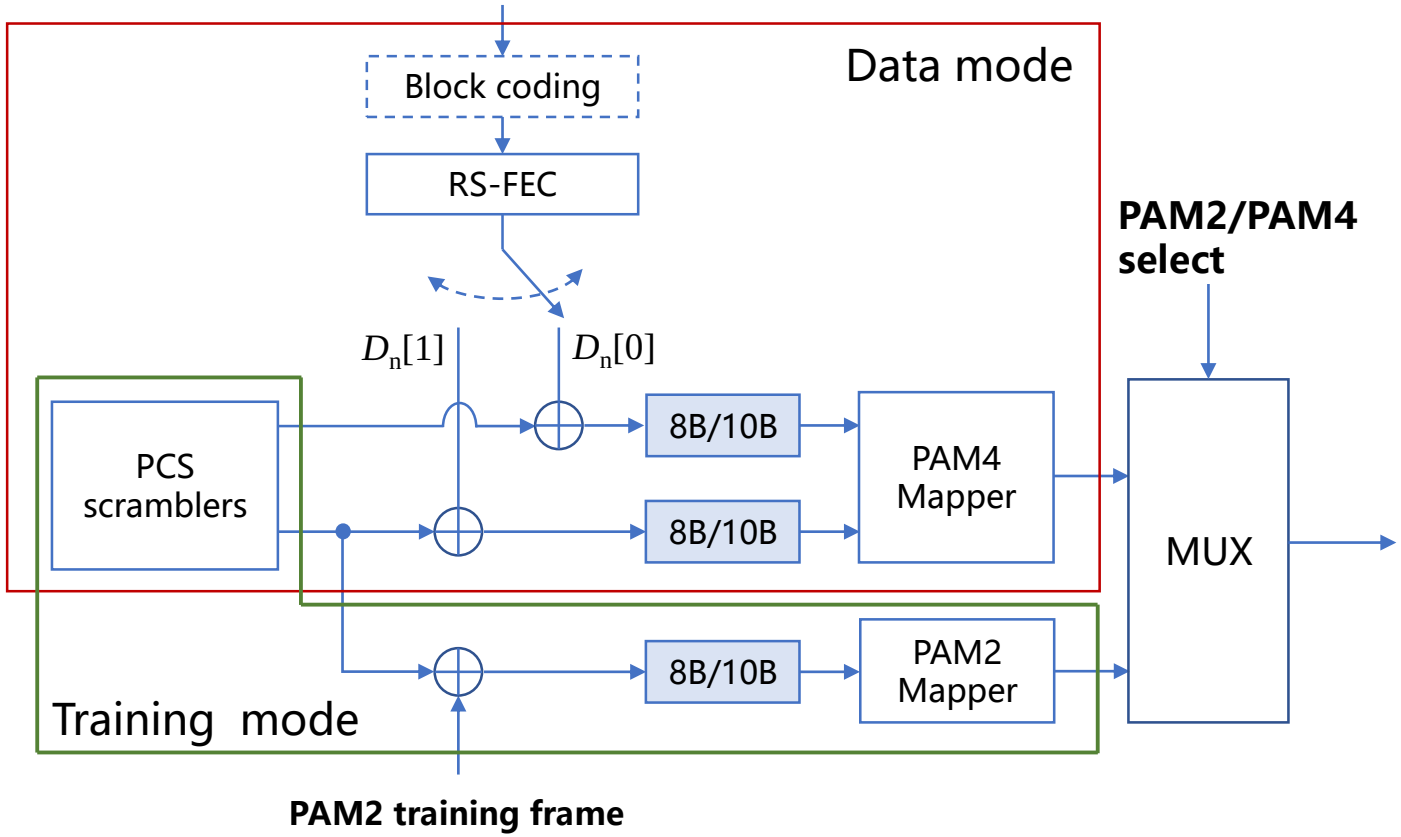
PAM candidates

- Many 802.3dg presentations (e.g. zimmerman_3dg_01a_03_15_2023, Murray_3dg_01a_07102023, Tingting_3dg_02_13_09_2023) have discussed and compared PAM3, PAM4, PAM5 in the aspects of SNR margin, disparity, bandwidth, PCS complexity etc..
- PAM3, PAM4, and PAM5 all achieve bounded disparity and similar SNR margin.
  - Due to the low coding efficiency, PAM3 results in large signal bandwidth, presenting challenges for LPF design. This also indicates more complicated FEC, as the high-frequency interference is not well suppressed.
  - 8B4T PAM5 achieves smallest signal bandwidth. To ensure fast convergence and bounded disparity during PMA training, block coded PAM2 is required, leading to the training PCS different from normal data mode.
  - PAM4 has been widely used in BASE-T1 standards. Coupled with 8B/10B coding, it also achieves bounded disparity and allows most PCS functions shared between data and training mode.
- With all these taken into account, we suggest 8B10B PAM4 for 802.3dg.

PCS architecture

- To ensure reliable 100Mbps transmission in the case of burst errors, FEC is required.
- Typical PCS architecture for automotive SPE is a good reference. To achieve bounded disparity for both training and data mode, 8B/10B is added before binary symbol mapper in the transmitter.
- PMA training selects PAM2 path, which uses the same clock as the normal data PAM4 path. FEC delimiting can be achieved by utilizing specifically designed PMA training frame with the equivalent length same as the FEC code word length in data mode.





FEC options

- 150ns burst error correction for single EFT pulse is sufficient if the interference is suppressed by more than 30dB.
- There are many FEC options with overhead within 10% in the case of no interleaving.
- The clock frequencies are achievable.

n	k	t	m	# OAM bits	# PCS blocks	Block coding	Frame (us)	Burst Error Protection (ns)	Symbol Rate (MBaud)	Overhead (%)	BERin @ BERout=1e-10	Net Coding Gain (dB)
96	90	3	8	5	11	64B/65B	5.632	176	68.18182 (25×30/11)	9.09	3.46E-5	3.80
104	98	3	8	4	12	64B/65B	6.144	177.2308	67.70833 (25×65/24)	8.33	3.26E-5	3.79
112	106	3	8	3	13	64B/65B	6.656	178.2857	67.30769 (25×35/13)	7.69	3.08E-5	3.78
120	114	3	8	2	14	64B/65B	7.168	179.2	66.96429 (25×75/28)	7.14	2.92E-5	3.77
128	122	3	8	1	15	64B/65B	7.68	180	66.66667 (25×8/3)	6.67	2.78E-5	3.75
77	71	3	8	1	7	80B/81B	4.48	174.5455	68.75 (25×11/4)	10	4.10E-5	3.81
87	81	3	8	0	8	80B/81B	5.12	176.5517	67.96875 (25×87/32)	8.75	3.73E-5	3.80
88	82	3	8	8	8	80B/81B	5.12	174.5455	68.75 (25×11/4)	10	3.70E-5	3.80
98	92	3	8	7	9	80B/81B	5.76	176.3265	68.05556 (25×49/18)	8.89	3.41E-5	3.79
108	102	3	8	6	10	80B/81B	6.4	177.7778	67.5 (25×27/10)	8	3.17E-5	3.78
120	112	4	8	5	11	80B/81B	7.04	234.6667	68.18182 (25×30/11)	9.09	7.99E-5	4.23

Conclusion

- Considering coding efficiency, SNR margin, disparity, PCS complexity, and the ecosystem, we suggest PAM4 for 802.3dg.
- PCS architecture for automotive SPE is a good reference for 802.3dg. To achieve bounded disparity for both training and data mode, 8B/10B can be added before binary symbol mapper in the transmitter.

Thank you!