Overall consideration on 802.3dg PHY

Tingting Zhang, Sen Zhang, Yan Zhuang, Tong Mu

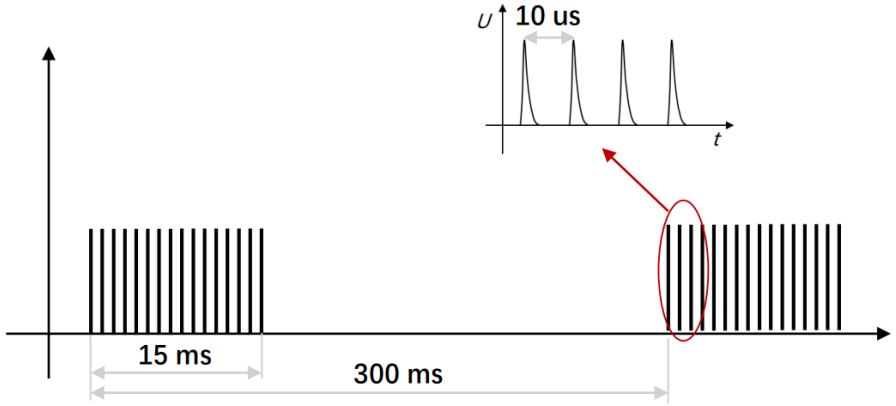
Huawei Technologies

Introduction

- This presentation discusses the EFT and ringing impact on the modulation format and burst error correction requirement for FEC. Overall considerations on the PCS architecture, the associated function blocks, and modulation formats are also presented.

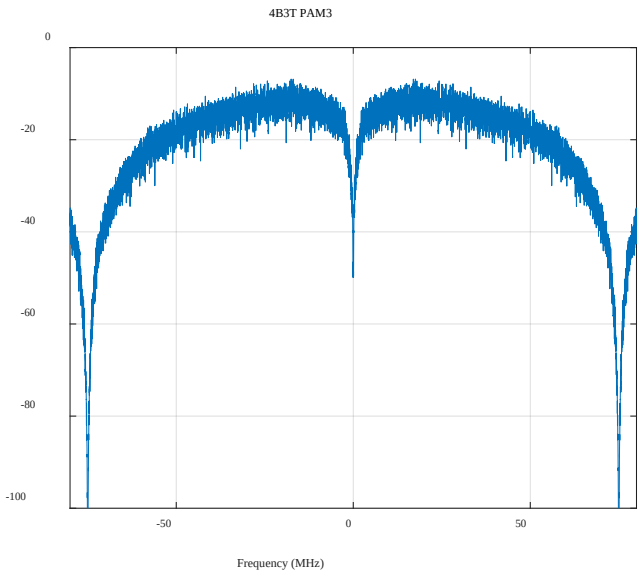
EFT impact

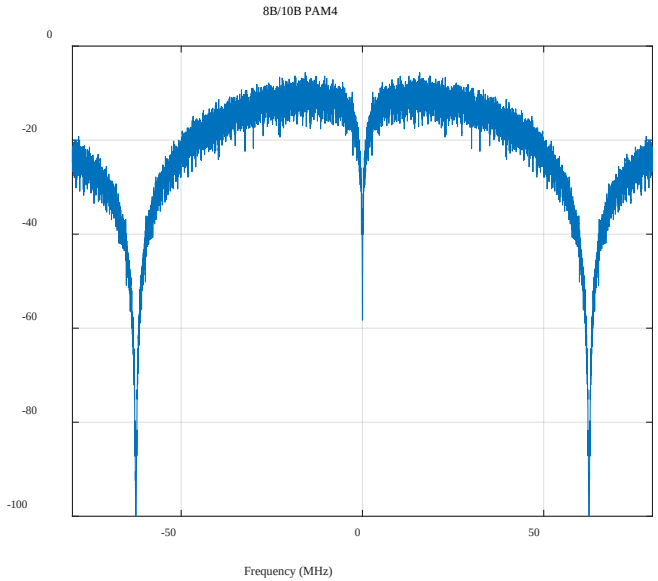
- The fastest burst rate of EFT specified by IEC61000-4-4 can reach 100 kHz (10 µs) with single burst duration of 50ns.
  - This indicates about 5 bit errors per 1000 bits transmitted at 100Mbps.
  - There are bunches of RS FEC satisfying this requirement.
- Single EFT pulse also adds ringing to the system. As evaluated by Graber, the ringing decays within 500ns and induces high-frequency (typ. ≥50MHz) interference (graber_3dg_01a_05172023.pdf).
  - Interleaved FEC or retransmission schemes can be used, which yet increases high latency and complexity.
  - LPFs are used in the 10BASE-T1L systems to suppress high-frequency components. For 802.3dg with data rate increased by 10 fold, the efficiency of LPF may be reduced, which yet depending on the signal bandwidth and filter design.

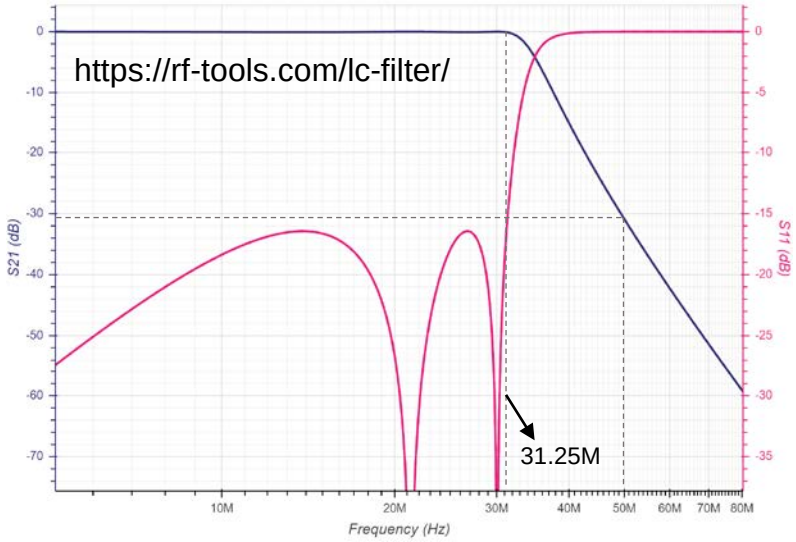


Ringing suppression by LPF

- Low spectral efficiency of PAM3 presents challenge on the PHY built-in LPF. Pulse shaping and partial response precoding can be considered to constrain signal bandwidth before transmission. Digital LPF may be also implemented to further suppress residual ringing.
- For PAM4 and PAM5, LPF with relatively low order and 30dB suppression for frequencies over 50MHz may be feasible. PAM4 has the same bandwidth as 8B4T PAM5 (Murray_3dg_01a_07102023.pdf). To achieve bounded disparity, 8B/10B PAM4 can be used, yet sacrificing spectral efficiency.







5th-order Chebyshev LPF

Burst error correction of FEC

- FEC is mainly used to correct burst errors induced by EFT pulse and the residual ringing after LPF.
  - 30dB suppression reduces the ringing Vpp by 96.8% (e.g. 2V to 63mV).
  - The decay duration may decrease from 500ns to less than 100ns.
- 150ns burst error correction for single EFT pulse might be sufficient for reliable communication.
  - There exist satisfied FEC codewords with overhead lower than 8%. Interleaving can be taken to further reduce the overhead, but needs to tradeoff hardware complexity.
  - Apart from these, coding gain, latency, complexity, and re-use are also important for FEC design.

Source: [graber_3dg_01a_05172023.pdf]

FEC delimiting

- For 10BASE-T1L, block coding and FEC are not utilized. 4B3T is used for data and idle, while special COMMA for data/idle transition. DISPRESET3 and the delimiter reset disparity and help distinguish the following information type.
- As mentioned before, FEC is required to ensure reliable 100Mbps communication. FEC delimiting needs to be done before normal data mode. PMA training frame is commonly used in BASE-T1 system for FEC delimiting.
  - Since FEC is not enabled during training, low-order PAM (e.g. PAM2) is preferred to achieve fast PMA convergence.
  - Intrinsic safety application requires bounded disparity in both data and training mode.
  - The length of the training frame should be decided according to the bit rate difference between two modes due to different PAMs, and the interleaved FEC length.

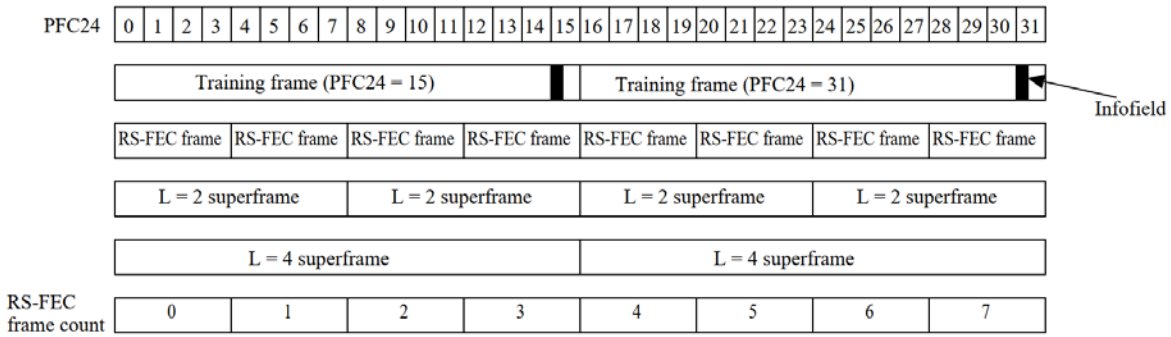
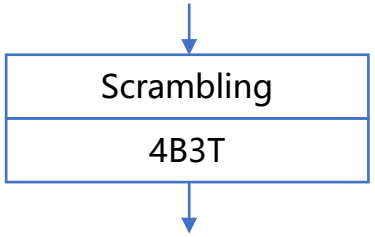


Figure 149–12—Timing relationship to PFC24

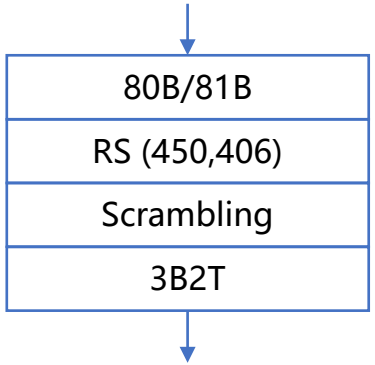
- 1000BASE-T1 data mode: RS(450,406,22,9), 3B2T
  - PAM2 training frame length: 2700 (450×9/3×2)
- 10GBASE-T1 data mode: RS(360,326,17,10), L=4, PAM4
  - PAM2 training frame length: 7200 (360×10×4/2)

PCS architecture

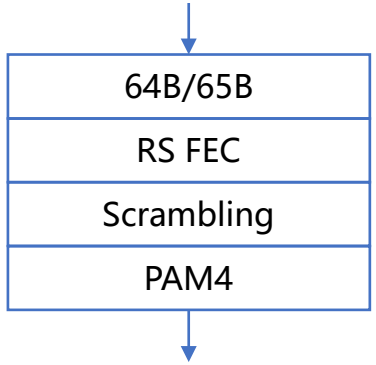
- For mBnT without FEC (e.g. 10BASE-T1L, 100BASE-T1), PCS can be simplified to only scrambling and line coding.
- PCS architecture in the case of FEC can learn from automotive SPE beyond 100Mbps. In the transmitter-side, block coding is implemented before FEC, which is followed by a side-stream scrambler before the final line coding.
  - PCS block coding may be shifted from the PCS to the serial MII, depending on the selected coding type.
  - To achieve bounded disparity for PAM4, 8B/10B can be performed separately on the scrambled two bit streams before binary (not Gray) coding. PCS architecture for PMA4 can be maximally shared with PMA training, selecting one 8B/10B coded bit stream for PAM2 mapping.
  - 33-bit side-stream scrambler has been widely used in full-duplex single pair Ethernet from 10Mbps to 25Gbps, covering EMC-sensitive applications (e.g. industry and automotive). It is also good option for 802.3dg.



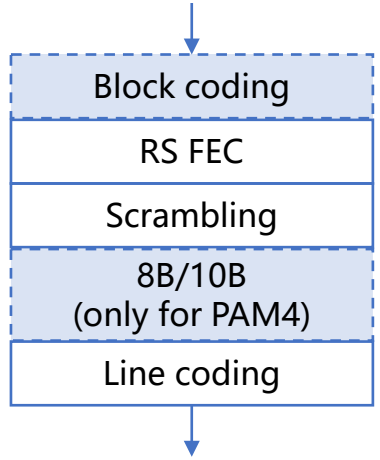
10BASE-T1L Tx PCS



1000BASE-T1 Tx PCS



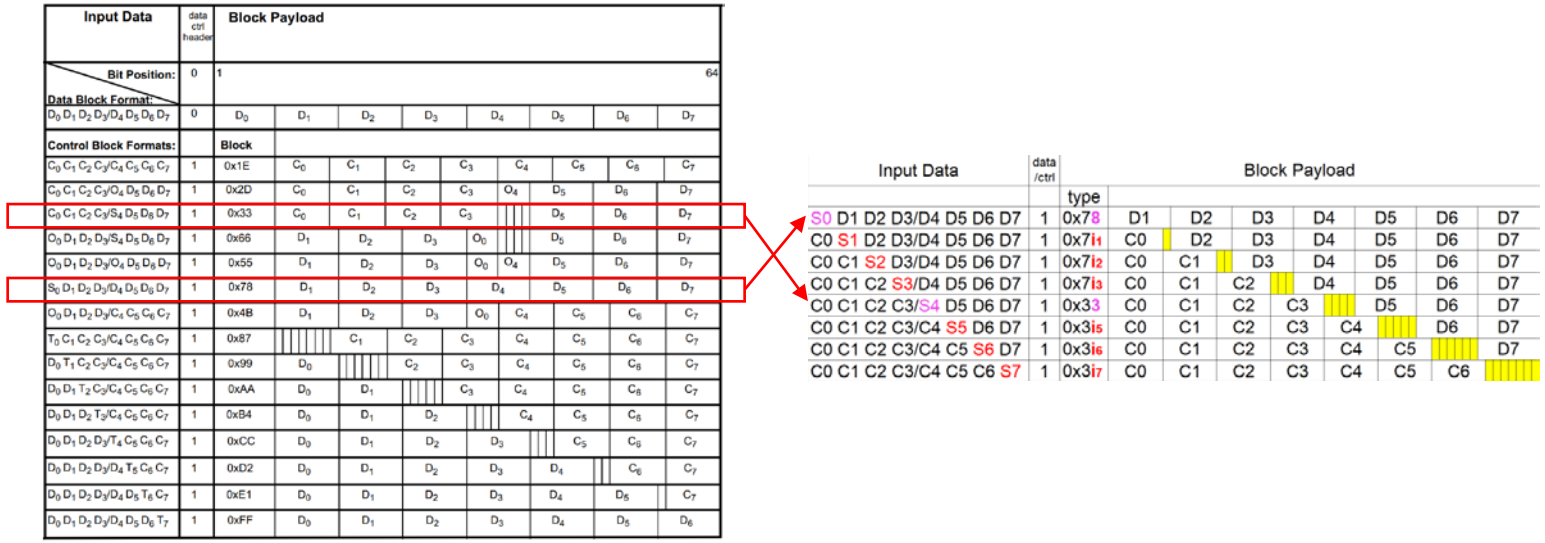
MultiGBASE-T1 Tx PCS



802.3dg Tx PCS

PCS block coding

- PCS block coding used in IEEE 802.3 standards mainly include 4B/5B, 8B/10B, 64B/66B, and 8n/8n+1.
  - The overhead of 4B/5B and 8B/10B is 25%, less attractive for the bandwidth-sensitive systems.
  - 64B/66B has been widely used in MultiGBASE-R.
  - The overhead of 8n/8n+1 coding decreases with the block size, sacrificing implementation complexity. 64B/65B is mainly adopted in MultiGBASE-T and MultiGBASE-T1. 80B/81B is only used in 1000BASE-T1.
- Option 1: Modified 64B/65B coding, with the block type field extended for different /S/ locations. 4-bit MSB of the 1-byte block type field may keep unchanged, while the 4-bit LSB is different depending on the /S/ location.
- Option 2: 80B/81B or a shorter block with similar coding principle. Any data and control combination is supported. Control code types can be increased by reducing the block length (e.g. from current 80bit to 64bit).



Input Data	data ctrl header	Block Payload							
Bit Position: / Data Block Format:	0	1							64
$D_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7$	0	D_0	D_1	D_2	D_3	D_4	D_5	D_6	D_7
Control Block Formats:		**Block**							
$C_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7$	1	0x1E	C_0	C_1	C_2	C_3	C_4	C_5	C_6	C_7
$C_0 C_1 C_2 C_3/O_4 D_5 D_6 D_7$	1	0x2D	C_0	C_1	C_2	C_3	O_4	D_5	D_6	D_7
$C_0 C_1 C_2 C_3/S_4 D_5 D_6 D_7$	1	0x33	C_0	C_1	C_2	C_3		D_5	D_6	D_7
$O_0 D_1 D_2 D_3/S_4 D_5 D_6 D_7$	1	0x66	D_1	D_2	D_3	O_0		D_5	D_6	D_7
$O_0 D_1 D_2 D_3/O_4 D_5 D_6 D_7$	1	0x55	D_1	D_2	D_3	O_0	O_4	D_5	D_6	D_7
$S_0 D_1 D_2 D_3/D_4 D_5 D_6 D_7$	1	0x78	D_1	D_2	D_3	D_4	D_5	D_6	D_7
$O_0 D_1 D_2 D_3/C_4 C_5 C_6 C_7$	1	0x4B	D_1	D_2	D_3	O_0	C_4	C_5	C_6	C_7
$T_0 C_1 C_2 C_3/C_4 C_5 C_6 C_7$	1	0x87		C_1	C_2	C_3	C_4	C_5	C_6	C_7
$D_0 T_1 C_2 C_3/C_4 C_5 C_6 C_7$	1	0x99	D_0		C_2	C_3	C_4	C_5	C_6	C_7
$D_0 D_1 T_2 C_3/C_4 C_5 C_6 C_7$	1	0xAA	D_0	D_1		C_3	C_4	C_5	C_6	C_7
$D_0 D_1 D_2 T_3/C_4 C_5 C_6 C_7$	1	0xB4	D_0	D_1	D_2		C_4	C_5	C_6	C_7
$D_0 D_1 D_2 D_3/T_4 C_5 C_6 C_7$	1	0xCC	D_0	D_1	D_2	D_3		C_5	C_6	C_7
$D_0 D_1 D_2 D_3/D_4 T_5 C_6 C_7$	1	0xD2	D_0	D_1	D_2	D_3	D_4		C_6	C_7
$D_0 D_1 D_2 D_3/D_4 D_5 T_6 C_7$	1	0xE1	D_0	D_1	D_2	D_3	D_4	D_5		C_7
$D_0 D_1 D_2 D_3/D_4 D_5 D_6 T_7$	1	0xFF	D_0	D_1	D_2	D_3	D_4	D_5	D_6	

64B/65B in IEEE 802.3-2022

Input Data	data /ctrl	Block Payload							
		type							
S0 D1 D2 D3/D4 D5 D6 D7	1	0x78	D1	D2	D3	D4	D5	D6	D7
C0 S1 D2 D3/D4 D5 D6 D7	1	0x7i1	C0	D2	D3	D4	D5	D6	D7
C0 C1 S2 D3/D4 D5 D6 D7	1	0x7i2	C0	C1	D3	D4	D5	D6	D7
C0 C1 C2 S3/D4 D5 D6 D7	1	0x7i3	C0	C1	C2	D4	D5	D6	D7
C0 C1 C2 C3/S4 D5 D6 D7	1	0x33	C0	C1	C2	C3	D5	D6	D7
C0 C1 C2 C3/C4 S5 D6 D7	1	0x3is	C0	C1	C2	C3	C4	D6	D7
C0 C1 C2 C3/C4 C5 S6 D7	1	0x3i6	C0	C1	C2	C3	C4	C5	D7
C0 C1 C2 C3/C4 C5 C6 S7	1	0x3i7	C0	C1	C2	C3	C4	C5	C6

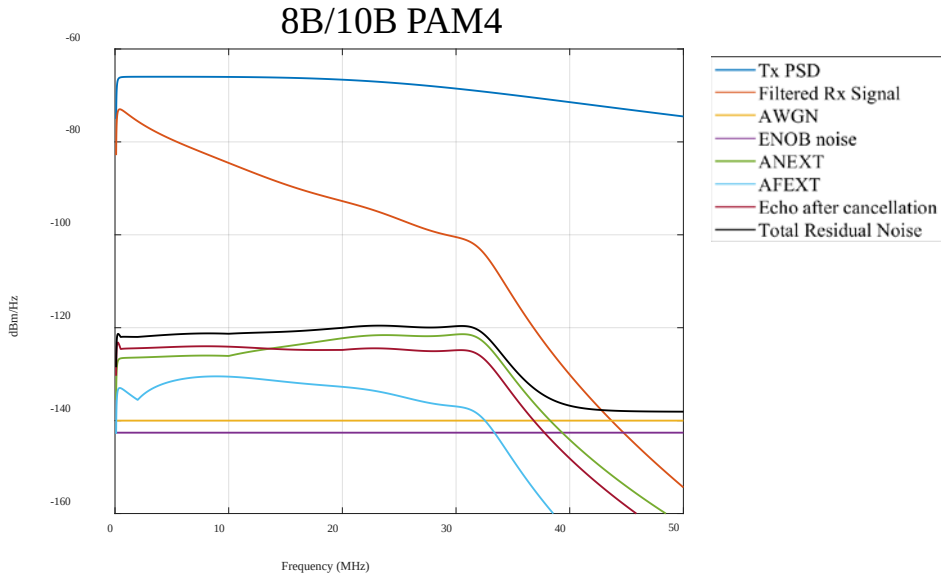
```
N = number of GMII octets encoded into block. Octets numbered n = 0,1,2,…,N-1.
octet 0 is the first one presented on GMII.
TC[n] = 0 if octet n is data octet on GMII, 1 if octet n is control octet on GMII
TC[-1] = 1 by definition
TD[n][0:7] = GMII octet n TXD[0:7] if TC[n] = 0
TD[n][5:7] = 010 - IPG (loc_phy_ready = OK), 101 - LPI, 001 - TX Error, 000 - IPG
(loc_phy_ready = NOT_OK) if TC[n] = 1. TD[n][0:4] is undefined.
B[0:8N] is the 8N+1 block. Bit 0 transmitted first.
OR(n) = Bitwise OR of TC[n:N-1]
NEXT(n)[0:3] = bit position of lowest bit in TC[n:N-1] that is a 1. Bit 3 is MSB.
NEXT(n)[4] = 0 if Bitwise SUM of TC[n:N-1] = 1, else 1

B[0] =              OR(0)
B[8n+1:8n+4] =      TD[n][0:3] - if OR(n) = 0
                    NEXT(n)[0:3] - if OR(n) = 1 AND TC[n-1] = 1
                    TD[n-1][3:6] - if OR(n) = 1 AND TC[n-1] = 0
B[8n+5] =           TD[n][4] - if OR(n) = 0
                    NEXT(n)[4] - if OR(n) = 1 AND TC[n-1] = 1
                    TD[n-1][7] - if OR(n) = 1 AND TC[n-1] = 0
B[8n+6:8n+8] =      TD[n][5:7] - if OR(n) = 0
                    TD[n][5:7] - if OR(n) = 1 AND TC[n] = 1
                    TD[n][0:2] - if OR(n) = 1 AND TC[n] = 0
```

80B/81B in IEEE 802.3-2022

Similar SNR Margin for PAM3, PAM4, PAM5

- Link segment parameters:
  - $IL(f) = \left(5.42 \times \sqrt{f} + 0.044 \times f + \frac{1.76}{\sqrt{f}}\right) + 5 \times 0.02 \times \sqrt{f}$
    with $0.1\ \text{MHz} \le f \le 60\ \text{MHz}$. $IL_{20} \approx 26\text{dB} > 23\text{dB}$
  - $RL = \begin{cases} 9 + 8f & 0.1\ \text{MHz} \le f < 0.5\ \text{MHz} \\ 13 & 0.5\ \text{MHz} \le f < 20\ \text{MHz} \\ 13 - 10log_{10}\left(\frac{f}{20}\right) & 20\ \text{MHz} \le f \le 60\ \text{MHz} \end{cases}$
  - $PSANEXT = \begin{cases} 60 & 0.1\ \text{MHz} \le f < 10\ \text{MHz} \\ 60 - 15log_{10}(f/10) & 10\ \text{MHz} \le f \le 60\ \text{MHz} \end{cases}$
  - $PSAACRF = \begin{cases} 60 & 0.1\ \text{MHz} \le f < 2\ \text{MHz} \\ 46 - 20log_{10}(f/10) & 2\ \text{MHz} \le f \le 60\ \text{MHz} \end{cases}$
- PHY parameters:
  - a 2nd-order butterworth filter at Nyquist Frequency;
  - 2.4V Vpp;
  - -140 dBm/Hz AWGN;
  - Chebyshev LPF with 1dB passband ripple and 30dB suppression for $f \ge 50\text{MHz}$ (filter order of 7, 6, 5 for PMA3/4/5);
  - 10-bit ENOB ADC, 45dB Echo suppression;
  - 64B/65B blocking coding overhead.

PAM level	Salz SNR (dB)	Required SNR (dB)	SNR Margin (dB)
4B3T PAM3	29.22	20.98	8.24
8B/10B PAM4	31.90	23.48	8.42
8B4T PAM5	34.79	25.42	9.37



PAM 3, 4, and 5 are all viable!

Comparison between different PAMs

- PAM3, PAM4, and PAM5 all achieve bounded disparity and similar SNR margin. PAM5 with smallest signal bandwidth allows easier LPF design. PAM3 and PAM4 has been widely used in BASE-T1 standards.
- Considering bounded disparity for PMA training using low-order PAM (typically PAM2), PAM4 realizes simplest PCS architecture without additional scrambler or line coding.

	PAM3	**PAM4**	**PAM5**
Usage in BASE-T1 standards	10BASE-T1 100BASE-T1 1000BASE-T1	2.5G/5G/10G/25GBASE-T1	None
Nyquist Frequncy (assuming 64B/65B block coding and 8% FEC overhead)	~41.1MHz	~34.3MHz	~27.4MHz
Bounded disparity	Yes (4B3T)	Yes (8B/10B)	Yes (8B4T)
Overall PCS complexity (data and training mode)	High	Low	High
LPF type (1dB passband ripple, ≥30dB suppression at 50MHz)	8^{th}-order Chebyshev	6^{th}-order Chebyshev	5^{th}-order Chebyshev
SNR Margin	8.24dB	8.42dB	9.37dB

Conclusion

- High-frequency (≥50MHz) interference induced by ringing needs to be suppressed by at least 30dB, so that FEC burst error correction may be relaxed to 150ns for single EFT pulse.
- FEC delimiting can be achieved with PMA training frame. The equivalent length of the training frame should be the same as the interleaved FEC in data mode.
- PCS architecture for 802.3dg starts from block coding, followed by FEC, scrambling, and the final line coding.
  - 64B/65B with extended the block type field can be used as the block coding.
  - The block coding may be shifted from the PCS to the serial MII, depending on the selected coding type.
  - 33-bit side-stream scrambler is a good choice for 802.3dg.
- PAM3, PAM4, and PAM5 all achieve bounded disparity and similar SNR margin. Each format has its advantages and disadvantages.
  - PAM5 with smallest signal bandwidth allows easier LPF design.
  - PAM3 and PAM4 has been widely used in BASE-T1 standards.
  - PAM4 allows most PCS functions shared between data and training mode.

Thank you!