Consideration on the solutions to low latency, intrinsic safety, and long reach

Tingting Zhang, Dongcheng Pan, Yan Zhuang

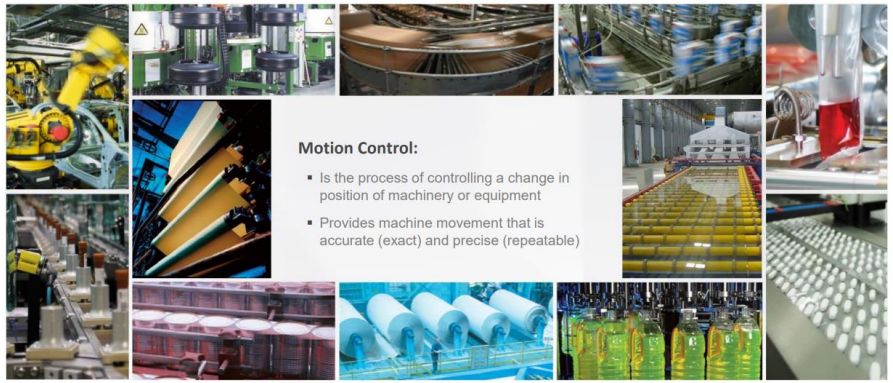
Huawei Technologies

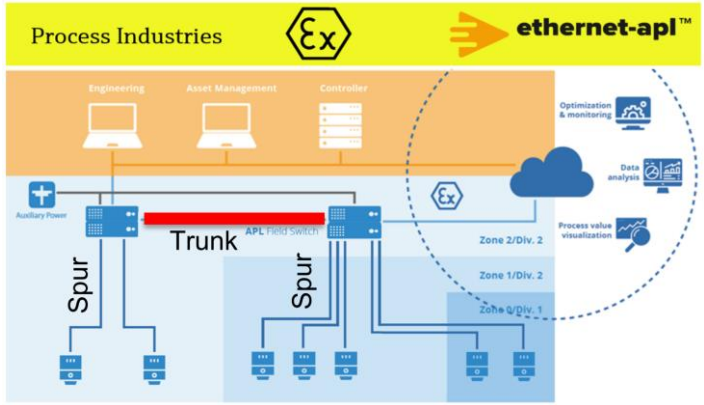
Introduction

- Progress of 802.3dg:
  - Consensus on link segments (July 2023)
  - Discussion on bounded disparity coding (4B3T PAM3, 8B/10B PAM4, 8B4T PAM5)
  - Discussion on PCS architecture, block coding, RS-FEC, and scrambler
  - Analysis on the latency of PCS sub-functions
- This presentation gives preliminary consideration on the solutions for motion control and process automation. Interleaved FEC and bounded disparity coding with smaller overhead is discussed.

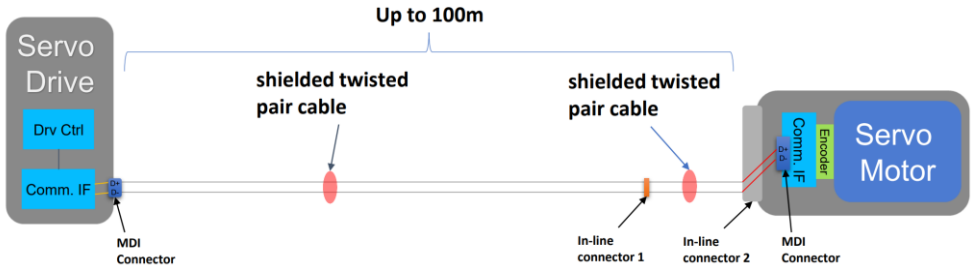
Application Scenarios

- Process automation and motion control are the two main driving forces for 100BASE-T1L.





mueller_3SPEP2P_01_0428_2021



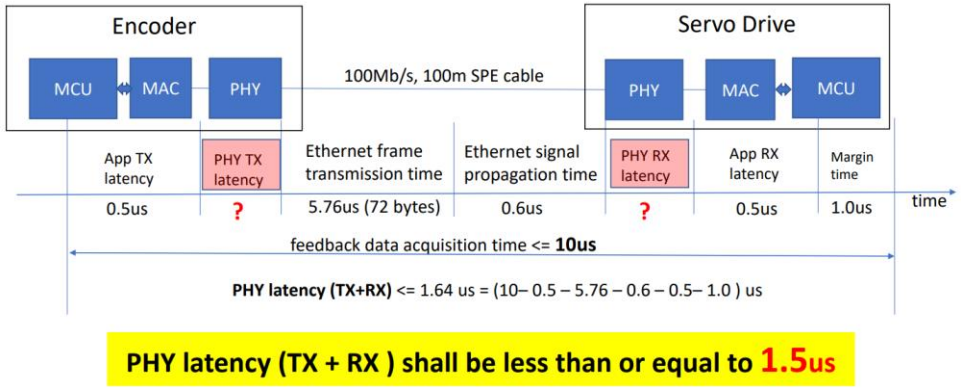
xu_3dg_01_05252022

	Motion control	PA-Spur	PA-Trunk
Cable length	≤100m (Typically AWG22)	≤200m	≤500m (AWG16)
Numbers of in-line connectors	≤2	≤5	≤5
Dominated Noise	PWM	EFT	EFT
Communication Characteristics	Low Latency	Bounded Disparity	Long reach

100BASE-T1 may be applicable to Motion Control

- The latency of a standard 100BASE-T1 PHY is constrained to be less than 1.32us, which meets the 1.5-us latency requirement for motion control application.
- IL of 100m AWG22 motor cabling @ 33.33MHz (3B/2T PAM3) is 12dB, which is also feasible for a 100BASE-T1 PHY with better equalization capability and higher SNR.

xu_3dg_01_05252022

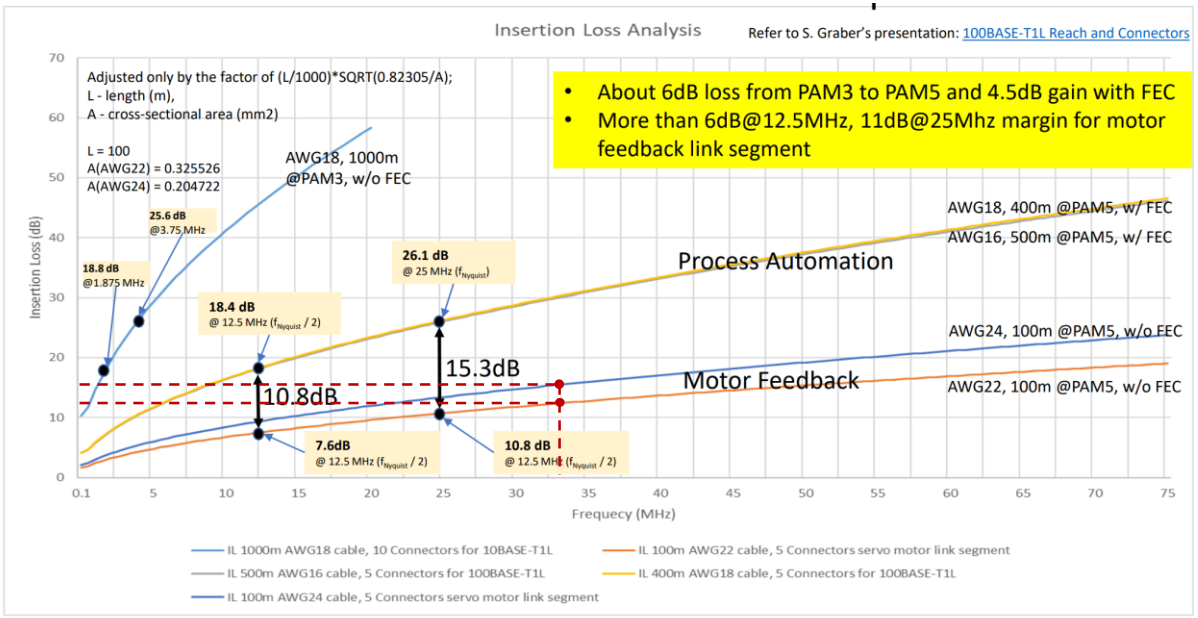


PHY latency (TX + RX) shall be less than or equal to 1.5us

96.10 Delay constraints

Every 100BASE-T1 PHY associated with MII shall comply with the bit delay constraints for full duplex operation. The delay for the transmit path, from the MII input to the MDI, shall be less than 360 ns. The delay for the receive path, from the MDI to the MII output, shall be less than 960 ns.

Source: IEEE 802.3 100BASE-T1 standard



xu_3dg_01_05252022

100BASE-T1L PHY Preferences

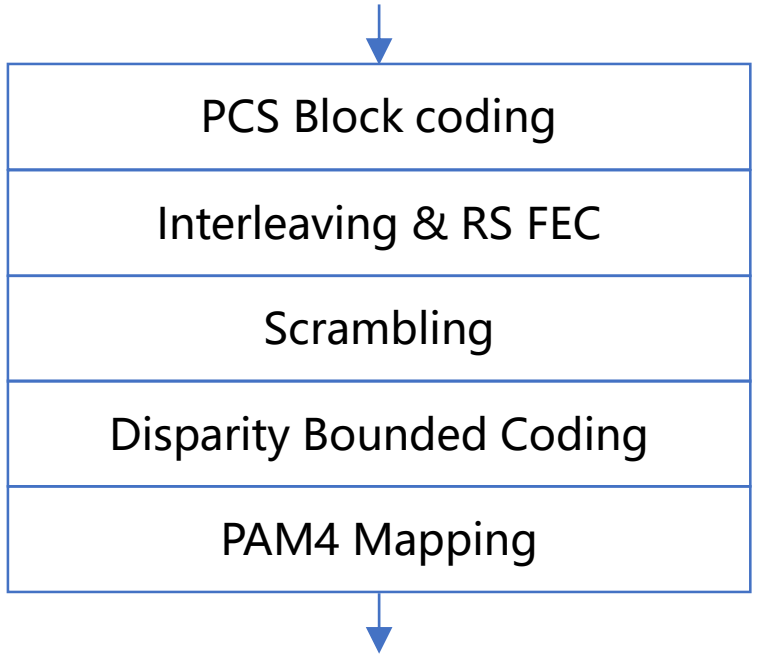
- The evolution of process industry is not as fast as automotive or data center, hybrid use of 10BASE-T1L and 100BASE-T1L in industry field is foreseeable in the near future.
    - 100BASE-T1L PHY supporting 10BASE-T1L mode benefits industrial SPE switches.
- Reusing 4B3T PAM3 in 100BASE-T1L results in symbol rate of 75MBaud, making 100BASE-T1L PHY design challenging due to large insertion loss (~36dB @ 37.25MHz for only link segment) for long-reach cable.
- PAM4 and PAM5 with higher spectral efficiency are more attractive, while PAM5 has higher linearity requirements.

Disparity and FEC

- Both PAM4 and PAM5 require special coding to bound the disparity for 200m spur application. The solutions include:
  - 8B4T PAM5 (Murray_3dg_01a_07102023) with coding rate of ~0.86
  - 8B/10B PAM4 (Tingting_3dg_01_25_10_2023) with 25% overhead
  - Lower overhead coding schemes (e.g. 9B/10B) may be considered.
- FEC in 802.3dg is mainly used to correct burst errors induced by EFT and the residual ringing.
  - Disparity bounded block coding may require longer burst error protection time, considering that the errors may affect more symbols.

PCS Architecture

- Since the low-latency requirement from motor control may be covered by 100BASE-T1, process automation is the prior application for 100BASE-T1L.
- The following PCS architecture not only allows bounded disparity for both training and data mode, but also simplifies PMA training.
  - 64B/65B or 80B/81B can be used as PCS block coding.
  - 8B/10B and 9B/10B are considered for disparity bounded coding.



FEC for 8B/10B PAM4

- RS FEC in GF(2^8) filed coupled with different interleaving depth (*L*) is considered for 8B/10B PAM4.
- For a given symbol error correction of 4, net coding gain decreases with *L* due to shorter block.
- FEC correcting 6 symbol errors, i.e. RS(67,61,3,8), is feasible with interleaving.
- For the listed FEC, the clock frequencies are achievable.

L	*n*	*k*	*t*	*m*	# OAM bits	# PCS blocks	Block coding	Frame (us)	Burst Error Protection (ns)	Symbol Rate (MBaud)	Overhead (%)	BERin @ BERout=1e-10	Net Coding Gain (dB)
1	89	81	4	8	0	8	80B/81B	6.4	287.6404	69.53 (25×89/32)	11.25	1.02E-04	4.27
	100	92	4	8	7	9	80B/81B	7.2	288	69.44 (25×25/9)	11.11	9.28E-05	4.26
	110	102	4	8	6	10	80B/81B	8	290.9091	68.75 (25×11/4)	10	8.58E-05	4.25
	120	112	4	8	5	11	80B/81B	8.8	293.3333	68.18 (25×30/11)	9.09	7.99E-05	4.23
	130	122	4	8	4	12	80B/81B	9.6	295.3846	67.71 (25×65/24)	8.33	7.49E-05	4.22
2	53	49	2	8	2	6	64B/65B	3.84	144.91	69.01 (25×265/96)	10.42	1.06E-05	3.16
	61	57	2	8	1	7	64B/65B	4.48	146.89	68.08 (25×305/112)	8.93	9.60E-06	3.16
	55	51	2	8	3	5	80B/81B	4	145.45	68.75 (25×11/4)	10	1.03E-05	3.16
	65	61	2	8	2	6	80B/81B	4.8	147.69	67.71 (25×65/24)	8.33	9.20E-06	3.16
	67	61	3	8	2	6	80B/81B	4.8	214.93	69.79 (25×67/24)	11.67	4.57E-05	3.81

FEC for 9B/10B PAM4

- 9B/10B and RS FEC in GF(2^9) field are considered. The coding rate is slightly higher than 8B4T PAM5.
- For interleaved RS(32,28,2,9), the symbol rate is the same as 100BASE-T1, allowing most resources to be shared.
- 12.5% overhead is more hardware friendly, allowing easier clock division and PLL.
- RS(62,54,4,9) with interleaving depth of 2 is able to correct up to 8 symbol errors.

L	*n*	*k*	*t*	*m*	# OAM bits	# PCS blocks	Block coding	Frame (us)	Burst Error Protection (ns)	Symbol Rate (MBaud)	Overhead (%)	BERin @ BERout=1e-10	Net Coding Gain (dB)
1	80	72	4	9	0	8	80B/81B	6.4	320	62.5 (25×5/2)	12.5	1.01E-04	4.21
	89	81	4	9	0	9	80B/81B	7.2	323.60	61.81 (25×89/36)	11.25	9.29E-05	4.21
	98	90	4	9	0	10	80B/81B	8	326.53	61.25 (25×49/20)	10.25	8.59E-05	4.20
	116	108	4	9	0	12	80B/81B	9.6	331.03	60.42 (25×29/12)	8.75	7.48E-05	4.18
2	32	28	2	9	9	3	80B/81B	2.4	150	66.67 (25×8/3)	20	1.39E-05	3.04
	48	44	2	9	6	6	64B/65B	3.84	160	62.5 (25×5/2)	12.5	1.05E-05	3.12
	50	46	2	9	9	5	80B/81B	4	160	62.5 (25×5/2)	12.5	1.02E-05	3.12
	58	54	2	9	0	6	80B/81B	4.8	165.52	60.42 (25×29/12)	8.75	9.19E-06	3.12
	60	54	3	9	0	6	80B/81B	4.8	240	62.5 (25×5/2)	12.5	4.55E-05	3.76
	61	55	3	9	9	6	80B/81B	4.8	236.07	63.54 (25×61/24)	14.38	4.49E-05	3.76
	62	54	4	9	0	6	80B/81B	4.8	309.68	64.58 (25×31/12)	16.25	1.25E-04	4.20

Conclusion

- Considering that PHY latency of 100BASE-T1 is within 1.32us, motion control application may be covered by 100BASE-T1 PHY with sufficient SNDR and equalization capability.
- Long reach prefers high-order modulation (PAM4 or PAM5), which enables easier PHY design than PAM3.
- Disparity bounded 9B/10B with lower overhead than 8B/10B can be considered. Its coding rate is also higher than 8B4T PAM5 requiring higher linearity.
  - Interleaved FEC helps improve burst error protection time.
  - A hardware-friendly symbol rate allows easier clock division and PLL.
  - Results in Slide 8 and 9 show that PAM4 can be a good start for PCS design.

Thank you!