PHY Parameter Decisions Towards Closure

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Agenda

- Present series of decisions to nail down PHY parameters
- Baseline acceptance criteria on what meets requirements
  - Eliminates moving target
  - Apples to Apples comparison
- Series of Straw Polls

- Recommendations (in red) are my opinions only

1. The MII

- MII as currently defined remains unchanged
  - Non-Negotiable
  - Nibble to byte alignment procedure easy to specify
  - For TSN – Timestamp at after the alignment, or (even better) don't send dribble nibbles at the MAC.
- Add sequence ordered set to MII
  - Recommend we add this
  - Fairly simple to do, just need to decide what this looks like.
- Reduce pin count MII – Single Port
  - Nice to have in current task force
- Reduce pin count MII – Multi Port
  - Out of scope for this task force in my opinion

2. Burst Error Protection

- Current consensus is FEC is needed for burst noise in some use cases
- Not all proposals include FEC in analysis
- Recommend we baseline at least one PHY variant shall include FEC
- All PHY proposals moving forward should include analysis with FEC variant.

3. How Long Should Burst Protection Be

- 150ns appears to be the number
- Do we need more? If so what is the target?

- Recommend we baseline 150 ns
  - Unless some other reasonable number is suggested

4. Low Latency Limit

- Early proposal of 1.5us max latency
- Moving target since

Reality check:

- Assume low latency is using FEC encoding but with FEC turned off at receiver
- Algorithm latency back of envelop calculation:
  - Proposals typically have 6 parity symbols ranging 5 to 9 bit symbols. Assume 8-bit symbols
  - Underflow buffering latency ~480ns
  - Assume 16/17 coding – latency ~2 x 16 bit-time = 320ns
  - Symbol mapping at receiver ~80ns
  - Total = 880ns

- Recommend we set the low latency acceptance criteria to not exceed 1.5us.

5. Transmit Bit Stream

- Do we require the transmit bit stream to be identical between full burst protection variant and low latency variant?
  - i.e. simply turn of FEC at the receiver for low latency
- Can reduce low latency variant latency even more if bit streams do not have to be identical.

- Recommend: Bit stream can be different between full FEC protection variant vs low latency variant

6. Baud Rates and PAM Levels

- This applies only if in #5 we can accept different bit streams

a) Same baud rate, same PAM
   - Can reduce latency with periodic padding instead of FEC frame. No electrical benefits.

b) Different baud rate, same PAM
   - Low latency runs slower without FEC parity overhead

c) Same baud rate, different PAM
   - Low latency runs PAM3 without FEC parity overhead, full protection runs PAM4

d) Different baud rate, different PAM
   - This permutation doesn't make sense

- No recommendation here. More complexity to get better low latency performance

7. Low Latency FEC Options

- This applies only if in #5 we can accept different bit streams, and we reject #6 b, c, d

- Options:
  - Low latency has no burst protection only
  - Low latency has some burst protection only
  - Low latency has some burst protection with option to disable FEC at receiver to lower latency even more

8. PAM 3 vs PAM 4

- Set the baselines above in 2-7
- Do apples to apples performance comparison between PAM3 vs PAM4
  - Same noise assumptions
  - Equivalent FEC strengths
  - Set the baud rates to accommodate the FEC overhead
  - Can we get similar 3dB gain from partial response with PAM 4 as with PAM 3

    https://www.ieee802.org/3/dg/public/May_2024/Murray_3dg_01_05132024.pdf

    1+D is 7 levels for PAM4 instead of 5 levels for PAM3

Straw Polls

1) I support adding sequence ordered set to MII: Y/N/A
2) I support at least one PHY variant with forward error correction: Y/N/A
3) I support FEC burst protection of at least 150 ns for one PHY variant: Y/N/A
4) I support low latency requirement not to exceed 1.5us: Y/N/A
5) I can accept the bit stream being different between full burst protection PHY variant vs low latency PHY variant: Y/N/A
6) (This one applies only if #5 is Yes) Chicago Rules:

   To better optimize low latency operation I can support

   a) Same baud rate, same PAM for both full burst protection and low latency
   b) Same PAM, but fast baud rate for full burst protection and slower baud rate for low latency
   c) Same baud rate, but PAM4 for full burst protection and PAM3 for low latency

THANK YOU