



The bridge to possible

# NEA MII Presentation Planning

Collaborative Development of an NEA Presentation

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Affiliated with Cisco

2024-07-15

# Goals for this Presentation

- Share starting point for an NEA presentation slide deck
- Recruit input on incomplete sections
- Recruit participants to join an Ad Hoc on Tuesday



The bridge to possible

# A New MII for the Future

Building Consensus around Goals and Strategy

Jason Potterf

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Date TBD

# NEA Presentation Agenda

- Brief History of Ethernet MII Solutions
- Motivating Factors in 802.3da and 802.3dg that Require a new MII
- Market Considerations
- Possible Path Forward Based on 802.3dg Straw Poll Results
- Discussion and Straw Polls

*Feedback Requested*

- This is far too much detail.  
How much is enough?

# Brief History of Ethernet MII Solutions

# MII Evolution

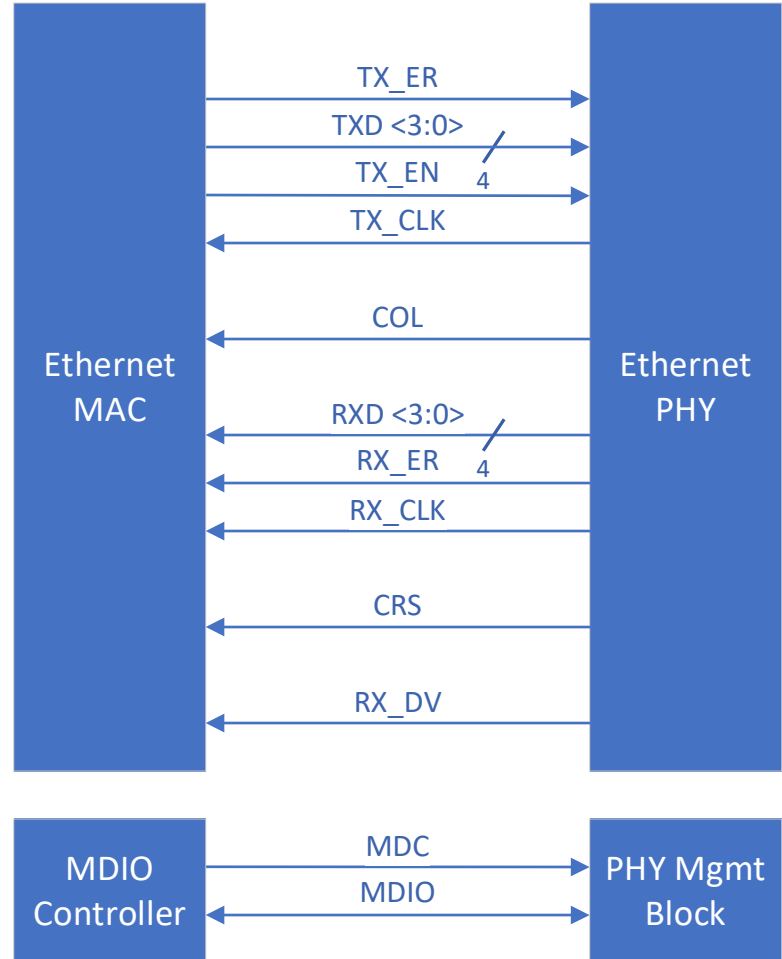
## The Parallel Busses

## IEEE 802.3

### Clause 22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

#### MII Score Card

<b>Max Data Rate</b>	100 Mbit/s
<b>Signal Count</b>	16 Data + 2 Mgmt
<b>Bus Max Clock Rate</b>	25 MHz
<b>Clock Scheme</b>	PHY Synchronous
<b>Command Space</b>	4-bit
<b>Commands Assigned</b>	Tx - 4/16, Rx – 5/16
<b>PLCA Support</b>	Yes, Beacon and Commit



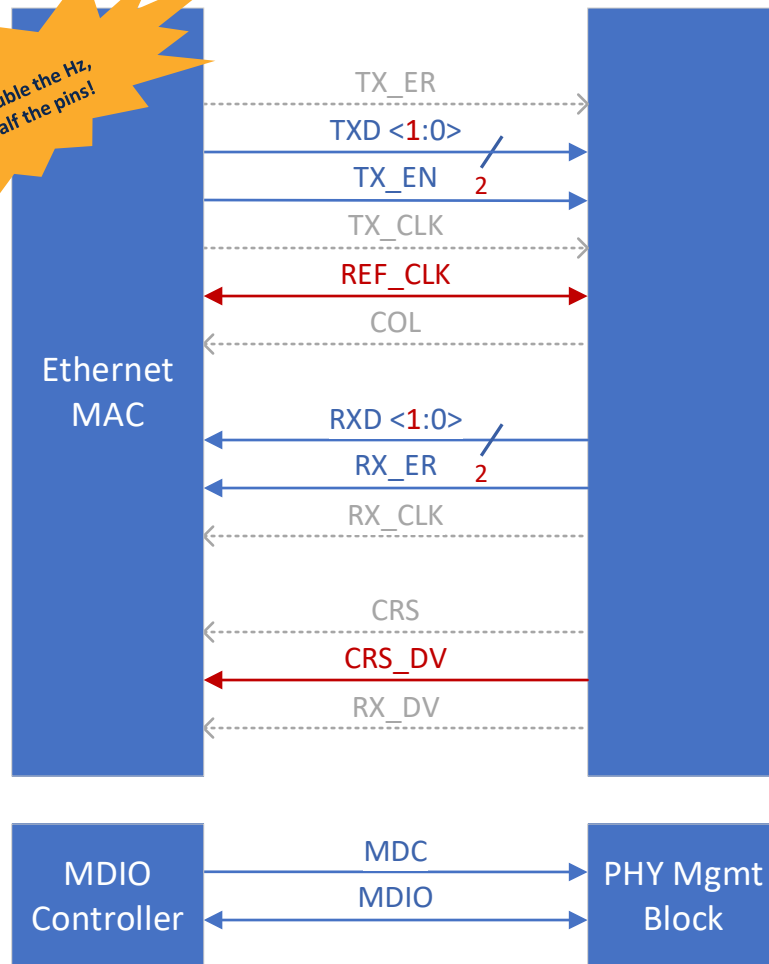
# Industry Specification Reduced Media Independent Interface

## MII Score Card

<b>Max Data Rate</b>	100 Mbit/s
<b>Signal Count</b>	<b>7 Data + 1 Clk + 2 Mgmt</b>
<b>Bus Max Clock Rate</b>	<b>50 MHz</b>
<b>Clock Scheme</b>	System Synchronous
<b>Command Space</b>	2-bit
<b>Commands Assigned</b>	Tx - 2/4, Rx - 2/4 (Note 1)
<b>PLCA Support</b>	<b>No</b>

**Note 1** – Some vendors have assigned values for EEE outside of the RMII spec.

Contribution to IEEE P802.3dg 100 Mb/s Long-Reach Single Pair Ethernet Task Force



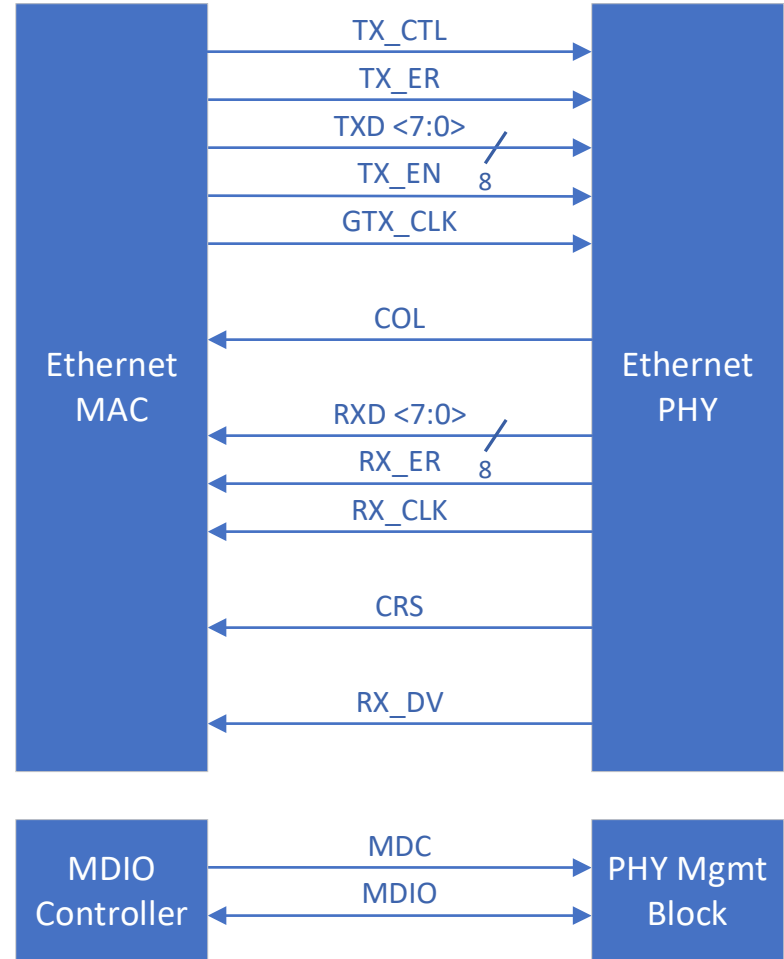


## IEEE 802.3

### Clause 35. Reconciliation Sublayer (RS) and Gigabit Media Independent Interface (GMII)

#### MII Score Card

<b>Max Data Rate</b>	1000 Mbit/s
<b>Signal Count</b>	25 Data + 2 Mgmt
<b>Bus Max Clock Rate</b>	125 MHz
<b>Clock Scheme</b>	Source Synchronous
<b>Command Space</b>	8-bit
<b>Commands Assigned</b>	Tx - 4/256, Rx - 5/256
<b>PLCA Support</b>	<b>No</b>

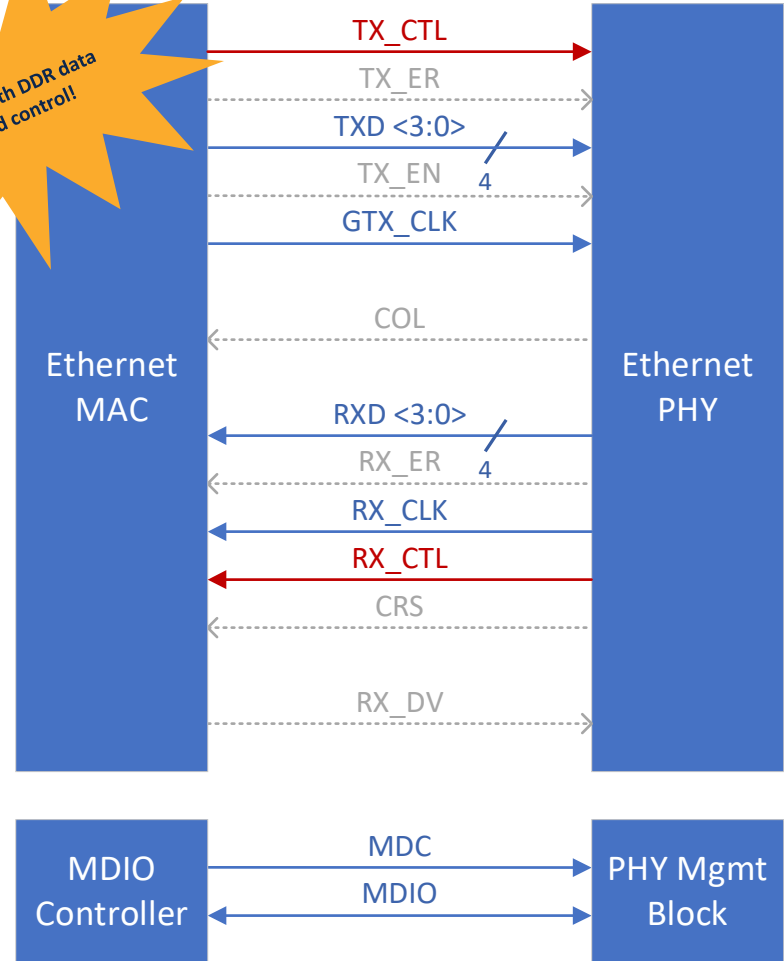


# Industry Specification Reduced Gigabit Media Independent Interface

## MII Score Card

<b>Max Data Rate</b>	1000 Mbit/s
<b>Signal Count</b>	<b>12 Data</b> + 2 Mgmt
<b>Bus Max Clock Rate</b>	125 MHz
<b>Clock Scheme</b>	Source Synchronous DDR
<b>Command Space</b>	8-bit
<b>Commands Assigned</b>	Tx - 2/256, Rx - 4/256
<b>PLCA Support</b>	<b>No</b>

Now with DDR data and control!



MII Evolution

Parallel Bus Command Space

# MII Commands

- Cause Transmission or Indicate Reception of something other than valid data bytes on the wire
- Uses TX\_EN / TX\_ER / RX\_En / RX\_ER to create address space
- Currently Defined in 802.3 Clause 22
  - Assert LPI
  - PLCA Beacon Request / Indication
  - PLCA Commit Request / Indication
  - False Carrier Indication

Table 22–1—Permissible encodings of TXD<3:0>, TX\_EN, and TX\_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Reserved
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON request
0	1	0011	PLCA COMMIT request
0	1	0100 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

Table 22–2—Permissible encoding of RXD<3:0>, RX\_ER, and RX\_DV

RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON indication
0	1	0011	PLCA COMMIT indication
0	1	0100 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

# GMII Commands

- GMII increases address space with wider bus
- Uses same control signals as MII, TX\_EN / TX\_ER / RX\_En / RX\_ER, to create address space
- Currently Defined in 802.3 Clause 22
  - Assert LPI
  - False Carrier indication
  - Carrier Extend/ Carrier Extend Error
- **PLCA not defined here, but RGMII would benefit when operating at 10 Mb/s data rates**

Table 35–1—Permissible encodings of TXD<7:0>, TX\_EN, and TX\_ER

TX_EN	TX_ER	TXD<7:0>	Description	PLS_DATA.request parameter
0	0	00 through FF	Normal inter-frame	DATA_COMPLETE
0	1	00	Reserved	—
0	1	01	Assert LPI	—
0	1	02 through 0E	Reserved	—
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	EXTEND_ERROR (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data transmission	ZERO, ONE (eight bits)
1	1	00 through FF	Transmit error propagation	No applicable parameter

NOTE—Values in TXD<7:0> column are in hexadecimal.

Table 35–2—Permissible encoding of RXD<7:0>, RX\_ER, and RX\_DV

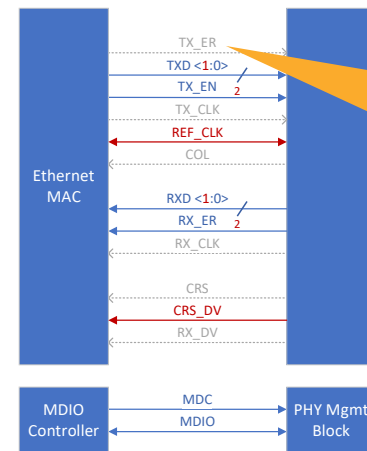
RX_DV	RX_ER	RXD<7:0>	Description	PLS_DATA.indication parameter
0	0	00 through FF	Normal inter-frame	No applicable parameter
0	1	00	Normal inter-frame	No applicable parameter
0	1	01	Assert LPI	No applicable parameter
0	1	02 through 0D	Reserved	—
0	1	0E	False Carrier indication	No applicable parameter
0	1	0F	Carrier Extend	EXTEND (eight bits)
0	1	10 through 1E	Reserved	—
0	1	1F	Carrier Extend Error	ZERO, ONE (eight bits)
0	1	20 through FF	Reserved	—
1	0	00 through FF	Normal data reception	ZERO, ONE (eight bits)
1	1	00 through FF	Data reception error	ZERO, ONE (eight bits)

NOTE—Values in RXD<7:0> column are in hexadecimal.

# RMII / RGMII Compromises

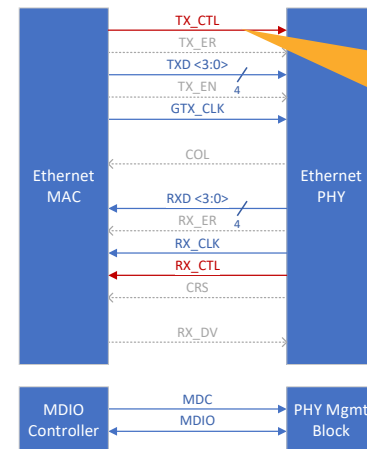
- RMII assumed the following
  - COL can be derived
  - CRS and RX\_DV can merge
  - TX\_ER's purpose can be accomplished by intentional data corruption and will be obsoleted by switches
  - Two-bit data bus values during TX\_EN / CRS\_DV low can be use for control codes
- RGMII made similar assumptions about derived signals, but due to DDR clocking **did not compromise on control codes**

## RMII



RMII Removed the TX\_ER signal and made RX\_ER optional, reducing address space

## RGMII



RGMII TX\_CTL and RX\_CTL for both clock edges, restoring address space parity with GMII

# MII Evolution

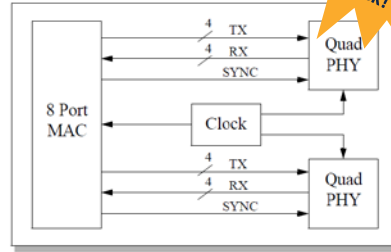
## The Serial Buses

# Cisco Specification Serial-MII (aka SMII)

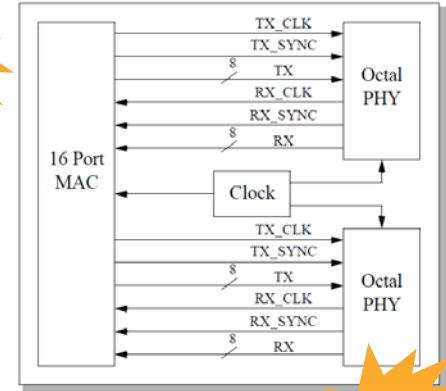
## MII Score Card

Max Data Rate	100 Mbit/s
Signal Count	<b>2/port</b> + 2-5/PHY + 2 Mgmt
Bus Max Clock Rate	125 MHz
Clock Scheme	System or PHY Synchronous
Command Space	<b>8-bit bitfield</b>
Commands Assigned	Tx - 5/8, Rx - 7/8 bits
PLCA Support	<b>No</b>

## System Diagrams

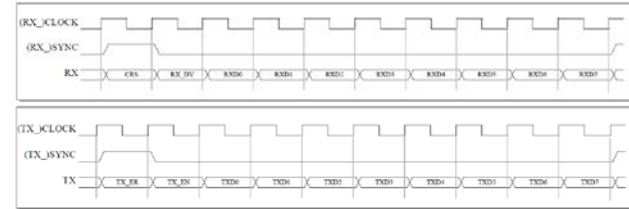


Typical SMII System



Source Synchronous SMII System

## Timing Diagrams



## Command Bit Assignments

CRS	RX_DV	RXD0	RXD1	RXD2	RXD3	RXD4	RXD5	RXD6	RXD7
x	0	RX_ER from previous frame	Speed 0 = 10MBit 1 = 100MBit	Duplex 0 = Half 1 = Full	Link 0 = Down 1 = Up	Jabber 0 = OK 1 = Error	Upper Nibble 0 = invalid 1 = valid	False Carrier Detected	1
x	1	One Data Byte (Two MII Data Nibbles)							

### RXD7-0 Encoding

TX_ER	TX_EN	TXD0	TXD1	TXD2	TXD3	TXD4	TXD7-5
x	0	Use to force an error in a direct MAC to MAC connection	1 100MBit	1 Full Duplex	1 Link Up	0 No Jabber	1
x	1	One Data Byte (Two MII Data Nibbles)					

### TXD7-0 Encoding

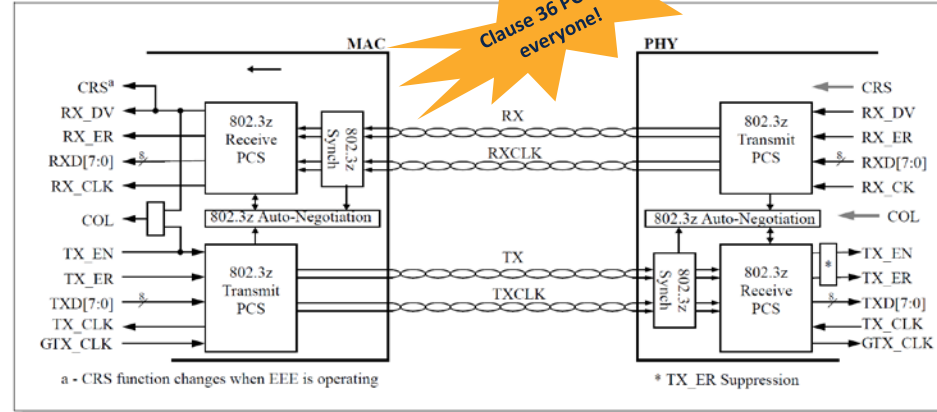


# Cisco Specification Serial-GMII (aka SGMII)

## MII Score Card

Max Data Rate	1000 Mbit/s
Signal Count	4/port + 2 Mgmt
SerDes Max Rate	1.25 Gb/s
Clock Scheme	SerDes or Source Sync
Command Space	Large – Ordered Sets
Commands Assigned	8 Non-Idle Sets Defined
PLCA Support	No

## System Diagrams (SGMII Spec)



## PCS Scheme (Clause 36)

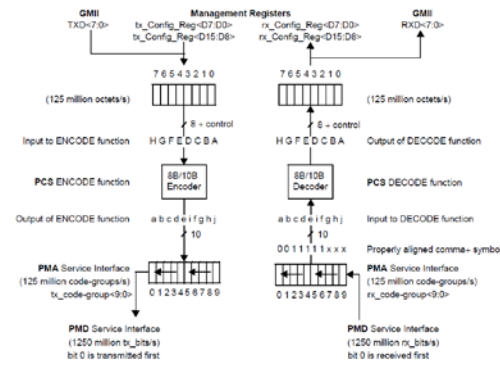


Figure 36-3—PCS reference diagram

## Commands (Clause 36)

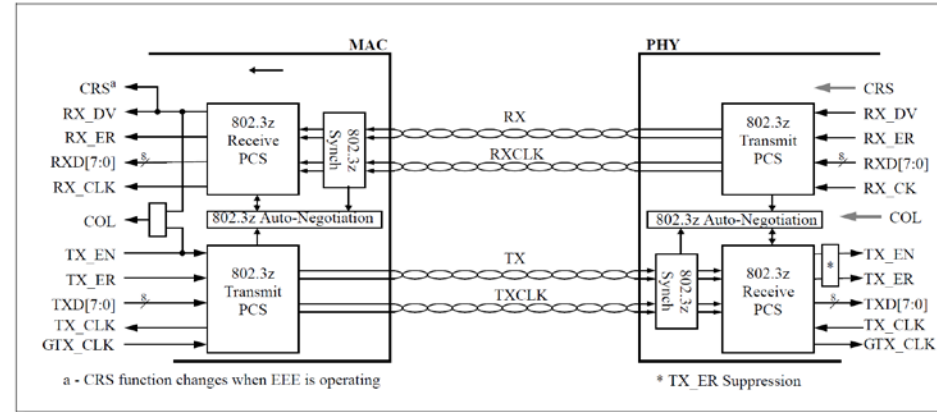
Table 36-3—Defined ordered sets

Code	Ordered Set	Number of Code-Groups	Encoding
C/	<b>Configuration</b>		Alternating C1/ and C2/
C1/	Configuration 1	4	/K28.5/D21.5/Config_Reg <sup>a</sup>
C2/	Configuration 2	4	/K28.5/D2.2/Config_Reg <sup>a</sup>
I/	<b>IDLE</b>		Correcting I1/, Preserving I2/
I1/	IDLE 1	2	/K28.5/D5.6/
I2/	IDLE 2	2	/K28.5/D16.2/
	<b>Encapsulation</b>		
R/	Carrier_Extend	1	/K23.7/
S/	Start_of_Packet	1	/K27.7/
T/	End_of_Packet	1	/K29.7/
V/	Error_Propagation	1	/K30.7/
L/	<b>LPI</b>		Correcting L1/, Preserving L2/
L1/	LPI 1	2	/K28.5/D6.5/
L2/	LPI 2	2	/K28.5/D26.4/

<sup>a</sup>Two data code-groups representing the Config\_Reg value.

# SGMII Choices

- Source Synchronous vs SerDes
  - Left to implementers, but all used SerDes
- SGMII assumed the following
  - CRS and COL can be derived
    - COL suffers added latency, though, which is problematic
  - Speeds < 1Gb/s achieved by “elongation” where bytes are duplicated 10x or 100x to allow constant SerDes data rates
- SGMII’s use of the Clause 36 PCS gives us a large control code address space via 8b/10b code group ordered sets
  - EEE modified Clause 36 to enable LPI
  - **PLCA did not define ordered sets in Clause 36 for COMMIT and BEACON as the PCS is only defined for 1 Gb/s data rates**



# MII Evolution

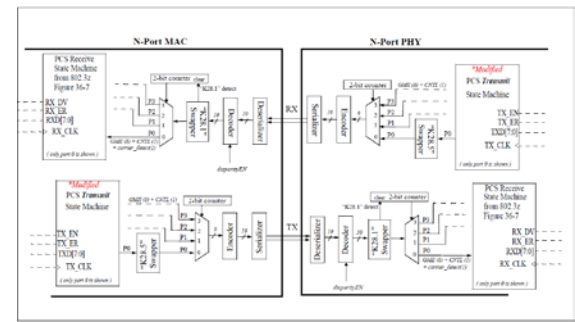
## The Multi-Port Serial Busses

# Cisco Specification Quad Serial GMII (aka QSGMII)

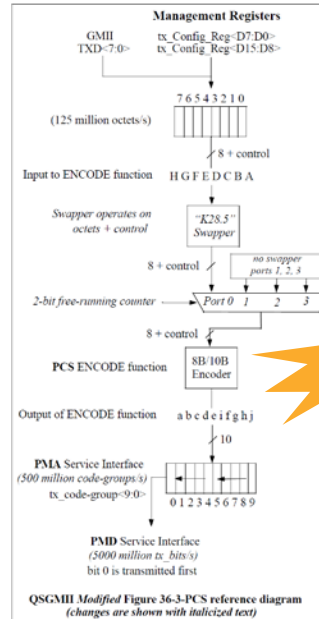
## MII Score Card

Max Data Rate	1000 Mbit/s, 4 Ports
Signal Count	4/Quad Phy + 2 Mgmt
SerDes Max Rate	5.0 Gb/s
Clock Scheme	SerDes
Command Space	Large – Ordered Sets
Commands Assigned	K28.1 Reserved 8 Non-Idle Sets Defined
PLCA Support	No

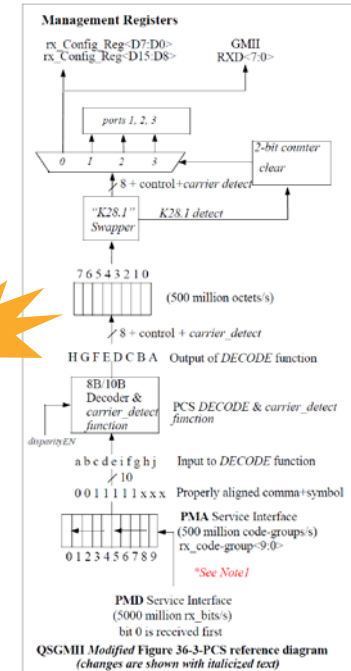
## QSGMII Overview



## QSGMII PCS TX Scheme



## QSGMII PCS RX Scheme



**Multiplex faster!**

QSGMII Modified Figure 36-3-PCS reference diagram (changes are shown with italicized text)

QSGMII Modified Figure 36-3-PCS reference diagram (changes are shown with italicized text)

One to Rule Them All!

We're tired of doing these!

# Cisco Specification Universal Serial GMII (aka USGMII)

## MII Score Card

**Max Data Rate** 1000 Mbit/s, with 8, 4, and 1 Port Modes

**Signal Count** 4/Octal PHY + 2 Mgmt

**SerDes Max Rate** 10.0, 5.0, 1.25 Gb/s

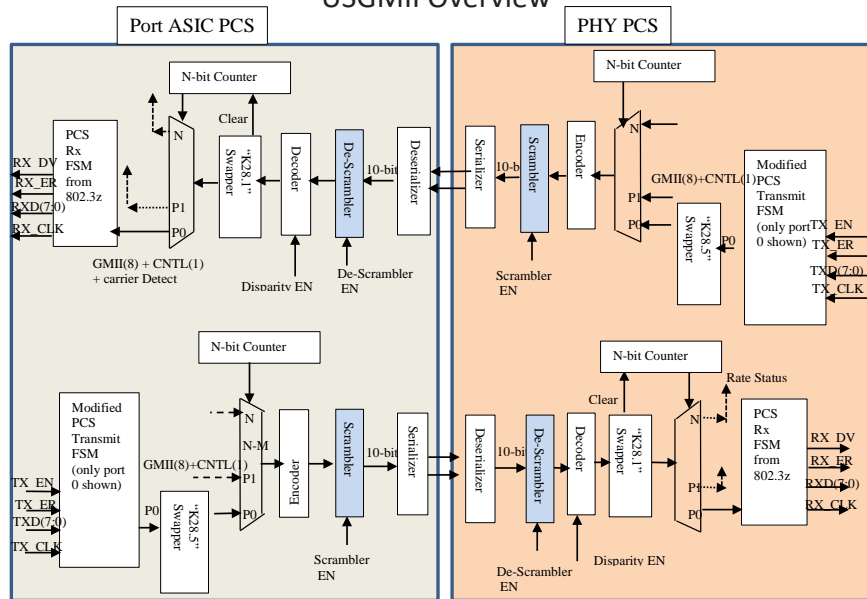
**Clock Scheme** SerDes

**Command Space** Large – Ordered Sets Packet Control Header

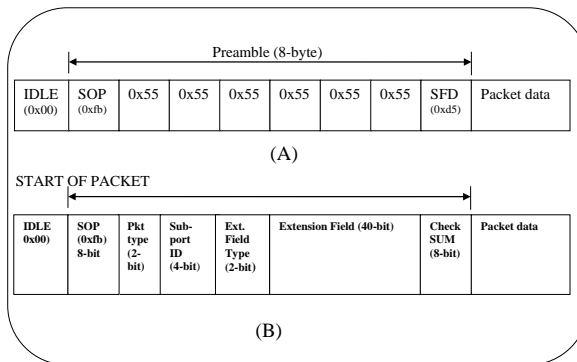
**Commands Assigned** K28.1 Reserved  
8 Non-Idle Sets Defined  
**PCH Packet Types**

**PLCA Support** No

## USGMII Overview



## Packet Control Header



## PCH Packet Types

- 00: Ethernet Packet with PCH
- 01: Ethernet packet, without PCH (packet information)
- 10: Idle Packet – Contains status data for a port – no packet data
- 11: Preemption Frame, aka Interspersing Express Traffic (IET) frame

**In-Band PTP Timestamps via Extension Field**

MII Evolution

10 Gig / mGig MII Interfaces

# XGMII

- XGMII Defined in 802.3 Clause 46. Reconciliation Sublayer (RS) and 10 Gigabit Media Independent Interface (XGMII)
- High complexity 32-bit wide bus
- Employs byte-wise lane striping
- Per-lane control signals add pins
- Lane management adds unnecessary complexity
- **Overkill for SPE applications**

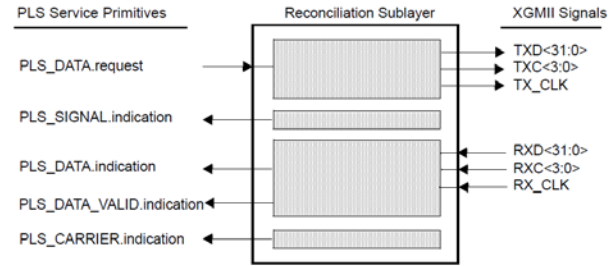


Figure 46-2—Reconciliation Sublayer (RS) inputs and outputs

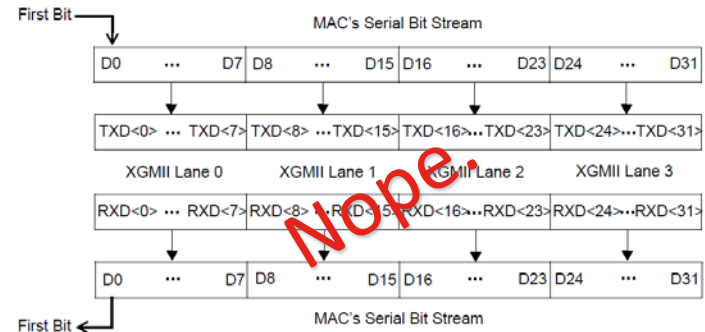


Figure 46-4—Relationship of data lanes to MAC serial bit stream

# USXGMII Family

- Two Cisco Specs for mGig
  - Universal SXGMII Interface for a Single MultiGigabit Copper Network Port
  - Universal SXGMII PHY-MAC Interface for Multiple Network Ports
- All the features
  - 1-8 ports per SerDes pair
  - SerDes Speeds from 5Gb/s to 20 Gb/s
  - Packet Control Header
  - Clause 46 ordered sets
  - Clause 49 PCS
    - 64/66b encoding adds latency
- **Complexity and latency not appropriate for SPE**

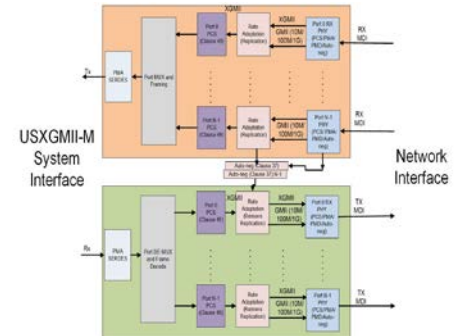
## USXGMII Modes

USXGMII Type	Num Prts	Network Port Types	Replications – Lowest to Highest data speed	PCS	SERDES Speed (Gbps)
10G-USXGMII	1	100M/1G/2.5G/5G/10G	100, 10, 4, 2, 1	Clause 49	10.3125
5G-USXGMII	1	100M/1G/2.5/5G	50, 5, 2, 1	Clause 49	5.15625

## USXGMII Modes

MP-USXGMII Type	Num Prts	Network Port Types	Replications – Lowest to Highest data speed	PCS	SERDES Speed (Gbps)
10G-SXGMII	1	10M/100M/1G/2.5G/5G/10G	1000/100/10/4/2/1	Clause 49	10.3125
5G-SXGMII	1	10M/100M/1G/2.5/5G	500/50/5/2/1	Clause 49	5.15625
10G-DXGMII	2	10M/100M/1G/2.5G/5G	500/50/5/2/1	Clause 49	10.3125
5G-DXGMII	2	10M/100M/1G/2.5G	250/25/2.5/1	Clause 49	5.156
20G-QXGMII	4	10M/100M/1G/2.5G/5G	500/50/5/2/1	Clause 49	20.625
20G-DXGMII	2	10M/100M/1G/2.5G/5G/10G	1000/100/10/4/2/1	Clause 49	20.625
2.5G-SXGMII	1	10M/100M/1G/2.5G	250/25/2.5/1	Clause 49	2.578125
10G-QXGMII	4	10M/100M/1G/2.5G	250/25/2.5/1	Clause 49	10.3125
20G-OXGMII	8	10M/100M/1G/2.5G	250/25/2.5/1	Clause 49	20.625

Nope.





*Feedback Requested*

- Is this the right amount of detail or is this too little?

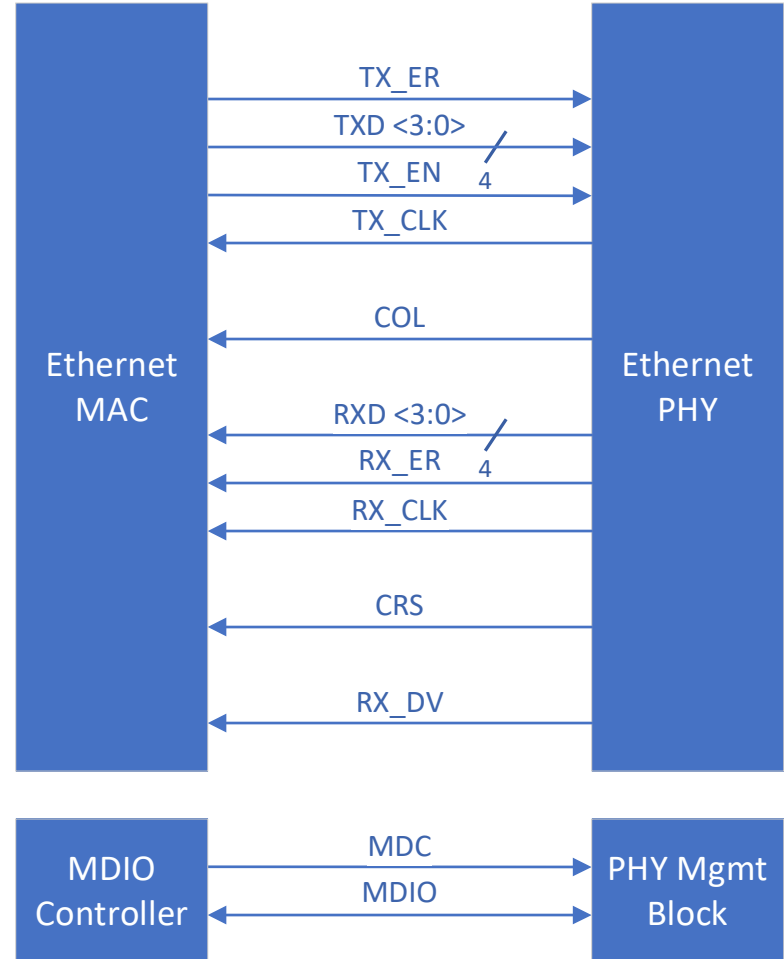
# Quick Review of Past MIIs

## IEEE 802.3

### Clause 22. Reconciliation Sublayer (RS) and Media Independent Interface (MII)

#### MII Score Card

<b>Max Data Rate</b>	100 Mbit/s
<b>Signal Count</b>	16 Data + 2 Mgmt
<b>Bus Max Clock Rate</b>	25 MHz
<b>Clock Scheme</b>	PHY Synchronous
<b>Command Space</b>	4-bit
<b>Commands Assigned</b>	Tx - 4/16, Rx – 5/16
<b>PLCA Support</b>	Yes, Beacon and Commit



# MII Commands

- Cause Transmission or Indicate Reception of something other than valid data bytes on the wire
- Uses TX\_EN / TX\_ER / RX\_En / RX\_ER to create address space
- Currently Defined in 802.3 Clause 22
  - Assert LPI
  - PLCA Beacon Request / Indication
  - PLCA Commit Request / Indication
  - False Carrier Indication

Table 22–1—Permissible encodings of TXD<3:0>, TX\_EN, and TX\_ER

TX_EN	TX_ER	TXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Reserved
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON request
0	1	0011	PLCA COMMIT request
0	1	0100 through 1111	Reserved
1	0	0000 through 1111	Normal data transmission
1	1	0000 through 1111	Transmit error propagation

Table 22–2—Permissible encoding of RXD<3:0>, RX\_ER, and RX\_DV

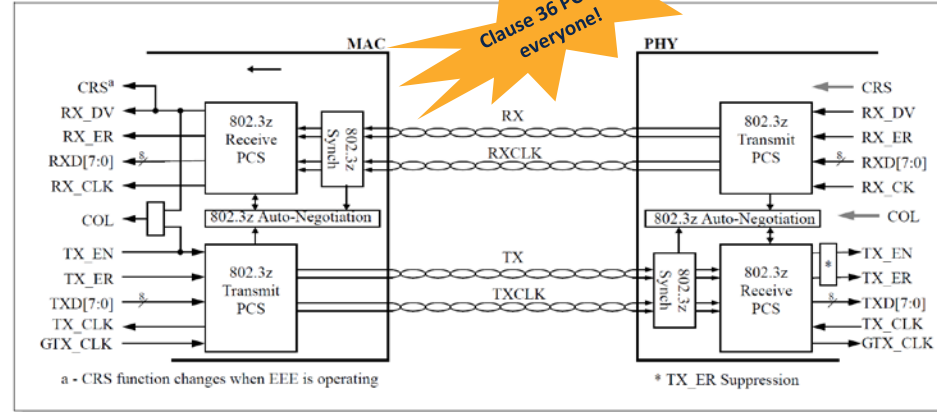
RX_DV	RX_ER	RXD<3:0>	Indication
0	0	0000 through 1111	Normal inter-frame
0	1	0000	Normal inter-frame
0	1	0001	Assert LPI
0	1	0010	PLCA BEACON indication
0	1	0011	PLCA COMMIT indication
0	1	0100 through 1101	Reserved
0	1	1110	False Carrier indication
0	1	1111	Reserved
1	0	0000 through 1111	Normal data reception
1	1	0000 through 1111	Data reception with errors

# Cisco Specification Serial-GMII (aka SGMII)

## MII Score Card

Max Data Rate	1000 Mbit/s
Signal Count	4/port + 2 Mgmt
SerDes Max Rate	1.25 Gb/s
Clock Scheme	SerDes or Source Sync
Command Space	Large – Ordered Sets
Commands Assigned	8 Non-Idle Sets Defined
PLCA Support	No

## System Diagrams (SGMII Spec)



## PCS Scheme (Clause 36)

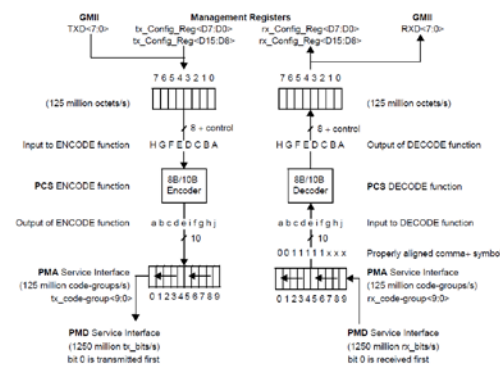


Figure 36-3—PCS reference diagram

## Commands (Clause 36)

Table 36-3—Defined ordered sets

Code	Ordered Set	Number of Code-Groups	Encoding
C/	<b>Configuration</b>		Alternating C1/ and C2/
C1/	Configuration 1	4	/K28.5/D21.5/Config_Reg <sup>a</sup>
C2/	Configuration 2	4	/K28.5/D2.2/Config_Reg <sup>a</sup>
I/	<b>IDLE</b>		Correcting I1/, Preserving I2/
I1/	IDLE 1	2	/K28.5/D5.6/
I2/	IDLE 2	2	/K28.5/D16.2/
<b>Encapsulation</b>			
R/	Carrier_Extend	1	/K23.7/
S/	Start_of_Packet	1	/K27.7/
T/	End_of_Packet	1	/K29.7/
V/	Error_Propagation	1	/K30.7/
<b>LPI</b>			
L1/	LPI 1	2	Correcting L11/, Preserving L12/
L11/	LPI 1	2	/K28.5/D6.5/
L12/	LPI 2	2	/K28.5/D26.4/

<sup>a</sup>Two data code-groups representing the Config\_Reg value.

One to Rule Them All!

We're tired of doing these!

# Cisco Specification Universal Serial GMII (aka USGMII)

## MII Score Card

**Max Data Rate** 1000 Mbit/s, with 8, 4, and 1 Port Modes

**Signal Count** 4/Octal PHY + 2 Mgmt

**SerDes Max Rate** 10.0, 5.0, 1.25 Gb/s

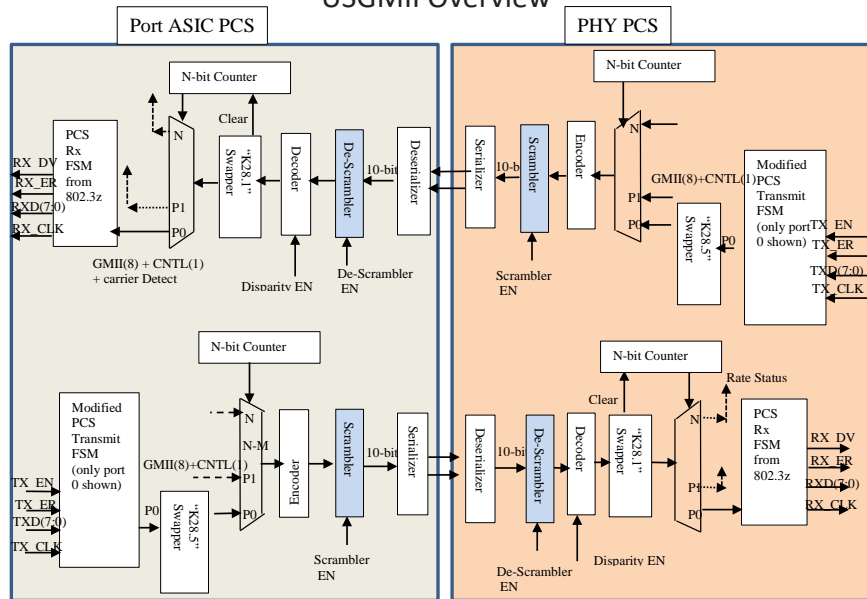
**Clock Scheme** SerDes

**Command Space** Large – Ordered Sets Packet Control Header

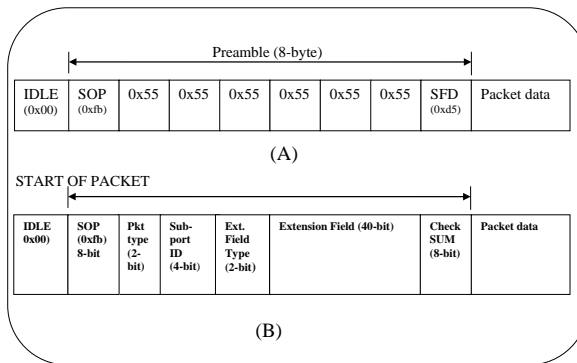
**Commands Assigned** K28.1 Reserved  
8 Non-Idle Sets Defined  
**PCH Packet Types**

**PLCA Support** No

## USGMII Overview



## Packet Control Header



## PCH Packet Types

- 00: Ethernet Packet with PCH
- 01: Ethernet packet, without PCH (packet information)
- 10: Idle Packet – Contains status data for a port – no packet data
- 11: Preemption Frame, aka Interspersing Express Traffic (IET) frame

**In-Band PTP Timestamps via Extension Field**

Motivating Factors in 802.3da  
and 802.3dg that Require a  
new MII

# Motivation

- 802.3dg wants a new MII
  - Needs to provide a modern single-port solution for 100 mbit/s data rates
  - Also need to solve multi-port applications to enable switch density
  - Ordered sets already proposed on top of existing MII to address gaps
- 802.3da also wants a new MII
  - Most issues from 802.3dg apply to 802.3da as well
  - PLCA over MII presents challenges
- We need consensus on the right place to do this work

# Market Considerations



# Market Stuff goes here

- Possible Topics
  - Implementation Complexity of High Pin Count Interfaces?
  - Challenges with existing four-pair/two-pair PHYs in existing applications?

***Feedback Requested***

- How much should go into this section? Should we keep it high level or get specific?

# Possible Path Forward Based on 802.3dg Straw Poll Results

# Implementation Rough Sketch

- Start with Cisco USGMII Specification
  - <https://developer.cisco.com/site/usgmii-usxgmii/>
- Use amended Clause 36 ordered sets with added PLCA support
- Update config register definitions
- Change rates to 1/10<sup>th</sup> USGMII data rates
  - Consider omitting scrambler
- Adopt SGMII-style source-synchronous clocking for lower complexity options:
  - Single-ended SDR data + 125 MHz Clock
  - Single-ended DDR data + 62.5 MHz Clock
  - Differential Data + Clock (at cost of 2x pins)
  - Differential Data + Clock Recovery (SerDes)

# Issue 1 – PLCA RS

- In theory, the Reconciliation Sublayer (RS) controls the PHY's PLCA-related actions from the host side of the MII
- In practice, backwards compatibility with non-PLCA MCUs in the market has driven PLCA into the PHY
- The success of PLCA-aware PHYs diminishes the market demand for PLCA signaling across the MII
- Standardized registers to manage PLCA-aware PHYs could be of value as part of the 802.3 standard

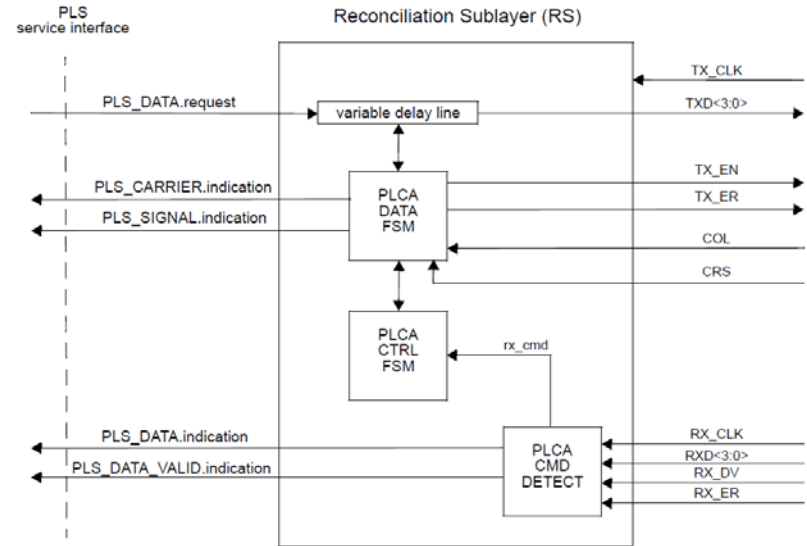
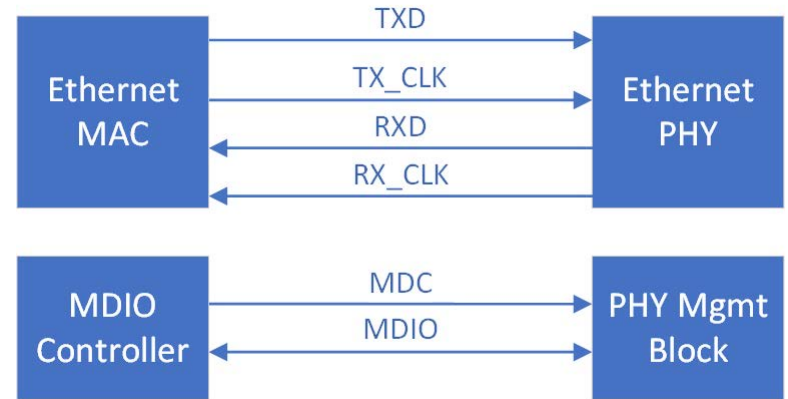


Figure 148–2—PLCA functions within the Reconciliation Sublayer (RS)

# Issue 2 – Single Port Interfaces

- Single Port Reduced Pin Interface
  - Competes with Open Alliance
    - SPI MAC/PHY Serial Interface
    - Three-Pin PMD Interface
  - More useful in 802.3dg than 802.3da due to ease of integration of a 10Base-T1S PHY in an MCU with external PMD
  - Could be useful for 4-pair 10/100 PHYs as well

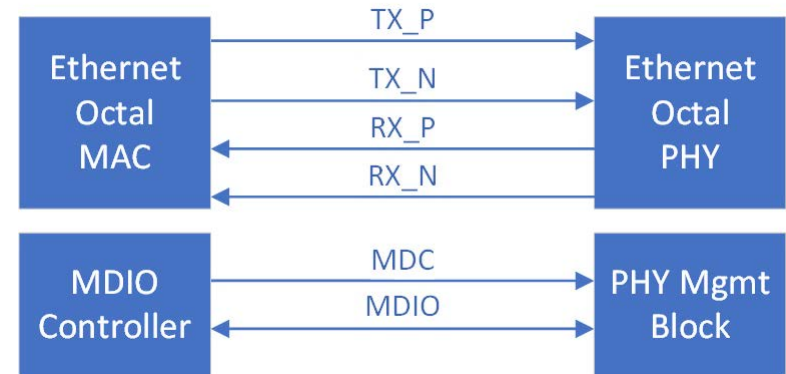
Single-Port Configuration



# Issue 3 – Multi-Port Interfaces

- Features to Consider
  - Slow SerDes / No SerDes
  - Variable Mux Ratio
    - 1-8 Ports / Interface
  - Embedded MDIO
  - Ordered Sets for Control
    - PLCA, LPI, Faults, Collisions, etc.
  - PTP Timestamping
  - Collision Notification
  - Preemption

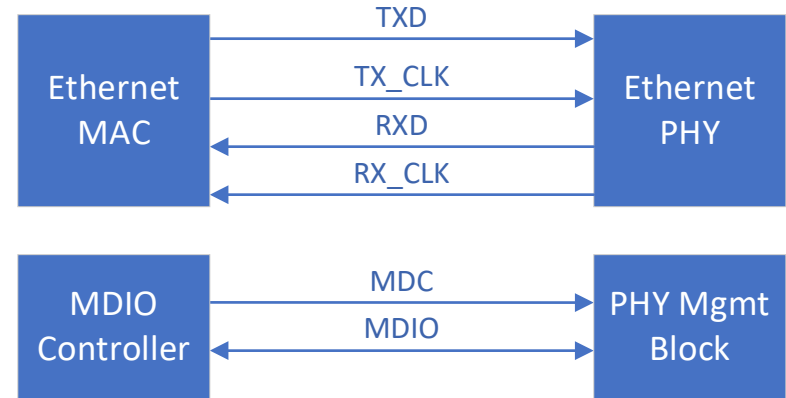
Multi-Port Configuration



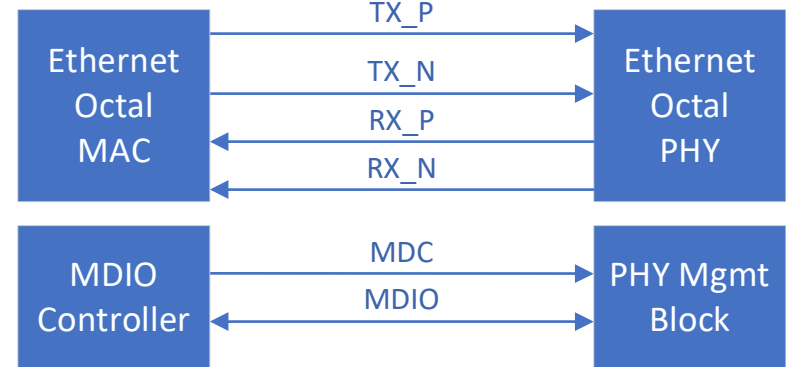
# Issue 4 – One Solution or Two?

- Should we have a single logical solution that scales from single to multi-port?
- Should we allow multiple electrical interfaces to enable hardware optimization?
- See following slides for an example of a single logical solution...

## Single-Port Configuration



## Multi-Port Configuration



# Supported Configurations Proposal A

Number of Data ports	Data Speed per port	Number of Parts	Maximum MII Data Rate (Mbps)	Comment
1-port	10M	1	12.5	One Port, 10 Mbit Only
10M				10 Mbps Data Payload Before 8b/10b Overhead
(USMII-Lite)				
1-port	10/100M	1	125	One Port
10/100M				100 Mbps Data Payload Before 8b/10b Overhead
(USMII)				
4-port	10/100M	4	500	Maximum of 4 ports
10/100M				400 Mbps Data Payload Before 8b/10b Overhead
(Q-USMII)				
8-port	10/100M	8	1000	Maximum of 8 ports
10/100M				800 Mbps Data Payload Before 8b/10b Overhead
(O-USMII)				

No In-Band Control Bandwidth Reservation



# Supported Configurations Proposal B

Number of Data ports	Data Speed per port	Number of Parts	Maximum MII Data Rate (Mbps)	Comment
1-port	10M	1	15.625	One Port, 10 Mbit Only
10M				10 Mbps Data Payload Before 8b/10b Overhead
(USMII-Lite)				2.5 Mbps In-Band Control Bandwidth Reserved
1-port	10/100M	1	156.25	One Port
10/100M				100 Mbps Data Payload Before 8b/10b Overhead
(USMII)				25 Mbps In-Band Control Bandwidth Reserved
4-port	10/100M	4	625	Maximum of 4 ports
10/100M				400 Mbps Data Payload Before 8b/10b Overhead
(Q-USMII)				100 Mbps In-Band Control Bandwidth Reserved
8-port	10/100M	8	1250	Maximum of 8 ports
10/100M				800 Mbps Data Payload Before 8b/10b Overhead
(O-USMII)				200 Mbps In-Band Control Bandwidth Reserved

Includes In-Band Control Bandwidth Reservation

Not another one!

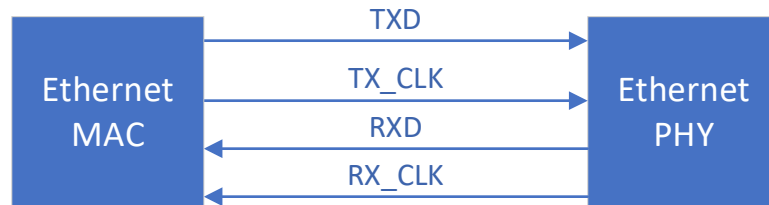
Make it stop!

## Proposal SPE-SMII and SPE-MP-SMII

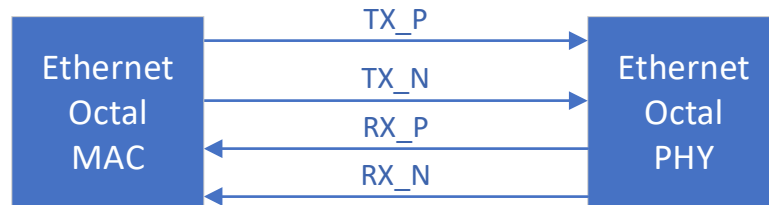
### MII Score Card

Max Data Rate	100 Mbit/s, with 8 and 1 Port Modes
Signal Count	<b>4 per PHY</b> + 2 Mgmt
Clock Scheme	SP - 125 MHz Source Sync Clock MP - 1.0 Gb/s SerDes
Command Space	Amended Clause 36 Ordered Sets, Packet Control Header
Features	<b>PTP Timestamp via PCH</b> <b>Preemption via PCH</b> <b>EEE via Ordered Sets</b> <b>PLCA via Ordered Sets</b>

### Single-Port Configuration



### Multi-Port Configuration



*Feedback Requested*

- What do we want to ask?

# Discussion and Straw Polls



The bridge to possible

# Specific Feedback Sought

- Clause 36 PLCA Ordered Set fix should be done in IEEE 802.3, but should it be part of .3dg or a one-off quick effort?
- Should MII Spec be done as an industry spec to accelerate the existing SPE market?
- Do we want to bump the multi-port SerDes to 1.25 Gb/s to enable in-band MDIO?
- Same question, but for single-port, source-synchronous interface by faster clock and/or DDR data transfer methods to enable in-band MDIO?
- Is using a common Clause 36 PCS coding scheme for both single and multi-port interfaces beneficial?
- Are we deluding ourselves in thinking the RS will be in charge of PLCA?
  - If so, should we pivot to a model where PHY-based PLCA is explicitly supported?

# Feature Requirement Straw Poll Summary

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation
PLCA Support

**Options:** Mandatory Feature, Optional Feature, Omit Feature

# Straw Poll Question

## Detailed Description

Features
<b>Control Bandwidth Reservation</b>
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation
PLCA Support

## Control Bandwidth Reservation

Should we allocate reserved bandwidth for guaranteed delivery of control messages in the MII data stream?

### Options:

**Yes**, Mandatory Feature 15

**Yes**, Optional Feature 2

**No**, Omit Feature 3

**Abstain**, No Opinion 13

# Straw Poll Question Detailed Description

Features
Control Bandwidth Reservation
<b>Embedded MDIO</b>
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation
PLCA Support

## Embedded MDIO

Should we support embedding MDIO transactions in the MII data stream?

### Options:

**Yes, Mandatory Feature 16**

**Yes, Optional Feature 5**

**No, Omit Feature 3**

**Abstain, No Opinion 10**



# Straw Poll Question Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
<b>PTP Timestamping</b>
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation
PLCA Support

## PTP Timestamping

Should we support communicating PTP timestamps in the MII data stream?

### Options:

**Yes, Mandatory Feature 14**

**Yes, Optional Feature 9**

**No, Omit Feature 1**

**Abstain, No Opinion 10**

# Straw Poll Question

## Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
<b>Frame Preemption (802.1Q IET)</b>
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation
PLCA Support

## Frame Preemption (802.1Q IET)

Should we support communicating information necessary to manage frame preemption in the MII data stream?

### Options:

**Yes**, Mandatory Feature 9

**Yes**, Optional Feature 4

**No**, Omit Feature 1

**Abstain**, No Opinion 18

# Straw Poll Question

## Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
<b>Energy Efficient Ethernet (LPI)</b>
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation
PLCA Support

## Energy Efficient Ethernet (LPI)

Should we support communicating control data necessary to enable EEE in the MII data stream?

### Options:

**Yes**, Mandatory Feature 15

**Yes**, Optional Feature 8

**No**, Omit Feature 0

**Abstain**, No Opinion 8

# Straw Poll Question

## Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation
PLCA Support

## Two-Pair 10/100 PHY Compatibility

Should we support communicating management information necessary to support legacy 10/100 four-pair PHYs in the MII data stream?

### Options:

**Yes, Mandatory Feature 15**

**Yes, Optional Feature 2**

**No, Omit Feature 2**

**Abstain, No Opinion 15**

# Straw Poll Question Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
<b>Half-Duplex Operation (COL)</b>
Half-Duplex Late Collision Frame Correlation
PLCA Support

## Half-Duplex Operation (COL)

Should we support communicating status messages necessary to manage collisions in the MII data stream?

### Options:

**Yes**, Mandatory Feature 15

**Yes**, Optional Feature 4

**No**, Omit Feature 2

**Abstain**, No Opinion 11

# Straw Poll Question

## Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
<b>Half-Duplex Late Collision Frame Correlation</b>
PLCA Support

## Half-Duplex Late Collision Frame Correlation

Should we support correlating collisions with frames to improve systems with high latency MII schemes?

### Options:

**Yes, Mandatory Feature 4**

**Yes, Optional Feature 4**

**No, Omit Feature 4**

**Abstain, No Opinion 24**

# Straw Poll Question Detailed Description

Features
Control Bandwidth Reservation
Embedded MDIO
PTP Timestamping
Frame Preemption (802.1Q IET)
Energy Efficient Ethernet (LPI)
Four-Pair 10/100 PHY Compatibility
Half-Duplex Operation (COL)
Half-Duplex Late Collision Frame Correlation
<b>PLCA Support</b>

## PLCA Support

Should we support PLCA control in the MII data stream?

### Options:

**Yes**, Mandatory Feature 13

**Yes**, Optional Feature 1

**No**, Omit Feature 1

**Abstain**, No Opinion 17

# Feature Requirement Straw Poll Results Summary

Features	Mandatory	Optional	Omit	Abstain
Control Bandwidth Reservation	15	2	3	13
Embedded MDIO	16	5	3	10
PTP Timestamping	14	9	1	10
Frame Preemption (802.1Q IET)	9	4	1	18
Energy Efficient Ethernet (LPI)	15	8	0	8
Four-Pair 10/100 PHY Compatibility	15	2	2	15
Half-Duplex Operation (COL)	15	4	2	11
Half-Duplex Late Collision Frame Correlation	4	4	4	24
PLCA Support	13	1	1	17

**Options:** Mandatory Feature, Optional Feature, Omit Feature



# Path Forward Decisions with Straw Poll Results

- What's the right construct?
  - New MII (e.g. USGMII)
  - Extender Sublayer (e.g. XAUI)
- Where should this be done?
  - IEEE 802.3 New Project 8
  - IEEE 802.3dg 6
  - Industry Specification 4
  - Nowhere 1
  - Abstain 8
- I would support defining at least the aspects of an MII relevant to 100mbit full duplex in 802.3dg.
  - Support 18
  - Oppose 2
  - Abstain 11
- Can IEEE complete this in a timely manner so as to compete with other industry standards?