Proposal for 100BASE-T1L PMA Training

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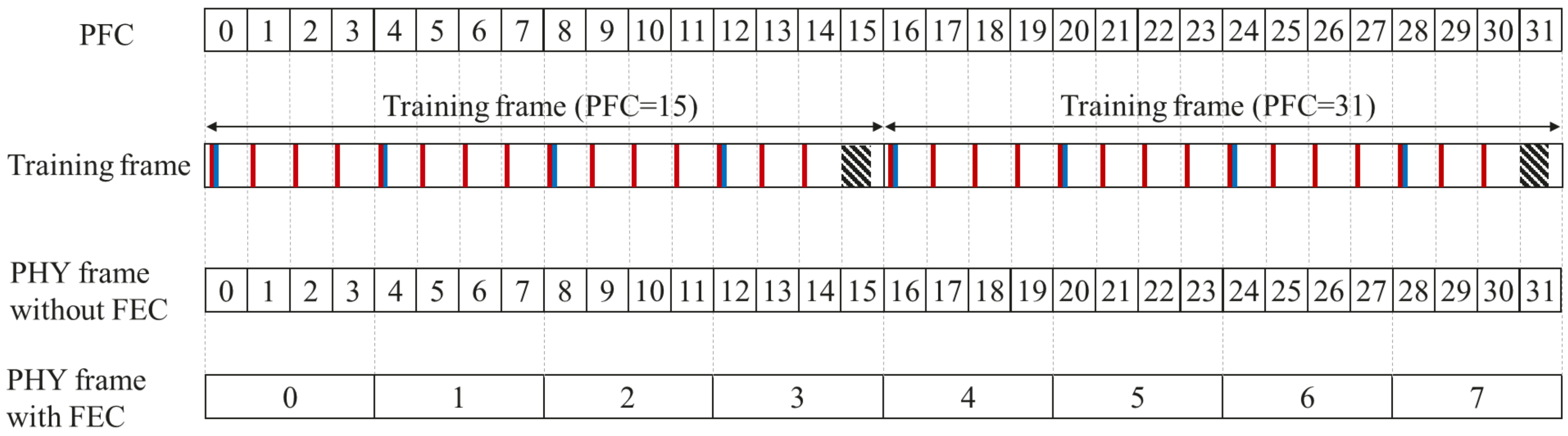
Introduction

- Data-mode PCS is almost in place. The details of PMA training including training frame with InfoField, scrambling, and line coding have been discussed.
  - Tingting_3dg_02a_16_09_2024
  - Tingting_3dg_01_29_10_2024
  - Riesco_3dg_01a_09172024
  - Riesco_3dg_02_10292024
- This presentation gives a proposal for PMA Training frame, the scrambler, and line coding used for 100BASE-T1L.

PMA Training Frame

- The PMA training frame follows a similar approach as in Clauses 97. During PMA training, the training frame with indicators is used to establish the PHY frame and block boundaries.
- Each training frame is composed of 16 partial PHY frames. Each partial PHY frame has 128 bits, aligned with the PHY frame without FEC.
- All the bits in each training frame are zero except:
  - The 2nd bit (in red) in the first 15 partial PHY frames is set to 1 to align the PHY frame without FEC.
  - The third bit (in blue) in every four partial PHY frames is set to 1 to align the PHY frame with FEC.
  - The 12-octet InfoField (in black shadow) in the 16th partial PHY frame.



PHY Control Infofield

- A 12-octet InfoField is used during PMA training to exchange PHY Control information between link partners.
  - Same approach as in Clauses 97, 149, and 165
  - Small modifications to the Slave Message field and PHY capability bits
- 1-octet Message field (octet 7):
  - Master: same as in Clauses 97, 149 and 165.
  - Slave: The timing_lock_OK<4> bit is replaced by a reserved bit (set to 0), since the Slave starts transmission after timing lock and the PCS synchronization.

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10			octets 11/12
0xBB	0xA7	0x00	PFC24	Message	MSG24	MSG24	MSG24	CRC16

Master Message Field

PMA_state <7:6>	loc_rcvr_status <5>	en_slave_tx <4>	reserved <3:0>
00	0	0	0000
00	0	1	0000
00	1	1	0000
01	1	1	0000

Slave Message Field

PMA_state <7:6>	loc_rcvr_status <5>	reserved <4:0>
00	0	00000
00	1	00000
01	1	00000

PHY Control Infofield

- 3-octet PHY capability bits (octets 8/9/10) sent during TRAINING (PMA_state=00) are modified to include RS-FEC and sequence order set support capability (Riesco_3dg_02_10292024).
- 3-octet DataSwPFC24 (octets 8/9/10) bits, indicating the partial PHY frame count when the transmitter switches from PAM2 to PAM3, are used during COUNTDOWN (PMA_state=01).
  - ➢ DataSwPFC24 shall be set to an integer multiple of 16.

PMA_state = 00

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	PHY Capability Bits	CRC16

PMA_state = 01

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

PHY capability bits (PMA_state = 00)

Octet 8	Octet 9	Octet 10							
7 6 5 4 3 2 1 0	7 6 5 4 3 2 1 0	7	6	5	4	3	2	1	0
Reserved		SEQen	EEECntrl[1:0]		RSen	Reserved			

- SEQen advertises support for sequence ordered sets
- EEECntrl[1:0] advertises the EEE abilities
- RSen advertises support for RS-FEC

Riesco_3dg_02_10292024

PMA Training Scrambling

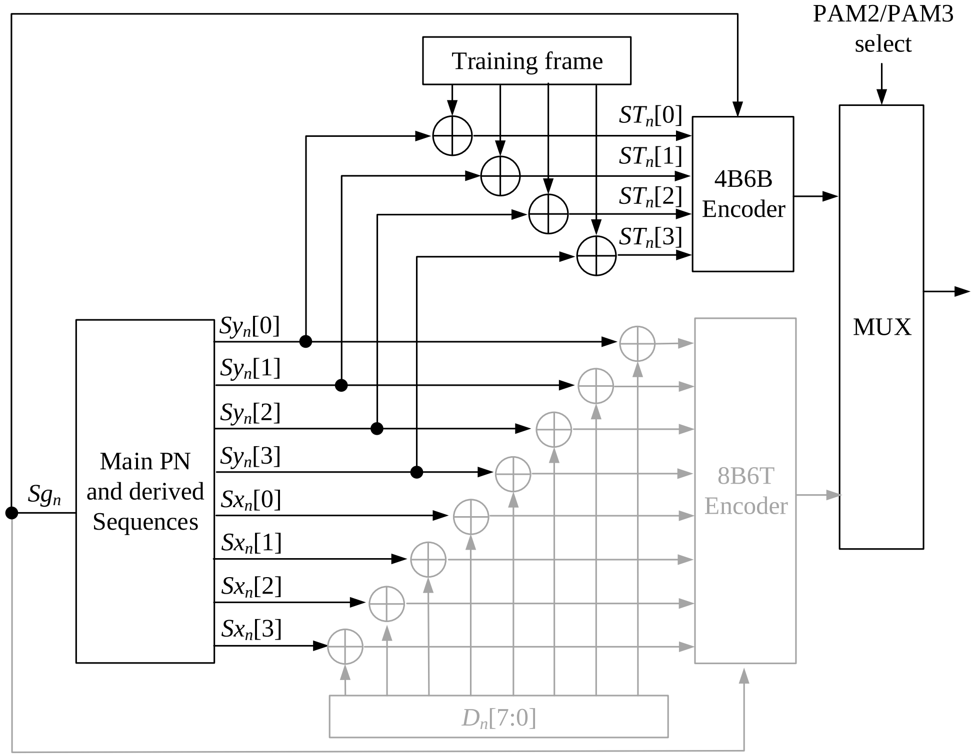
- The training frame with embedded InfoField is XORed with the scrambler bits $Sy_n[3:0]$ (also used in data mode) in nibble width. The 1st bit of each partial PHY frame is scrambled with $Sy_n[0]$ (i.e. $Scr_n[0]$).
  - Setting the 1st bit of the first 15 partial PHY frames to zero, makes $Scr_n[0]$ available on the 1st bit of each nibble except the InfoField, facilitating scrambler synchronization.
  - Each partial PHY frame (128 bits) corresponds to 32 nibbles.
- The scrambled nibble $ST_n[3:0]$ during training can be expressed as:

$$ST_n[3] = \begin{cases} Sy_n[3] \oplus \text{InfoField}_{(4n+3 \bmod 128)} & 480 \le (n \bmod 512) \le 503 \\ Sy_n[3] & \text{otherwise} \end{cases}$$

$$ST_n[2] = \begin{cases} Sy_n[2] \oplus \text{InfoField}_{(4n+2 \bmod 128)} & 480 \le (n \bmod 512) \le 503 \\ Sy_n[2] \oplus 1 & \text{else if } (n \bmod 128) = 0 \\ Sy_n[2] & \text{otherwise} \end{cases}$$

$$ST_n[1] = \begin{cases} Sy_n[1] \oplus \text{InfoField}_{(4n+1 \bmod 128)} & 480 \le (n \bmod 512) \le 503 \\ Sy_n[1] \oplus 1 & \text{else if } (n \bmod 32) = 0 \\ Sy_n[1] & \text{otherwise} \end{cases}$$

$$ST_n[0] = \begin{cases} Sy_n[0] \oplus \text{InfoField}_{(4n \bmod 128)} & 480 \le (n \bmod 512) \le 503 \\ Sy_n[0] & \text{otherwise} \end{cases}$$



PMA Training Modulation: 4B6B PAM2

- The scrambled nibble $ST_n[3:0]$ is mapped to PAM2 6-tuple with bounded running disparity during PMA training.
- Each of the 16 4-bit values is associated with one of the non-negative disparity (NND) 6-tuples, shown in the right table.
  - Each NND 6-tuple has a unique complementary code group (not in the table), generated by negating each element of the NND 6-tuple. Both 6-tuples correspond to the same 4-bit value.
- The running disparity (RD) at the transmitter is controlled as follows:
  - If both RD and the disparity of the 6-tuple associated with the 4-bit value are positive, then the 6-tuple is negated before transmission.
  - If RD is zero or the disparity of the 6-tuple corresponding to the 4-bit value is zero, then the random bit Sg_n determines whether to negate the 6-tuple before transmission.
  - RD is recomputed after transmission of each 6-tuple.

4 bits input	**NND PAM2 6-tuples**					
0000	-1	1	-1	1	-1	1
0001	-1	-1	1	1	-1	1
0010	-1	1	1	1	1	1
0011	1	-1	1	-1	1	1
0100	-1	1	-1	1	1	-1
0101	1	1	1	-1	1	-1
0110	-1	1	1	-1	-1	1
0111	-1	1	-1	-1	1	1
1000	1	1	1	1	-1	-1
1001	-1	-1	-1	1	1	1
1010	-1	-1	1	-1	1	1
1011	-1	-1	1	1	1	-1
1100	1	1	-1	1	1	-1
1101	-1	1	1	-1	1	-1
1110	-1	1	1	1	-1	-1
1111	1	1	-1	-1	1	1

PAM2 Training Sequence

- With the proposed 4B6B coding, the spectrum of the generated PAM2 training sequence has no spurs and is very close to that of 8B6T PAM3 (see Tingting_3dg_01_29_10_2024).
- Time-domain simulation (Tingting_3dg_01_29_10_2024) also demonstrates that:
  - In the case of 500m transmission, the Rx equalizer works stably when the transmit signal is switched from 4B6B PAM2 to 8B6T PAM3, regardless of the equalizer operation mode (traditional or PR).
  - The convergence speed for PAM2 is much faster than PAM3. This enables fast startup/retrain and leaves more time for the other device functions (e.g. processor) to start.

Conclusion

- The proposed PMA Training frame uses similar approach as in Clauses 97, 149, and 165 with small modifications:
  - Composed of 16 partial PHY frames with 128 bits per partial frame
    - The 2nd bit of each partial PHY frame except the InfoField and the third bit in every four partial PHY frames are set to 1, to establish PHY frame alignment and facilitate scrambler synchronization.
  - InfoField in the 16th partial PHY frame:
    - timing_lock_OK not used in the Salve Message field
    - modified PHY capability bits in Riesco_3dg_02_10292024
    - DataSwPFC24 is an integer multiple of 16
  - Scrambled with the data-mode scrambler bits ($Sy_n[3:0]$) in a nibble width before being mapped to PAM2 6-tuple
- Using PAM2 sequence for 100BASE-T1L PMA training, as in Clause 97, 149, and 165
  - 4B6B coding ensures the transmitted spectrum has no spurs and is close to that of 8B6T PAM3.
  - PAM2 enables more robust DSP with fast convergence, and stable performance during format switching regardless of the equalizer operation mode. It makes fast startup/retrain and long-distance transmission achievable.

Q & A