Further Consideration on PHY Control

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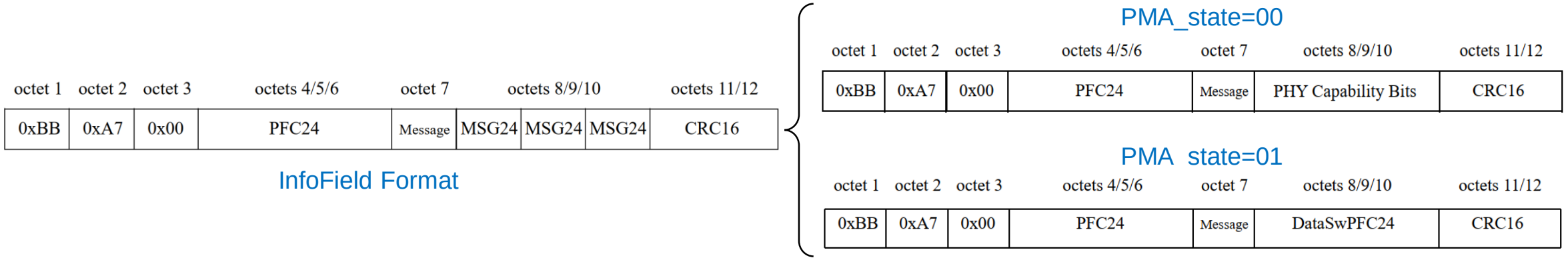
Introduction

- The Master/Slave architecture is commonly used in SPE standard, where the Master uses a local clock while the Slave recovers the clock from the received signal sent by the Master.
- There is a concern about the reliability of the timing lock for the Slave in 802.3dg. Brian proposes to use timers with different transmit signaling (SEND_U/SEND_F) during training (Curran_3dg_01_01152025).
- This presentation shares a simple scheme by using SENT_T as most SPE standards do with times introduced during TRAINNING to ensure stable timing lock. A Capability Exchange state (PMA_state=10) is added between TRAINING and COUNTDOWN to exchange the capability bits and PFC24 after both receivers are fully up to improve training efficiency.

Traditional InfoField for PHY Control

- For existing SPE standards with PAM2 for training and higher-order PAM (e.g. PAM3/PAM4) for data, the training frame with an embedded InfoField is used for PHY control and frame boundary establishment.
- The InfoField consists of a 3-octet SFD (0xBBA700), 3-octet PFC24, 1-octet Message, 3-octet MAG24 and 2-octet CRC16.
  - The 1-octet Message contains the information on the PMA state (PMA_state), local receiver status, and Slave transmission control or timing-lock result.
  - PMA_state=00 represents TRAINING. During this stage, the Master and Slave train the receiver and exchange PHY capability. The 3-octet MSG24 in the InfoField carries PHY capability bits.
  - PMA_state=01 represents COUNTDOWN. DataSwPFC24 in the 3-octet MSG24 is used for format switching.
  - PMA_state=10/11 are reserved.



Proposed InfoField Format

- InfoField is still used for PHY Control during PMA training. PFC24 and COUNTDOWN are also used.
  - DataSwPFC24 ensures reliable, fast, and accurate recognition of format switching, due to the repeated transmission of the fixed value and sufficient SNR margin bought by PAM2.
  - PFC24 with an increasing step of 16 also improves the robustness to bit errors.
- Considering the link may not be stable during the first stage of TRAINING, PHY capability bits and PFC24 are transmitted after the receiver is fully up (loc_rcvr_status=OK and rem_rcvr_status=OK).
- Similar to Clauses 97, 149, and 165, the 2-bit PMA_state (Oct7<7:6>) in the Message field indicates different states during PMA training.
  - PMA_state=00: TRAINING. Only SFD, Message, and CRC16 are transmitted.
  - PMA_state=10: CAPABILITY EXCHANGE. PFC24 and PHY Capability bits are transmitted.
  - PMA_state=01: COUNTDOWN, switching from PAM2 to PAM3.

PMA_state=00 (TRAINING)

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	RSV	Message	RSV	CRC16

PMA_state=01 (COUTDOWN)

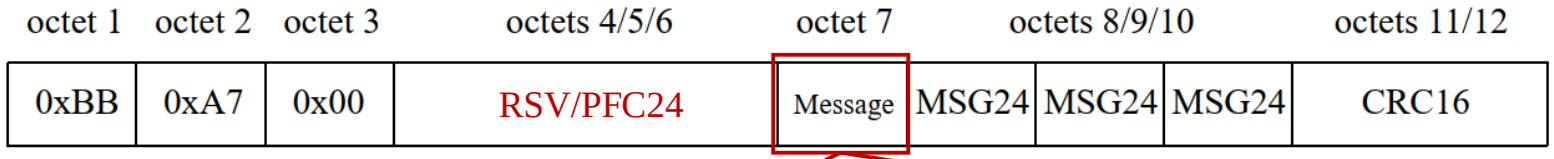
octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	DataSwPFC24	CRC16

PMA_state=10 (CAPABILITY EXCHANGE)

octet 1	octet 2	octet 3	octets 4/5/6	octet 7	octets 8/9/10	octets 11/12
0xBB	0xA7	0x00	PFC24	Message	PHY Capability Bits	CRC16

Updated Message Field

- The 1-octet Message is similar to Clauses 97, 149, and 165, but adds PMA_state=10 for Master and Slave. The timing_lock_OK<4> bit is replaced by a reserved bit 0.
  - The Slave starts transmission after min_slave_slient_timer and en_slave_tx=1, ensuring sufficient time for Master echo canceller training, and Slave equalizer training and timing locking.
  - Master_init_timer and Slave_init_timer are used during the first stage of training to ensure sufficient time for stable timing lock.



Master Message Field

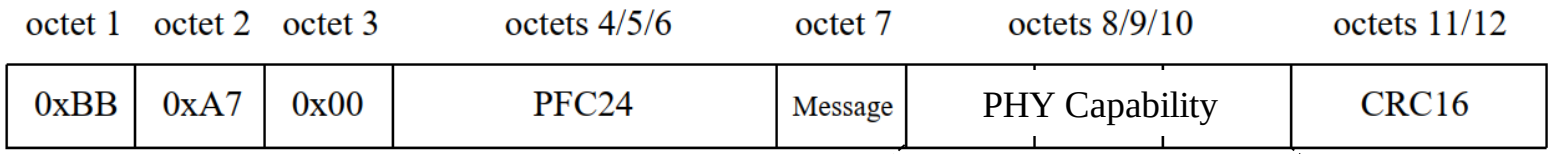
PMA_state <7:6>	loc_rcvr_status <5>	en_slave_tx <4>	reserved <3:0>
00	0	0	0000
00	0	1	0000
00	1	1	0000
10	**1**	**1**	**0000**
01	1	1	0000

Slave Message Field

PMA_state <7:6>	loc_rcvr_status <5>	reserved <**4**:0>
00	0	**0**0000
00	1	**0**0000
10	**1**	**00000**
01	1	**0**0000

PHY Control Infofield

- During CAPABILITY EXCHANGE (PMA_state=10), 3-octet PFC24 (octets 4/5/6) and PHY capability bits (octets 8/9/10) are sent.
  - PHY Capability includes the RS-FEC, EEE, LPI, and sequence order set support capability. The SLAVE shall synchronize its partial PHY frame count (PFC24) to the MASTER's PFC24.
- 3-octet DataSwPFC24 during COUNTDOWN (PMA_state=01) shall be set to an integer multiple of 16.



Riesco_3dg_02_10292024

Octet 8								Octet 9								Octet 10							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Reserved																SEQen	EEECntrl[1:0]		RSen	Reserved			

- SEQen advertises support for sequence ordered sets
- EEECntrl[1:0] advertises the EEE abilities
- RSen advertises support for RS-FEC

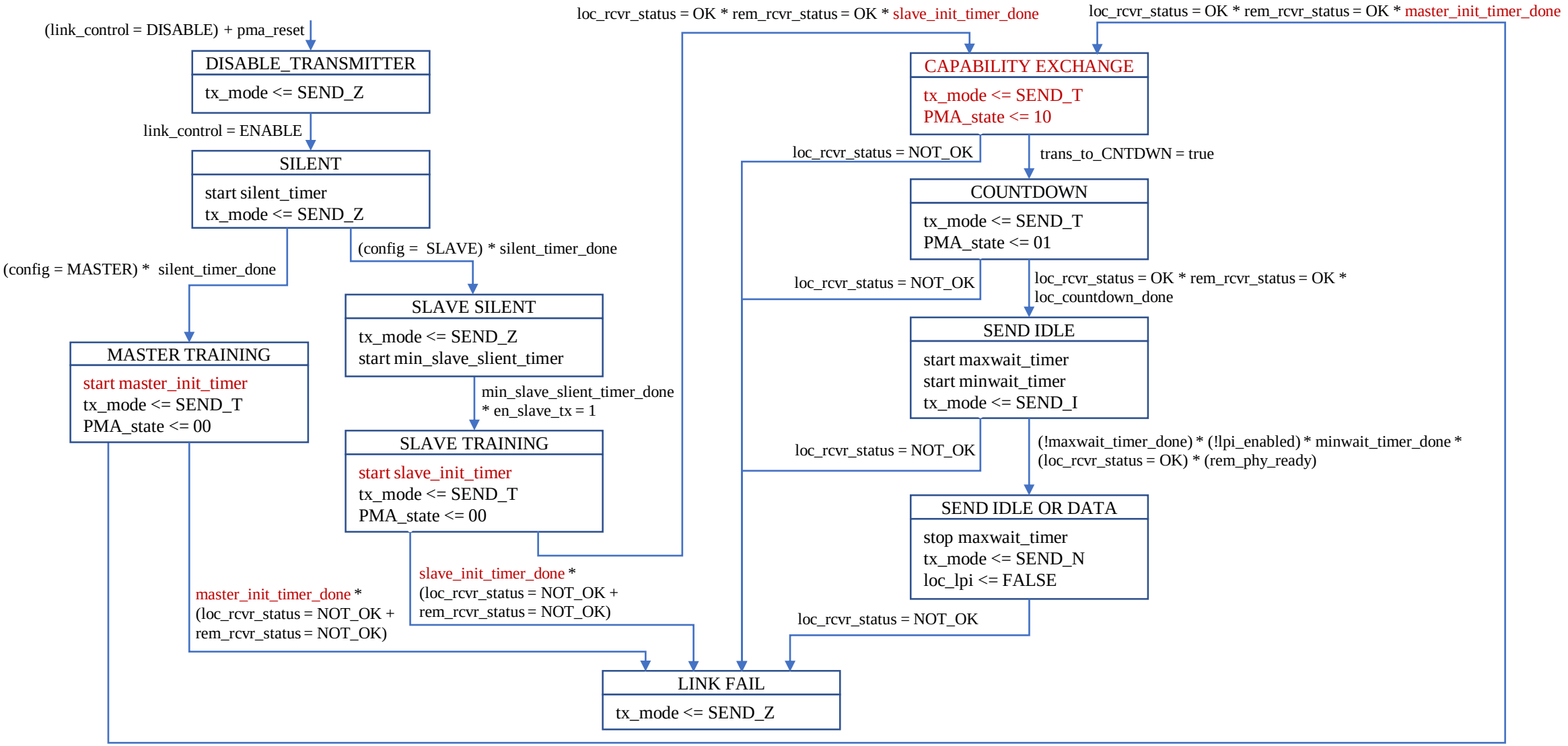
Transmit Signaling

- **SEND_Z:** transmission of zero code groups in the DISABLE_TRANSMITTER state, SILENT state, SLAVE_SILENT state and LINK_FAIL state.
- **SEND_T:** transmission of PAM2 code groups in MASTER/SLAVE TRAINING state, CAPABILITY EXCHANGE state, and COUNTDOWN state. The PAM2 sequence is generated using from 4B6B encoding and the nibble-wise scrambled training frame.
- **SEND_I:** transmission of PAM3 Idle code groups in SEND IDLE state. The PAM3 symbols are generated using 8B6T with 8N/(8N+1) block corresponding to the idle mode with loc_phy_ready = TRUE/FALSE.
- **SEND_N:** transmission of PAM3 symbols in SEND IDLE OR DATA state. The PAM3 symbols are generated using 8b6T with 8N/(8N+1) block representing normal MII Data Stream, Control Information, or idle.

State Diagram Parameters

- **silent_timer:** A timer used to determine the amount of time the PHY Control state diagram stays in the SILENT state. The timer shall expire 1 ms ± 1 µs after being started.
- **min_slave_slient_timer:** A timer used to determine the minimum amount of time the PHY Control state diagram stays in the SLAVE_SILENT state. The timer shall expire 10 ms ± 10 µs after being started.
- **master_init_timer:** A timer used to determine the amount of time the PHY Control state diagram stays in the MASTER_TRAINING state. The timer shall expire 50 ms ± 10 µs after being started.
- **slave_init_timer:** A timer used to determine the amount of time the PHY Control state diagram stays in the SLAVE_TRAINING state. The timer shall expire 40 ms ± 10 µs after being started.
- **minwait_timer:** A timer used to determine the minimum amount of time the PHY Control state diagram stays in the SEND_IDLE state. The timer shall expire 5 ms ± 5 µs after being started.
- **maxwait_timer:** A timer used to limit the amount of time during which a receiver dwells in the SEND_IDLE state. The timer shall expire 10 ms ± 5 µs after being started.
- **trans_to_CNTDWN:** This variable indicates whether a valid InfoField containing PHY capability bits has been received.
- **loc_countdown_done:** This variable is set to false when the PHY Control state diagram is in the DISABLE_TRANSMITTER state and is set to true immediately after transmitting the last bit of the DataSwPFC24–1 partial PHY frame.

PHY Control State Diagram



Conclusion

- PHY Control for 100BASE-T1L is similar to Clauses 97, 149, and 165, using InfoField with partial frame counter (PFC24).
  - PFC24 and DataSwPFC24 allows reliable, fast, and accurate recognition of format switching and is more robust to bit errors due to the regular value and transmitting PAM2.
- To improve training success probability, timers are introduced to Master and Slave TRAINING state (PMA_state=00), ensuring sufficient time to achieve stable timing lock.
  - The timing_lock bit in the Slave Message field can be replaced by a reserved bit 0.
- After both receivers are fully up, the capability bits and PFC24 are transmitted to improve training efficiency. The CAPABILITY EXCHANGE state (PMA_state=10) is added between TRAINING and COUNTDOWN.
  - As long as one valid InfoField containing PHY capability bits is received, it moves to COUNTDOWN.
  - DataSwPFC24 can be greatly reduced to e.g. 128.

Q & A