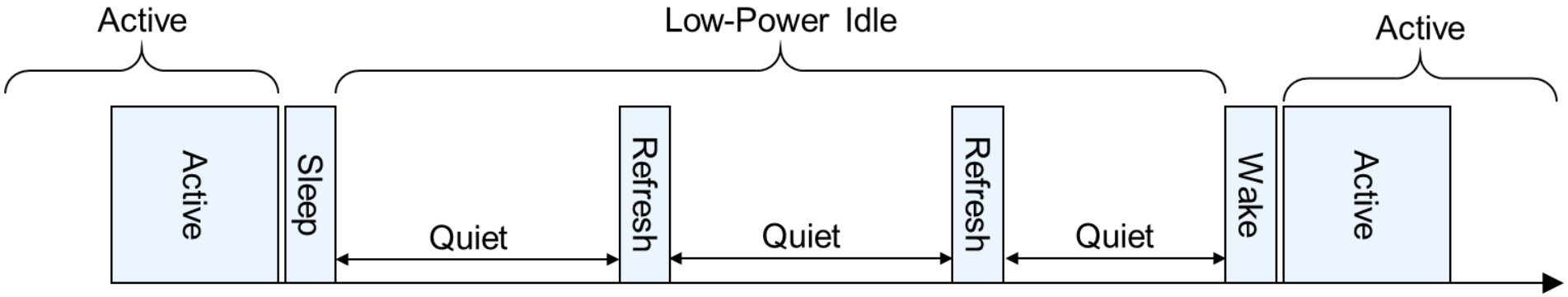
Proposal for EEE Signaling

Tingting Zhang
Huawei Technologies

Optional EEE Capability

- Using a similar approach as in Clause 97,149, and 165
- EEE abilities are advertised using EEECntrl bits (octet10<6:5> of InfoField) during TRAINING (PMA_state=00).
  - LPI is only entered when EEECntrl<1:0> bits are set to 1 for both Master and Slave.
  - Each direction of the link can enter and exit LPI mode independently.
- EEE LPI operation:
  - The alert signal is not used (same as Clause 97).
  - Transitions to and from the LPI mode are controlled using sleep and wake signaling.



Sleep

- the encoded 8N+1 blocks containing only LPI_IDLE
- ending at the PHY frame boundary
- conventional duration of multiple PHY frames
  - With FEC taken into account, the duration should be $4m$ partial PHY frames.
  - Should ensure enough redundancy for RX detection

LPI Signaling

- Within the LPI mode, PHYs use a repeating quiet-refresh cycle.
- During the quiet period, the transmitter passes zero symbol to the PMA.
- PAM2 symbols, enabling simple filter coefficient updates and timing recovery for both the local and remote PHYs, are used as the refresh signal.
  - Same as in Clause 149 and 165
  - PAM2 refresh symbols are generated from the scrambled training frame with 4B6B encoding (Tingting_3dg_01_29_10_2024).
    - all zeros for the Infofield
    - The 4th bit of each training nibble before scrambling is set to 1 to indicate that LPI refresh is insufficient to maintain reliable operation of the receiver.

$$ST_n[3] = \begin{cases} Sy_n[3] \oplus 1 & if \text{ insufficient SNR} \\ Sy_n[3] & \text{otherwise} \end{cases}$$

Infofield=0s ➡

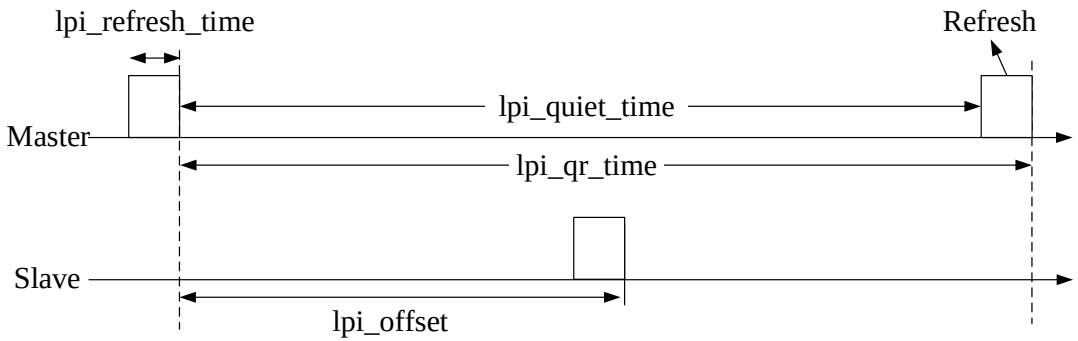
$$ST_n[2] = \begin{cases} Sy_n[2] \oplus 1 & \text{else if } (n \bmod 128) = 0 \\ Sy_n[2] & \text{otherwise} \end{cases}$$

$$ST_n[1] = \begin{cases} Sy_n[1] \oplus 1 & \text{else if } (n \bmod 32) = 0 \\ Sy_n[1] & \text{otherwise} \end{cases}$$

$$ST_n[0] = Sy_n[0]$$

Quiet/Refresh

- The quiet-refresh (QR) cycle is established from the Master partial PHY frame Count (PFC24) during PMA Training. The SLAVE synchronizes its PFC24 to MASTER within 1 partial PHY frame during link-up.
- The start of the SLAVE QR cycle is delayed from the MASTER by nearly half of the QR cycle. This offset is commonly multiple FEC frames.
- The Quiet time (T_Q) is a trade-off between power saving and timing preserving. The Refresh time (T_R) should be long enough for Echo/Equalizer update and scrambler synchronization.
  - A duty cycle $T_R/(T_R+T_Q)$ of less than 5% is reasonable for 100BASE-T1L.



PHY Type	T_Q (µs)	T_R (µs)	Duty Cycle $T_R/(T_R+T_Q)$
10BASE-T1L	6000	250	4%
100BASE-TX	20000	200	0.99%
1000BASE-T1	84.95	1.44	1.67%
1000BASE-T	20000	198	0.98%
2.5GBASE-T1	121.6	1.28	1.04%
5GBASE-T1	60.8	0.64	1.04%
10GBASE-T1	30.4	0.32	1.04%
25GBASE-T1	31.616	0.3328	1.05%

Wake Signal

- the encoded 8N+1 blocks containing only IDLE
- ending at the PHY frame boundary
- The duration of the wake signal can be the same as that of the sleep signal.
  - Same as Clause 97, 149, and 165

Conclusion

- EEE uses a similar approach as in Clause 97,149, and 165.
- No alert signal
  - Same as Clause 97
- the encoded 8N+1 blocks containing only LPI_IDLE/IDLE for the Sleep/Wake signal
  - the same duration ($4m$ partial PHY frames) for both signals
  - Same as Clause 97, 149, and 165
- a refresh duty cycle of less than 5%
- PAM2 symbols sent as the refresh signal
  - Same as Clause 149 and 165
  - generated from the scrambled training frame with 4B6B encoding
  - The 4th bit of each training nibble before scrambling is set to 1, to indicate that LPI refresh is insufficient to maintain reliable operation of the receiver.

Q & A