PCS Proposal for 802.3dg

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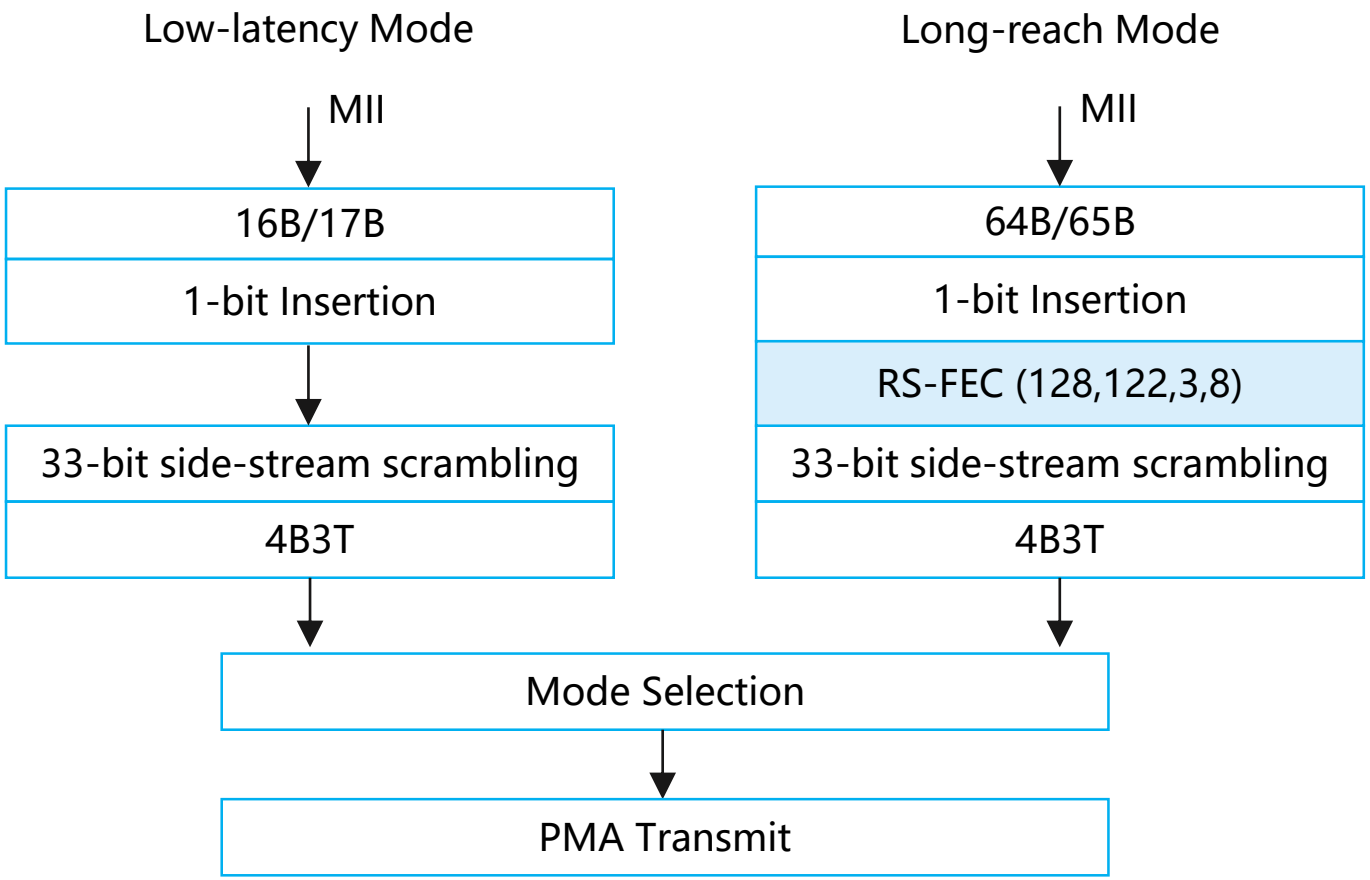
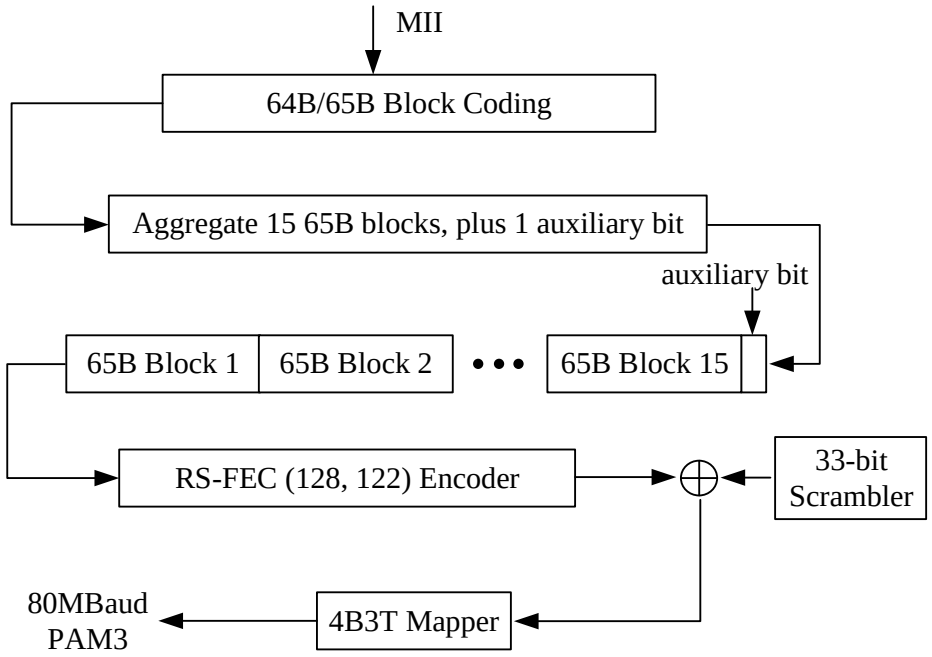
Proposed dual-mode PCS architecture

- PCS for 500m (long-reach mode) and motion control (low-latency mode) uses 4B3T PAM3, achieving bounded disparity. The PCS overhead in both modes is 6.67%, giving the same symbol rate (80MBaud).

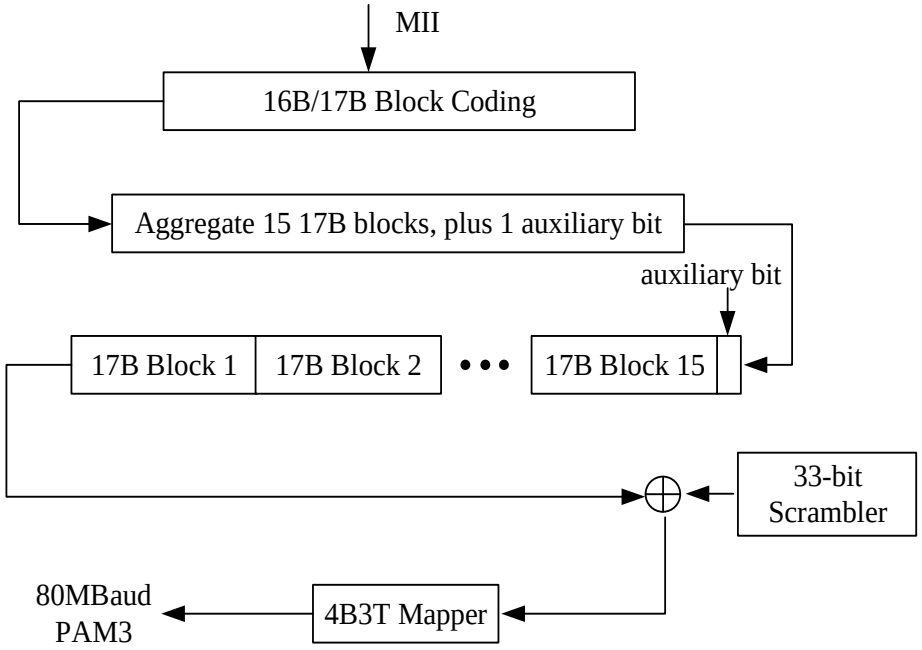


PCS transmit bit ordering (reverse order for receive)

- Long-reach mode with FEC: 1 auxiliary bit is inserted every 15 65b blocks before RS (128,122,3,8) encoder. The FEC frame is scrambled before 4B3T mapping.
- Low-latency mode without FEC: 1 auxiliary bit is inserted every 15 17b blocks before scrambling and 4B3T coding.
- The auxiliary bit can be used for vendor-specific communication (e.g. OAM).



Long reach



Low latency

PCS block coding

- As also presented in Lo_3dg_01_012524, 64B/65B and 16B/17B with similar coding principle as 80B/81B are used for long reach and low latency application, respectively.
- Since the control octet only appears in octet 1-8 for 64B/65B (N=8), the position pointer can be shorted to 3 bits (i.e. NEXT (n) [0:2]). This allows more control characters (i.e. TD [n] [4:7]) to be transmitted.
- 16B/17B for motion control application minimizes coding latency with acceptable overhead.

The 80B/81B block encoding is defined by the following pseudo-code, where N = 10.

```
N = number of GMII octets encoded into block. Octets numbered n = 0,1,2,…,N-1.
octet 0 is the first one presented on GMII.
TC[n] = 0 if octet n is data octet on GMII, 1 if octet n is control octet on GMII
TC[-1] = 1 by definition
TD[n][0:7] = GMII octet n TXD[0:7] if TC[n] = 0
TD[n][5:7] = 010 - IPG (loc_phy_ready = OK), 101 - LPI, 001 - TX Error, 000 - IPG
(loc_phy_ready = NOT OK) if TC[n] = 1. TD[n][0:4] is undefined.
B[0:8N] is the 8N+1 block. Bit 0 transmitted first.
OR(n) = Bitwise OR of TC[n:N-1]
NEXT(n)[0:3] = bit position of lowest bit in TC[n:N-1] that is a 1. Bit 3 is MSB.
NEXT(n)[4] = 0 if Bitwise SUM of TC[n:N-1] = 1, else 1

B[0] =              OR(0)
B[8n+1:8n+4] =      TD[n][0:3] - if OR(n) = 0
                    NEXT(n)[0:3] - if OR(n) = 1 AND TC[n-1] = 1
                    TD[n-1][3:6] - if OR(n) = 1 AND TC[n-1] = 0
B[8n+5] =           TD[n][4] - if OR(n) = 0
                    NEXT(n)[4] - if OR(n) = 1 AND TC[n-1] = 1
                    TD[n-1][7] - if OR(n) = 1 AND TC[n-1] = 0
B[8n+6:8n+8] =      TD[n][5:7] - if OR(n) = 0
                    TD[n][5:7] - if OR(n) = 1 AND TC[n] = 1
                    TD[n][0:2] - if OR(n) = 1 AND TC[n] = 0
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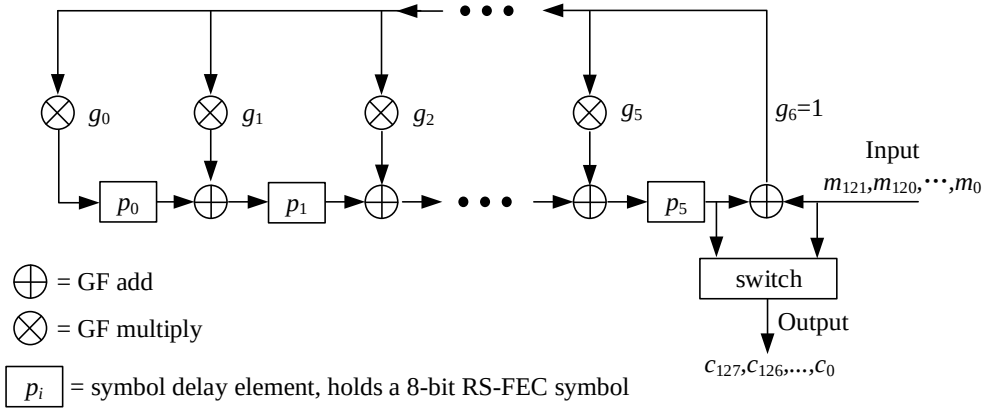
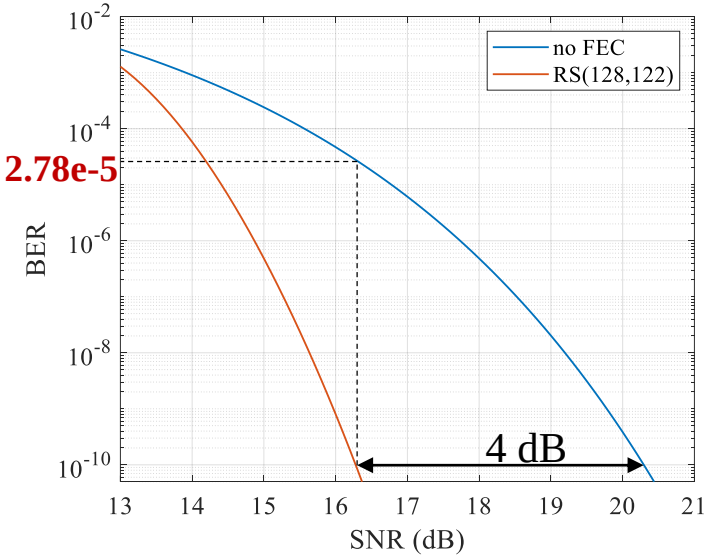
Source: Clause 97.3.2.2.4

RS-FEC encoder

- RS (128, 122) in GF(2^8) field with 6 parity symbols is only used for long-reach transmission. No FEC is used for low-latency mode.
  - FEC frame consisting of 122 message and 6 parity symbols, has duration of 9.6us.
  - 976 message bits is composed of 15 65B blocks and 1 auxiliary bit.
  - The RS encoder provides 3.79dB net coding gain (4-10*$\log_{10}$128/122) and tolerates 225ns burst. The BER threshold is 2.78e-5 for a given output BER of 1e-10.



RS-FEC (128, 122)	
g_0	38
g_1	227
g_2	32
g_3	218
g_4	1
g_5	63
g_6	1



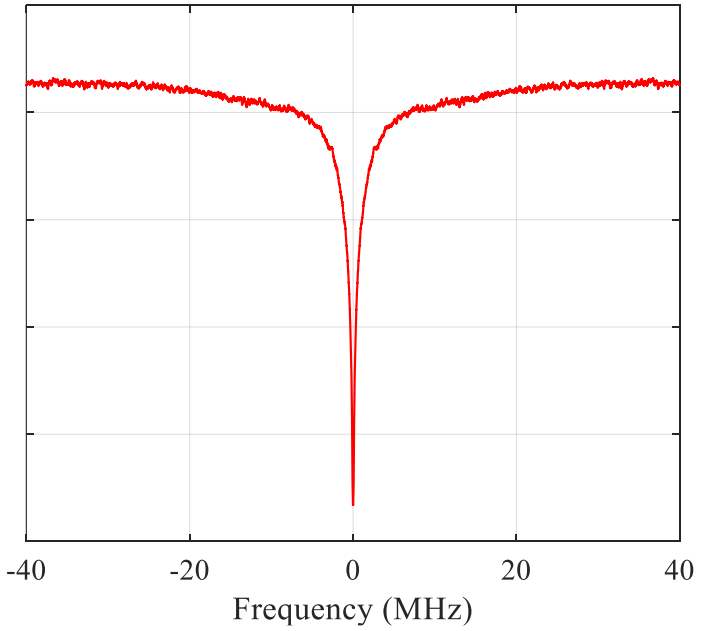
Scrambling

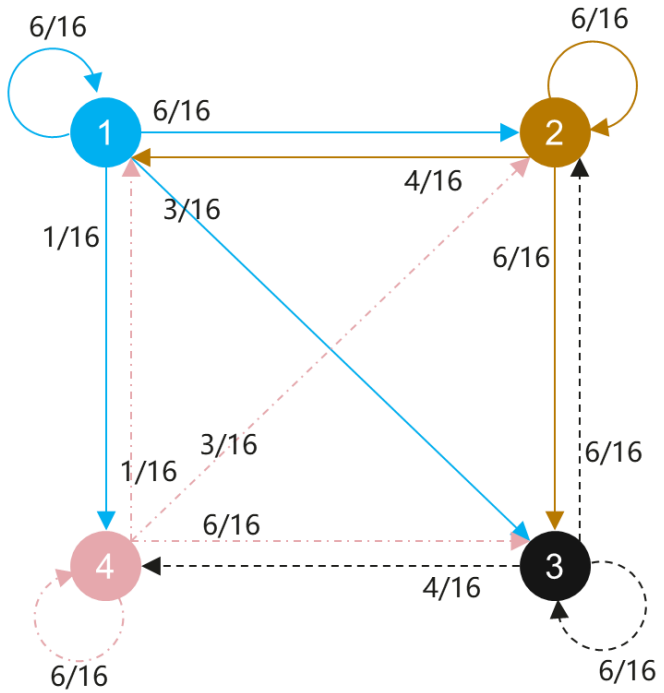
- Data mode for both long-reach and low-latency PCS uses 10BASE-T1L scrambler. The generator polynomial for Master and Slave are:
  - Master: $g_M(x) = 1 + x^{13} + x^{33}$
  - Slave: $g_s(x) = 1 + x^{20} + x^{33}$
- Training mode may also employ the same scrambler by resorting to reliable synchronization.

4B3T line coding

- Table 146-1 in Clause 146 is used for 4B3T encoding, which employs 26 code-groups to achieve bounded disparity. The redundant 3-tuple (0,0,0) is not utilized for data transmission.

3T code group				
Sum 0	Sum ±1	Sum ±2	Sum ±3	Total
7	6	3	1	17





Summary

- The proposed dual-mode PCS architecture based on 4B3T PAM3 achieves the same symbol rate of 80MBaud, simplifying PMA design and reducing PHY cost.

- RS(128,122) with 64B/65B block coding is used to ensure reliable long-distance transmission. For latency-sensitive application, 16B/17B is used without FEC. Both cases allocate 1-bit channel for vendor-specific communication.

- Can we achieve any PHY baseline (dual-mode PCS, block coding, FEC, scrambling, 1 auxiliary bit, and line coding) from this proposal?

Thank you!