100BASE-T1L PMA Training

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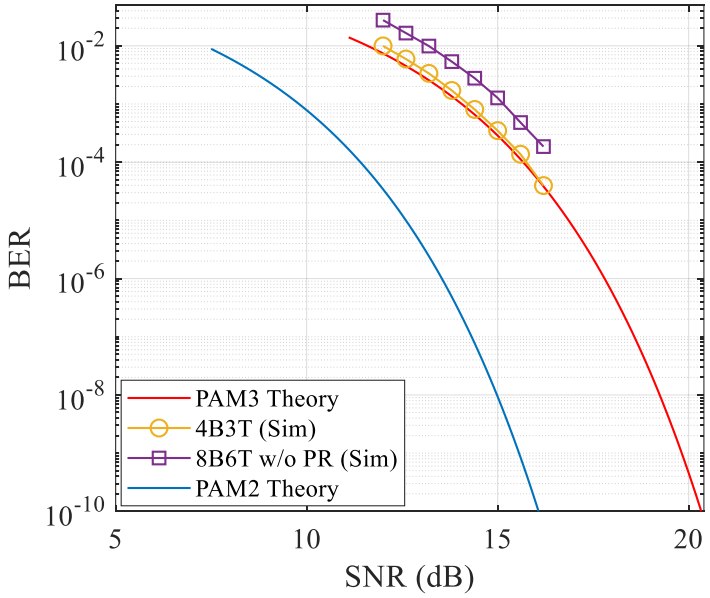
Introduction

- PHY baseline has been achieved up to now:
  - 8B6T PAM3 for data mode
  - Dual-mode PCS: 64B/65B + 1bit insertion + RS(128,122) + Side-stream scrambling + 8B6T for long reach, and 16B/17B + 1bit insertion + Side-stream scrambling + 8B6T for low latency.
- To do list:
  - the inserted 1 bit TBD (for vendor-specific communication is more favored)
  - data-mode scrambling
  - PMA training
- This presentation proposes a reliable and efficient PMA training scheme.

PM2 Training Sequence

- Training mode using 8B6T with blind PAM3 equalization does not achieve coding gain brought by partial response.
- In the case of EFT event or long-reach transmission, PAM3 suffers from more burst errors, resulted from either EFT or DFE. This impacts scrambling synchronization and InfoField acquisition. As a result, training efficiency is decreased, leading to increased startup or link up time.
- PAM2 with ~4dB lower SNR requirement than PAM3, mitigates the error impact and allows fast convergence for Rx DSP. Therefore, it allows fast startup/retrain and also reduces the risk of training failure.



Other Considerations for PMA training

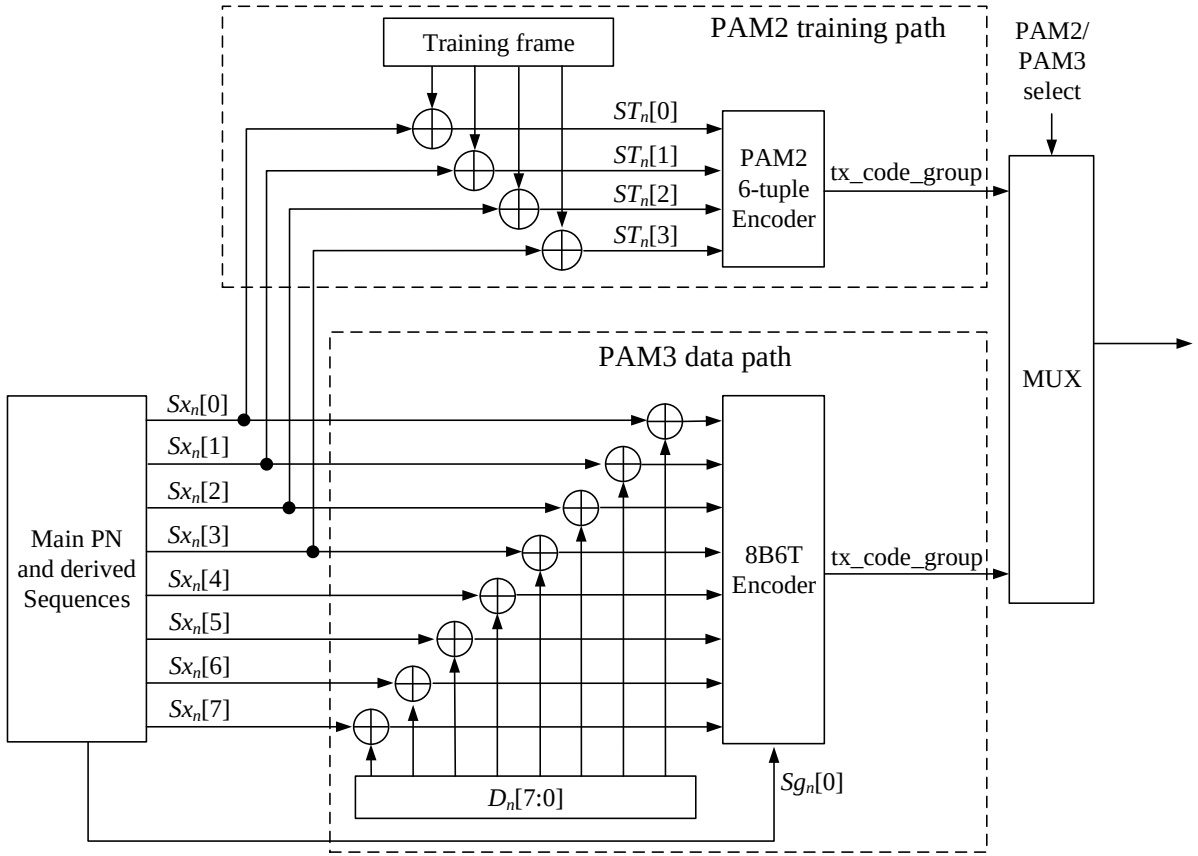
- Disparity-bounded line coding during training is mandatory for intrinsic safety application.
  - Better low-frequency suppression also enables low cost and compact inductors for power delivery.
  - Line coding used for automatic polarity detection and delimiting helps reduce startup time.
- Using the same side-steam scrambler as data mode has the following advantages:
  - less hardware complexity (one scrambler with one clock VS two scramblers with different clocks)
  - improved training efficiency, as exchanging data mode scrambler seed is not required.
- Training frame embedded with InfoField is required, since:
  - It provides an efficient method to establish PHY frame boundary without bandwidth requirement.
  - It allows more information (e.g. local receiver status, transmission indicator, PHY capability, LPI etc.) to be transmitted than the traditional method, which commonly swaps or inverts scrambler bits.

Overview of PMA Training Scheme

- Training frame with embedded InfoField for startup operation is scrambled with 4 bits $Sx_n[3:0]$. The four bits $Sx_n[3:0]$ are also used in data mode to decorrelate PHY frames.

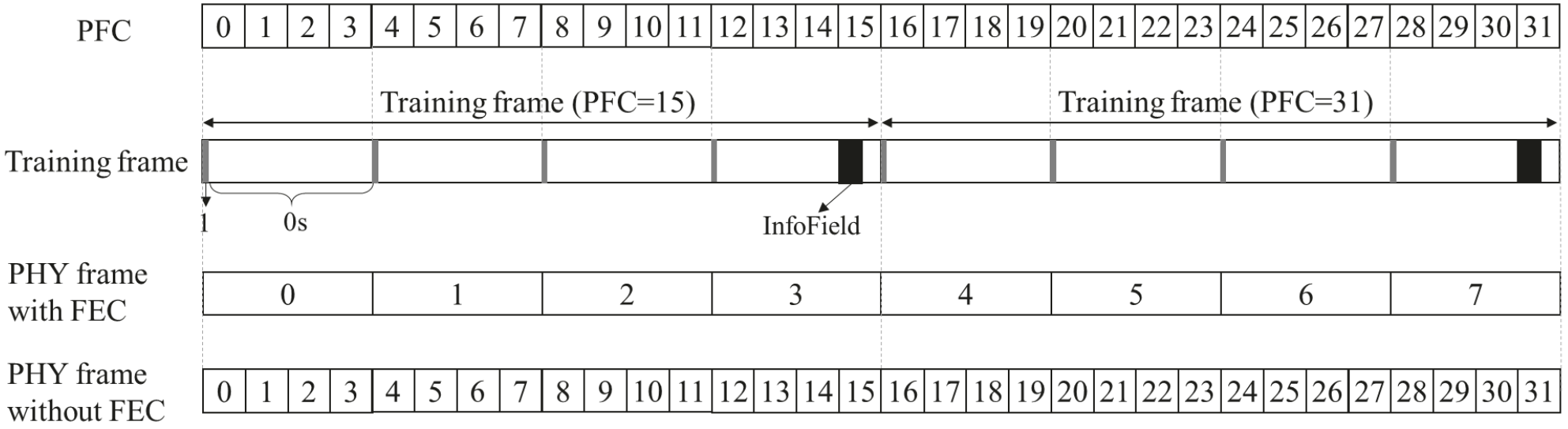
- Bits $Sx_n[3:0]$ generated from different combinations of the bits stored in 33bit LFSR have no short-term correlation.

- The scrambled bits $ST_n[3:0]$ are converted to a PAM2 6-tuple with strictly bounded disparity enabled by 4B6B encoder and delimiter generator.
  - The 4B6B encoder has maximum 4 consecutive 1s and -1s, while delimiter includes 5 consecutive 1s.
  - The delimiter can be used for fast symbol synchronization and automatic polarity detection.



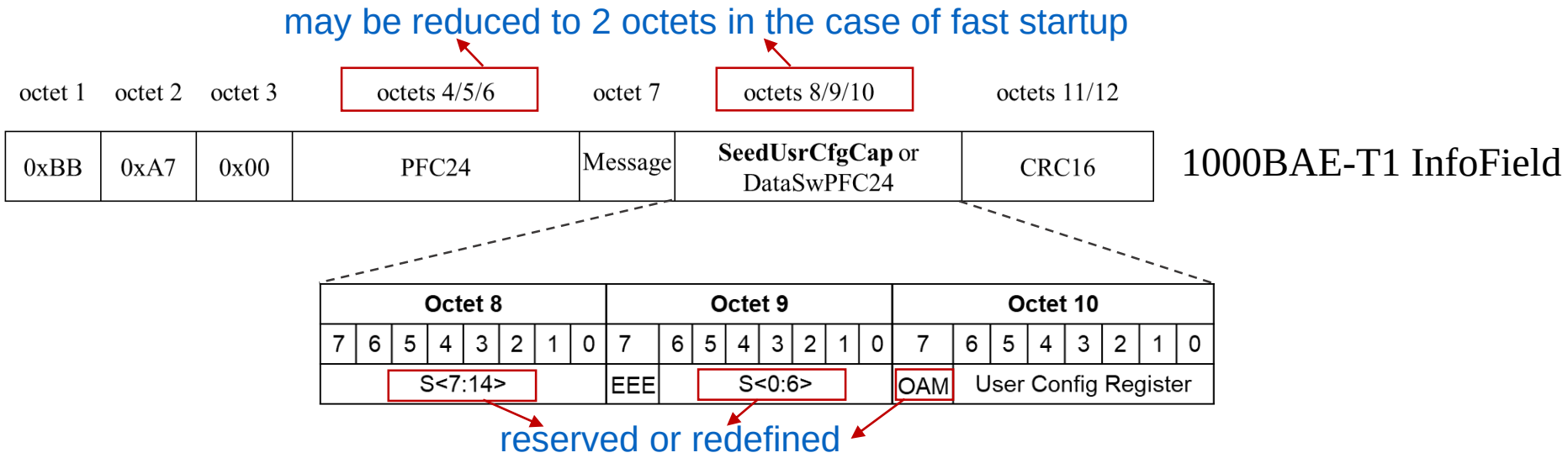
PMA Training Frame

- Training frame boundary corresponds to the boundary of multiple PHY frames, therefore, training frame synchronization allows establishment of PHY frame and block boundaries.
  - PHY frame length in the case of FEC is 1024 bits, which is four times longer than that in low-latency mode without FEC.
  - Each training frame with 2048 bits is composed of 16 partial PHY frames. Each partial PHY frame has 128 bits. InfoField is embedded in the last partial frame. 1st bit of every four partial frames, corresponding the FEC frame boundary, are inverted.



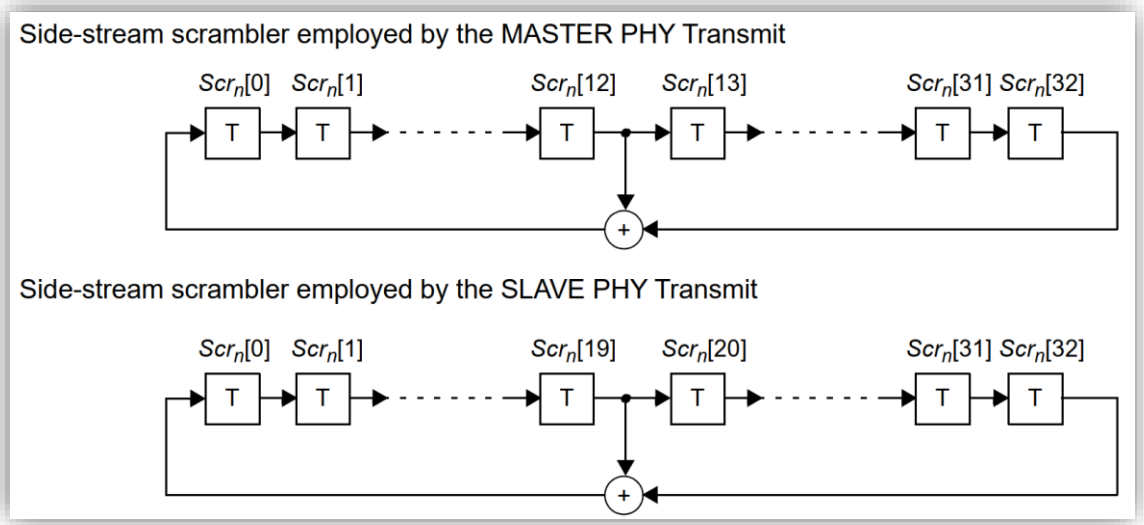
InfoField

- 12-octet InfoField is used in 1000BASE-T1 includes 3-octet SeedUsrCfgCap or DataSwPFC (depending on the 2b PMA_state in 1-octet Message).
  - 24-bit SeedUsrCfgCap consists of 2 PHY capability bits, 7 user configurable register bits, and 15-bit data mode scrambler seed.
- For 100BASE-T1L, both training and data mode uses 33-bit side-stream scrambler, therefore, data-mode scrambler seed is not required to be transmitted. Oct8<7:0> and Oct9<6:0> can be reserved or redefined for other usage. If OAM is not supported, Oct10<7> can be also reserved or redefined.
- Bit length for PFC24 and MSG24 (UsrCfgCap/DataSwPFC24) may be reduced to 2 octets, if startup time can be less than 100ms.



PMA Training Side-stream Scrambler

- Scrambler bits $Sx_n[3:0]$ are generated based on the bit $Scr_n[0]$ and an auxiliary generating polynomial $g(x) = x^3 \oplus x^8$.
  - The bit $Scr_n[0]$ for Master is generated with the polynomial $g_{\mathrm{M}}(x) = 1 + x^{13} + x^{33}$, while Slave uses $g_{\mathrm{S}}(x) = 1 + x^{20} + x^{33}$.
  - $Sx_n[0] = Scr_n[0]$
  - $Sx_n[1] = g(Scr_n[0]) = Scr_n[3] \oplus Scr_n[8]$
  - $Sx_n[2] = g^2(Scr_n[0]) = Scr_n[6] \oplus Scr_n[16]$
  - $Sx_n[3] = g^3(Scr_n[0]) = Scr_n[9] \oplus Scr_n[14] \oplus Scr_n[19] \oplus Scr_n[24]$



Scrambled training bits $ST_n[3:0]$

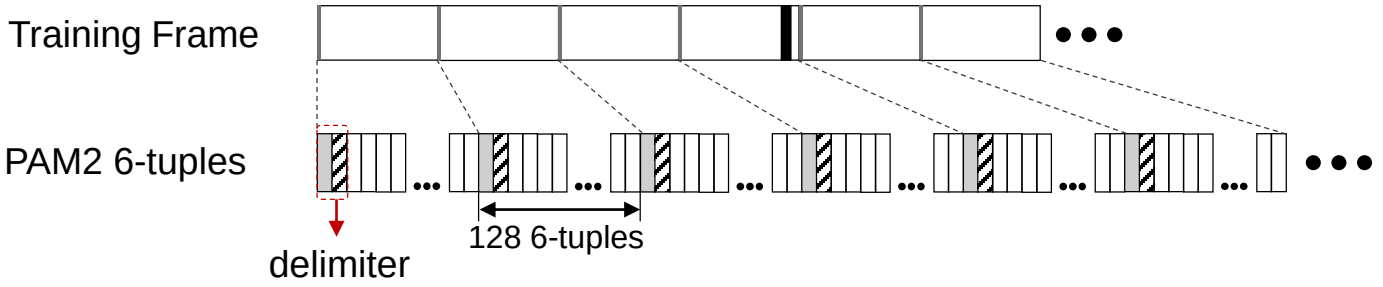
- The scrambled bits $ST_n[3:0]$ are generated as:
  - $ST_n[0] = \begin{cases} Sx_n[0] \oplus \text{InfoField}_{(4n \bmod 128)} & 480 \le (n \bmod 512) \le 503 \\ Sx_n[0] \oplus 1 & \text{else if } (n \bmod 128) = 0 \\ Sx_n[0] & \text{otherwise} \end{cases}$
  - $ST_n[1] = \begin{cases} Sx_n[1] \oplus \text{InfoField}_{(4n+1 \bmod 128)} & 480 \le (n \bmod 512) \le 503 \\ Sx_n[1] & \text{otherwise} \end{cases}$
  - $ST_n[2] = \begin{cases} Sx_n[2] \oplus \text{InfoField}_{(4n+2 \bmod 128)} & 480 \le (n \bmod 512) \le 503 \\ Sx_n[2] & \text{otherwise} \end{cases}$
  - $ST_n[3] = \begin{cases} Sx_n[3] \oplus \text{InfoField}_{(4n+3 \bmod 128)} & 480 \le (n \bmod 512) \le 503 \\ Sx_n[3] & \text{otherwise} \end{cases}$

PAM2 6-tuple Generation

- Scrambled bits $ST_n[3:0]$ are mapped to tx_code_group, consisting of six PAM2 symbols:

$$tx\_code\_group = \begin{cases} (-,-,-,+,+,+) & (n \bmod 128) = 0 \\ (+,+,-,+,-,-) & (n \bmod 128) = 1 \\ Encoder\_4B6B(ST_n[3:0]) & \text{otherwise} \end{cases}$$

- (- - - + + +) and (+ + - + - -) form the delimiter, corresponding to each partial frame. The delimiter includes 5 consecutive 1s, while 4B6B encoder outputs maximum 4 consecutive 1s or -1s.
  - 5 consecutive 1s can be used for symbol synchronization and polarity detection.
  - With the knowledge of delimiter and InfoField coding rule, the receiver can realize fast scrambler synchronization and recognize training frame boundary.



4B6B encoder

$ST_n[3:0]$	tx_code_group
0000	- - + - + +
0001	+ - + - + -
0010	- - + + - +
0011	- + + - + -
0100	- + + - - +
0101	+ - - + + -
0110	+ + - - + -
0111	+ + - - - +
1000	+ - + - - +
1001	+ - + + - -
1010	+ - - - + +
1011	+ - - + - +
1100	- + - + + -
1101	- + - + - +
1110	+ + - + - -
1111	- + - - + +

Conclusion

- PAM2 training sequence enables sufficient SNR margin and allows fast Rx DSP convergence. It enables fast startup and retrain as well as reduces the risk of training failure.
- PMA training frame approach is the same as Clauses 97, 149 and 165 (except the invert bit position). Synchronizing training frame with embedded InfoField allows establishment of PHY frame and block boundaries.
- Four scrambler bits $Sx_n[3:0]$, generated from different elements stored in 33bit LFSR, are used for training frame scrambling. These four bits have the maximum shift register sequence length of 2^{33}-1, but are not correlated in short term.
  - Bits $Sx_n[3:0]$ are also used in data mode for PHY frame decorrelation, reducing hardware complexity and saving startup time.
- PAM2 training sequence resulted from delimiter and 4B6B encoder has bounded disparity.
  - The delimiter with 5 consecutive 1s can be used for fast symbol synchronization and automatic polarity detection, improving training efficiency.

Q & A