Further consideration on 100BASE-T1L PHY

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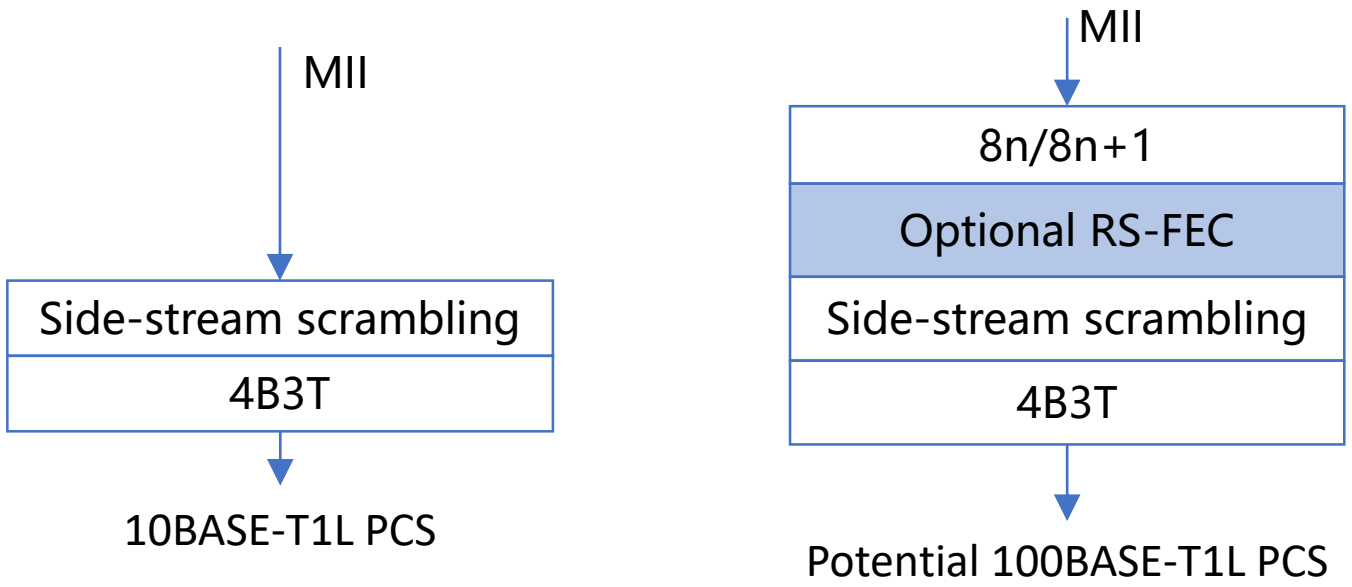
Reusing 4B3T in 100BASE-T1L PCS

- 4B3T in 10BASE-T1L achieves bounded disparity for intrinsic safety application. However, time-domain simulations (Murray_3dg_03122024, Tingting_3dg_12_03_2024) show insufficient SNR margin for 500m transmission.
- Coupled noise on cable impacts on the PAM3 decision, in the case of 1kV EFT and screw terminal connectors (Brychta_3dg_update_B_2024-Mar-09). The impact aggregates at 2kV EFT (IEC61000-4-4).
- FEC is a simple and direct method to correct both random and burst errors. Transmit signal level keeps the same (still PAM3), allowing easier analog/digital signal processing.
  - For latency-sensitive application, FEC can be bypassed.



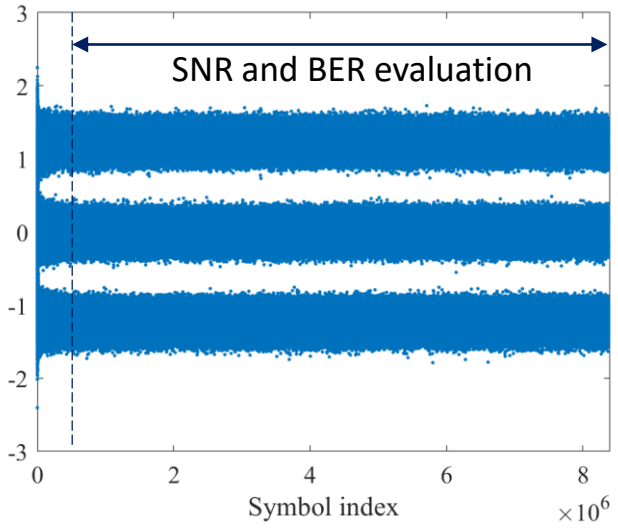
PCS block coding and FEC option

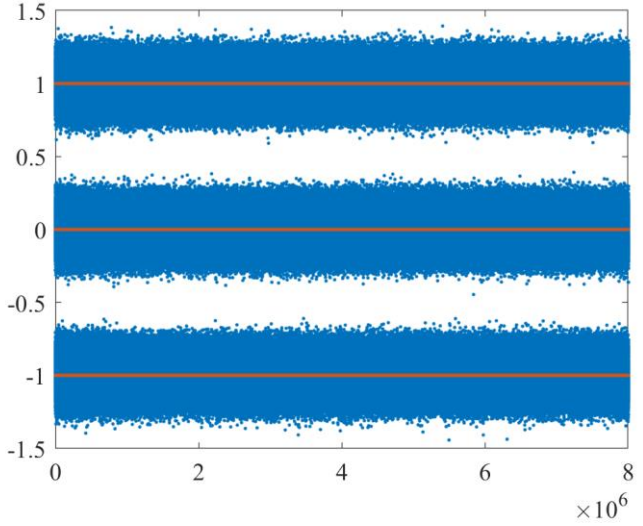
- For 500m transmission, RS (128, 122) in GF(2^8) field with 6 parity symbols provide 3.75dB net coding gain and tolerates 225ns burst, sufficient for both burst and random error correction. The signal bandwidth is slightly increased by 2.5MHz.
- When FEC is turned off, PCS function includes 64B/65B, scrambling and 4B3T mapping. The PCS latency is about 0.8us, still leaving 0.7us for PMA.
  - 16B/17B with the same coding principle as 64B/65B may be considered to further reduce PCS latency. For example, 1 bit is inserted every 15 17b blocks, symbol rate keeps the same ($100 \times \frac{(15\times17+1)}{15\times16} \times \frac{3}{4}$ =80MBaud) as the case with FEC.

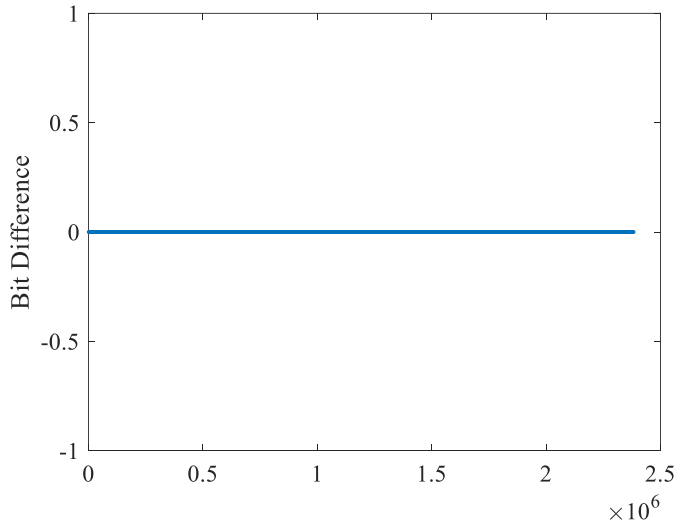
n	*k*	*t*	*m*	# OAM bits	# PCS blocks	Block coding	Frame (us)	Burst Error Protection (ns)	Symbol Rate (MBaud)	Overhead (%)	BERin @ BERout=1e-10	Net Coding Gain (dB)
103	99	2	8	0	24	32B/33B	7.68	149.13	80.47	7.29	6.73E-06	3.12
96	90	3	8	5	11	64B/65B	7.04	220	81.82	9.09	3.46E-05	3.80
102	98	2	8	4	12	64B/65B	7.68	150.59	79.69	6.25	6.77E-06	3.13
104	98	3	8	4	12	64B/65B	7.68	221.54	81.25	8.33	3.26E-05	3.79
110	106	2	8	3	13	64B/65B	8.32	151.27	79.33	5.77	6.43E-06	3.12
112	106	3	8	3	13	64B/65B	8.32	222.86	80.77	7.69	3.08E-05	3.78
118	114	2	8	2	14	64B/65B	8.96	151.86	79.02	5.36	6.14E-06	3.11
120	114	3	8	2	14	64B/65B	8.96	224	80.36	7.14	2.92E-05	3.77
126	122	2	8	1	15	64B/65B	9.6	152.38	78.75	5.00	5.87E-06	3.10
128	**122**	**3**	**8**	**1**	**15**	**64B/65B**	**9.6**	**225**	**80**	**6.67**	**2.78E-05**	**3.75**

Time-domain simulation for 80MBaud 4B3T PAM3

- Simulation parameters: 2.4Vpp, 12-bit DAC/ADC, -113.28dBm/Hz AWGN, 802.3dg baseline IL, 30-tap FFE and 5-tap DFE. Without FEC, the required SNR at BER of 10^{-10} for PAM-3 is 20.2 dB.
- Simulation results: 80MBaud 4B3T PAM3 achieves 19.6dB SNR, and no bit error is observed for 10^{7} bits. The 0.6dB SNR gap can be solved by RS (128, 122) with 3.75dB NCG, leaving some margin for burst errors.







Conclusion

- 4B3T adopted in 10BASE-T1L to limit the running disparity can be reused in 100BASE-T1L. Apart from the advantage of compatibility, the three–level signal (PAM3) also makes PHY design easier.

- To ensure BER <1e-10 after 500m transmission, FEC e.g. RS(128,122,3,8) with 3.75dB NCG and 225ns burst error correction capability can be used for 4B3T PAM3. The overall PCS overhead is ~6.7% and the signal bandwidth is only increased by 2.5MHz (from 37.5MHz to 40MHz).

- For latency-sensitive application, FEC can be bypassed. The symbol rate keeps the same, minimizing PHY cost.

Thank you!