PHY requirements

Why PHY delays matter!

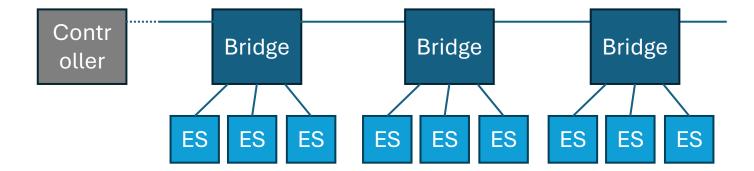
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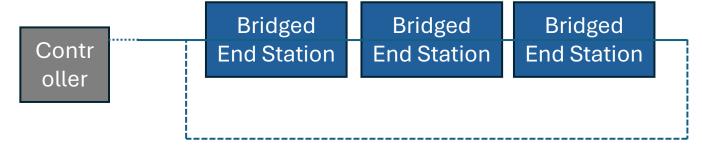
Markets and Topologies

- Process automation
 - Often tree topology



- Factory automation
 - Often linear or ring topology

- Machine automation
 - Often linear or ring topology



Performance impact of PHY delays

- Tree topology
 - The PHY delay of an end station only applies once in the communication between end station and controller
- Linear or ring topology
 - The PHY delay of a bridged end station applies for each hop in the communication between end station and controller
 - Example: Linear topology with 64 bridged end stations connect to a controller
 - ⇒The frame transmitted to the last end station is charged with a delay of ⇒63 hops, each with two PHY delays (receive and transmit)

Expected PHY delays An example

- IEC61158 / IEC61784 family of fieldbus standards
 - Example "IEC61158 Type 10 PROFINET"
 - The expected PHY delays (Table 88) are specified in the IEC61784-2-3:2023

Link Speed	RX delay ª	TX delay ^a	Jitter
10 Mbit/s – 1 Tbit/s	Mandatory: < 1 μs Recommended:< 500 ns	Mandatory: < 1 μs Recommended:< 500 ns	< 4 ns
10 Mbit/s Special case: 10BaseT1L	Mandatory: < 5 μs ^b Recommended:< 500 ns	Mandatory: < 5 μs Recommended:< 500 ns	< 4 ns
a If IEEE 802.3 defines lower values, then these definitions apply. Lower values mean lesser latencies. ^b 5 μs are equivalent to 6,25 octets at 10 Mbit/s.			

NOTE – Latency variation influences the synchronization quality!

Customer expectations

Existing machine and automation cell designs are not PHY dependent

 Introducing a new PHY for copper should not require changes in the machine and automation cell

 Roundtrip delays for motion or other high-speed applications shall still be achievable without new machine designs

Link diagnostics An example

- IEC61158 / IEC61784 family of fieldbus standards
 - Example "IEC61158 Type 10 PROFINET"
 - State machines use the information provided e.g. by ifOperStatus and ifAdminStatus controlling the behavior of the stations
 - ⇒ Stable link states (UP or DOWN) concurrently on both sides of the link are required no intermediate states used

NOTE – It is expected that during UP the nominal link speed is always provided!

Thanks

Questions