Cl **00** *SC* **0** *P* **0** *L* **0** # 581

Brown, Matt — Alphawave Semi

Comment Type **T** *Comment Status* **R** *AUI Generations (common)*

In the past, we have included all previously defined AUI for each new PHY type defined. Given that the PMA multiplexing methods were consistent this was simple to support. Now that we have switched to a different PMA muttiplexing method (RS-FEC symbol) things are getting more complicated.

SuggestedRemedy

For each PHY new 200 Gb/s per lane or higher PHY type, include only one or two previous generations of AUI. Specifically, the new PHY types defined in 802.3dj indication only 100 Gb/s per lane and 200 Gb/s per lane AUIs as being optional within a PHY. Perhaps, also include 50 Gb/s per lane AUIs as well.

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **00** *SC* **0** *P* **0** *L* **0** # 185

Brown, Matt — Alphawave Semi

Comment Type **T** *Comment Status* **A** *Machine Convention (bucket)*

Many state diagrams in this draft as well as in the base standard use the operator "++" to indicate that the variable be incremented by 1. However, this operator is never defined.

SuggestedRemedy

Import Clause 21 andà
Amend 21.5 to include definition of "++.
Delete the following from state diagram conventions in multiple clauses. "The notation used in the state diagrams follows the conventions of 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Import Clause 21 and.
Amend 21.5 to include definition of "++".
Delete the following from state diagram conventions in 175.2.6.1, 176.5.1.6, 177.6.1, 184.6.1, 176A.10.1.
"The notation ++ after a counter or integer variable indicates that its value is to be incremented."
Implement with editorial license.

Cl **1** *SC* **1.3** *P* **46** *L* **33** # 506

Dawe, Piers — Nvidia

Comment Type **TR** *Comment Status* **A** *MDI references (bucket)*

Add and update connector references as necessary. This is what is in 1.3:
SFF-8402, Rev 1.1, September 13, 2014, Specification for SFP+ 1X 28 Gb/s Pluggable Transceiver Solution (SFP28).
SFF-8432, Rev 5.1, August 8, 2012, Specification for SFP+ Module and Cage.
SFF-8436, Rev 4.8, October 31, 2013, Specification for QSFP+ 10 Gb/s 4X Pluggable Transceiver.
SFF-8665, Rev 1.9, June 29, 2015, Specification for QSFP+ 28 Gb/s 4X Pluggable Transceiver Solution (QSFP28).

SuggestedRemedy

Use these for now (most will be updated before this project is done):
OSFP Octal Small Form Factor Pluggable Module, Rev 5.0, October 2, 2022
QSFP-DD/QSFP-DD800/QSFP-DD1600 Hardware Specification for QSFP Double Density 8x Pluggable Transceivers, Rev 7.0, September 29, 2023
SFF-8665 Rev 1.9.4, 2022-04-01, QSFP+ 4X Pluggable Transceiver Solutions
SFF-TA-1011 Rev 1.1, 2024-04-19, Cross Reference to Select SFF Connectors and Modules
SFF-TA-1027, Rev 1.0, 2024-04-16, QSFP2 Connector, Cage, & Module Specification
SFF-TA-1031, Rev 1.0, 2023-06-11, SFP2 Cage, Connector, & Module Specification
https://osfpmsa.org/specification.html
http://www.qsfp-dd.com/specification/
Refer to these documents from 179C.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.

Cl **1** *SC* **1.4.184da** *P* **49** *L* **43** # 309

D'Ambrosia, John — Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *ER1 PHY (bucket)*

800GBASE-ER1 is defined as using 800GBASE-R encoding, but per 802.3df-2024, 1.4.184e - "The term 800GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) defined in Clause 172 for 800 Gb/s operation." This PHY as noted in Table 169-3a,uses PCS encoding as defined in Clause 186.

SuggestedRemedy

Define new name for family / encoding based on Clause 186 encoding.
Modify definition of entry for 800GBASE-ER1 to reflect new family name.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The comment correctly points out that the definition is not correct. However, it is not necessary to define a new family.
Change the definition of 800GBASE-ER1 and 800GBASE-ER1-20 to the following:
1.4.184da 800GBASE-ER1: IEEE 802.3 Physical Layer specification for 800 Gb/s PHY using 800GBASE-ER1 PCS and PMA encoding, dual polarization 16-state quadrature amplitude modulation (DP-16QAM) modulation, and coherent detection with reach up to at least 40 km. (See IEEE Std 802.3, Clause 186 and Clause 187).
1.4.184db 800GBASE-ER1-20: IEEE 802.3 Physical Layer specification for 800 Gb/s PHY using 800GBASE-ER1 PCS and PMA encoding, dual polarization 16-state quadrature amplitude modulation (DP-16QAM) modulation, and coherent detection with reach up to at least 20 km. (See IEEE Std 802.3, Clause 186 and Clause 187).
Implement with editorial license.

Cl **1** *SC* **1.4.184da** *P* **49** *L* **44** # 111

Huber, Thomas — Nokia

Comment Type **T** *Comment Status* **A** *ER1 PHY (bucket)*

Since 800GBASE-ER1 and -ER1-20 have a separate PCS, the definition for 800GBASE-ER1 and ER1-20 should refer to 800GBASE-ER1 encoding rather than 800GBASE-R encoding

SuggestedRemedy

Change 800GBASE-R to 800GBASE-ER1 for both the ER1 and ER1-20 definitions.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #309.

Cl **1** *SC* **1.4.184da** *P* **49** *L* **47** # 310

D'Ambrosia, John — Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *ER1 PHY (bucket)*

800GBASE-ER1-20 is defined as using 800GBASE-R encoding, but per 802.3df-2024, 1.4.184e - "The term 800GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) defined in Clause 172 for 800 Gb/s operation." This PHY as noted in Table 169-3a,uses PCS encoding as defined in Clause 186.

SuggestedRemedy

Define new name for family / encoding based on Clause 186 encoding.
Modify definition of entry for 800GBASE-ER1 to reflect new family name.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #309.

Cl **1** *SC* **1.5** *P* **51** *L* **11** # 74

Lusted, Kent — Intel Corporation

Comment Type **TR** *Comment Status* **A** *(bucket)*

The abbreviation "MLSD" is used numerous times in Annex 178A to reference Maximum Likelihood Sequence Detection and should be added to the abbreviations list.

SuggestedRemedy

Add MLSD | Maximum Likelihood Sequence Detection

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.

Cl **30** *SC* **30** *P* **56** *L* **33** # 369

He, Xiang Huawei

Comment Type **TR** *Comment Status* **R** *timesync (bucket)*

Add TimeSync entity managed object classes for Inner FEC sublayers defined in Clause 177 and 184.

SuggestedRemedy

Add register set for Inner FEC sublayers in subclauses of 30.13.1: (30.13.1.1 - 30.13.1.14)

(Presentation will be prepared for this comment.)

Response *Response Status* **C**

REJECT.
The following related presentation was reviewed by the 802.3dj task force during the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/he_3dj_01_2405.pdf
This presentation does not provide sufficient detail to describe the requested change in Clause 30.

Cl **30** *SC* **30.3.2.1.2** *P* **53** *L* **11** # 112

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *(bucket)*

There should also be an entry for 800GBASE-ER1 since it is a different PCS

SuggestedRemedy

Add a new editing instruction to insert 800GBASE-ER1 after 400GBASE-R.(or before the entry for 800GBASE-R).

Response *Response Status* **C**

ACCEPT.

Cl **30** *SC* **30.3.2.1.3** *P* **53** *L* **21** # 75

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *(bucket)*

There should also be an entry for 800GBASE-ER1 since it is a different PCS

SuggestedRemedy

Add a new editing instruction to insert 800GBASE-ER1 after 400GBASE-R (or before the entry for 800GBASE-R).

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45** *P* **57** *L* **1** # 603

de Koos, Andras Microchip Technology

Comment Type **T** *Comment Status* **A** *timesync (bucket)*

Inner FEC (Clause 177 or Clause 184) needs MDIO registers for TimeSync. They should look like the PMA/PMD clause registers.

SuggestedRemedy

Add the following MDIO registers for the Inner FEC, in the same style as the equivalent PMA/PMD MDIO registers
- TimeSync capability
- TimeSync transmit path data delay register
- TimeSync receive path data delay register

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The following related presentation was reviewed by the 802.3dj task force during the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/he_3dj_01_2405.pdf

The register bits and names described on page 8 of the presentation will be used with the exception that the ability bits will be added to example register "TimeSync PMA/PMD capability (Register 1.1800)" and the new delay registers will be added to MMD 1 from location 1.1820 onwards.

Implement the register bits and names described on page 8 of the presentation and with the exception that the ability bits will be added to example register "TimeSync PMA/PMD capability (Register 1.1800)" and the new delay registers will be added to MMD 1 from location 1.1820 onwards.

Implement with editorial licence.

Cl **45** *SC* **45** *P* **81** *L* **9** # 370

He, Xiang Huawei

Comment Type **TR** *Comment Status* **R** *timesync (bucket)*

Add MDIO interface reigsters for Inner FEC sublayers defined in Clause 177 and 184.

SuggestedRemedy

Add definitions for the new register set defined for the Inner FEC sublayers in 30.3.1.1 - 30.1.1.14.

(Presentation will be prepared for this comment.)

Response *Response Status* **C**

REJECT.
The following related presentation was reviewed by the 802.3dj task force at the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/he_3dj_01_2405.pdf
This presentation concerns TimeSync management and refers to the register set "30.13.1.1 - 30.13.1.14" rather than "30.3.1.1 - 30.1.1.14".
A different comment (#603) addresses adding registers for inner FEC TimeSync.
Another comment (#183) concerns adding additional status counters for the inner FEC which will require new registers.
There is insufficient detail given in this comment (#370) and comment #183 to make a change to Clause 45 for inner FEC register definitions at this time.

Cl **45** *SC* **45.2.1.60b** *P* **65** *L* **17** # 507

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **A** *(bucket)*

Shouldn't LR4 come before LR1 (same reach, narrower) and the order goes up the page, counting the bits forward

SuggestedRemedy

Swap 800GBASE-LR4 and 800GBASE-LR1

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.60b** *P* **65** *L* **24** # 508

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **A** *(bucket)*

800GBASE-DR4-2 has longer reach than 800GBASE-FR4-500

SuggestedRemedy

Swap them

Response *Response Status* **C**

ACCEPT.

Cl **45** *SC* **45.2.1.60c** *P* **67** *L* **21** # 509

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **A** *(bucket)*

It's unfortunate that 800GBASE-ER1 and 800GBASE-ER1-20 are in different registers, and 800GBASE-ER1-20, having less reach, should come first

SuggestedRemedy

Move 800GBASE-ER1 from 1.73.14 to 1.74.0. 1.73.14 goes back to reserved - maybe it can be used for 800GBASE-LR20-1 ;)

Response *Response Status* **C**

ACCEPT.

Cl **73** *SC* **73** *P* **83** *L* **1** # 460

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

We are now using a Next Page to advertise IEEE defined PHYs. However the order of when Next Pages are introduced, defined and then used is a bit out of order. So re-arranging the order in which AN is specified would help readers to better understand what how Next Pages are defined, how to use them and when to use them.

SuggestedRemedy

Presentation will be provided.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The following presentation was reviewed by the 802.3dj task force at the May Interim meeting.
https://www.ieee802.org/3/dj/public/24_05/slavick_3dj_01_2405.pdf
Implement the changes proposed in slavick_3dj_01_2405 with editorial licence and using appropriate editing instructions.

Cl **73** *SC* **73** *P* **85** *L* **9** # 149

Mi, Guangcan Huawei Technologies Co., Ltd

Comment Type **TR** *Comment Status* **A** *(bucket1p)*

Table 73-5 is missing the indication of higherst priority.

SuggestedRemedy

change 1.6Tb/s 8lane in the capability column to 1.6Tb/s 8 lane, highest priority.

Response *Response Status* **C**

ACCEPT.

Cl **73** *SC* **73.9.1.1** *P* **86** *L* **26** # 194

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **R** *ILT RTS SI (common)*

The existing semantics of the link_status parameter of AN_LINK.indication enables only two values, OK and FAIL. This imposes a need to bring up a link within a specified time (link_fail_inhibit_timer), otherwise AN will restart (per the Arbitration state diagram, Figure 73-11). This can cause numerous problems in a segmented link.

The AN should be tolerant to a link in which one or more of the devices is still in the process of training. This can be achieved by adding a third possible value to link_status, indicating that the negotiated PHY is still training.

SuggestedRemedy

A presentation with proposed content is planned.

Response *Response Status* **C**

REJECT.

The IEEE 802.3dj Task Force reviewed the following presentation during the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/ran_3dj_05_2405.pdf

The presentation does not provide sufficient detail to implement. A consensus presentation with a complete proposal is encouraged.

Cl **90A** *SC* **90A** *P* **519** *L* **43** # 456

Opsasnick, Eugene Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

In table 90A-1, the column titled "Alignment marker/ codeword marker insertion/removal" has a value of 2.56ns for 1.6T in the last row. This value should be the xMII time (at MAC data rate) of one Alignment marker block. The 1.6TE PCS lanes are now running at 100G vs 25G for slower speeds, so this number does not scale directly from the other entries. The value for the 1.6T row should be 1.28ns (a full AM group = 8 256b/257b blocks, so the MII time = 8 * 256 / 1600 = 1.28ns). Note that this column has correct values for 25G, 40G, 50G, and 100G. However, the value listed for 200G, 400G and 800G of 2.56ns should be 5.12ns and should also be fixed in maintenance.

SuggestedRemedy

Change the accuracy impairment value of 2.56 ns to 1.28 ns for the 1.6T Ethernet rate in Table 90A-1.

Response *Response Status* **C**

ACCEPT.

Cl **90A** *SC* **90A.3** *P* **519** *L* **43** # 330

de Koos, Andras Microchip Technology

Comment Type **T** *Comment Status* **A** *(bucket)*

For the added row in Table 90A-1, the potential timestamp accuracy impairment due to alignment marker insertion/removal for 1.6T is incorrect. It should be 1.28ns, not 2.56ns. The values for 200G, 400G, and 800G are also erroneous (should all be 5.12ns). I've filed a maintenance request to correct these, too.

SuggestedRemedy

Change 2.56 to 1.28ns in the added row for Table 90A-1

Response *Response Status* **C**

ACCEPT.

Cl **116** *SC* **116** *P* **92** *L* **40** # 445

Simms, William NVIDIA

Comment Type **E** *Comment Status* **A** *(editorial)*

spacing of text on line 40 is different than spacing of the same text in lin 38

SuggestedRemedy

make spacing the same

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **116** *SC* **116** *P* **94** *L* **6** # 150

Mi, Guangcan Huawei Technologies Co., Ltd

Comment Type **TR** *Comment Status* **A** *(bucket)*

In table 116-3, the last two column, missusage of PMD names.

SuggestedRemedy

change PHY type of CL 178 and 179 in the table to the correct nomenclature, i.e., 200GBASE-KR1 and 200GBASE-CR1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **116** *SC* **116** *P* **95** *L* **4** # 151

Mi, Guangcan — Huawei Technologies Co., Ltd

Comment Type **TR** *Comment Status* **A** *(bucket)*

In table 116-3a, the last two column, missusage of PMD names.

SuggestedRemedy

change PHY type of CL 178 and 179 in the table to the correct nomenclature, i.e., 400GBASE-KR2 and 400GBASE-CR2

Response *Response Status* **C**

ACCEPT.

Cl **116** *SC* **116** *P* **102** *L* **5** # 152

Mi, Guangcan — Huawei Technologies Co., Ltd

Comment Type **TR** *Comment Status* **A** *(bucket1p)*

200GBASE-R SM PMA delay constraint is missing

SuggestedRemedy

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
A suggested remedy is not provided.
200GBASE-R 8:1, 1:8, and 1:1 PMA types, all SM-PMA types are listed. Note that the term SM-PMA is used to reference any symbol multiplexing PMA, where it would otherwise be ambiguous. In the referenced text the multiplex ratio is unambiguous and the reference to Clause 176 in the notes column backs that up.
However, in this case using the SM-PMA term would be helpful.
With editorial license include the term SM-PMA and BM-PMA, instead of just PMA, where appropriate in this and similar tables.

Cl **116** *SC* **116** *P* **107** *L* **4** # 153

Mi, Guangcan — Huawei Technologies Co., Ltd

Comment Type **TR** *Comment Status* **A** *(bucket)*

In Table 116-9, there should be no applicable SP1 and SP6 for 113.4375GBd PMD lane

SuggestedRemedy

change the content of row SP1 and SP6 in the column of 113.4375GBd PMD lane to N/A

Response *Response Status* **C**

ACCEPT.

Cl **116** *SC* **116.1.3** *P* **92** *L* **30** # 311

D'Ambrosia, John — Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *FR1*

With the adoption of the objective to do 500m over 4 WDM lanes on a single mode fiber and its nomenclature 800GBASE-FR4-500, "FR" is no longer limited to just represent 2km (e.g. FR-500). This introduces an inconsistency for 200GBASE-FR1 and 200GBASE-DR1 (DR1 is not FR1-500). In addition, when looking at 2km for 1,2,4,8 fibers- a confusing "family" of PHYs emerges (200GBASE-FR1, 400GBASE-DR2-2, 800GBASE-DR4-2, and 1.6TBASE-DR8-2)

SuggestedRemedy

Rename 200GBASE-FR1 to 200GBASE-DR1-2

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The following presentation was reviewed by the 802.3dj task force at the May Interim meeting.

https://www.ieee802.org/3/dj/public/24_05/dambrosia_3dj_02a_2405.pdf
Implement the suggested remedy with editorial license.

Cl **116** *SC* **116.1.4** *P* **94** *L* **6** # 530

Rechtman, Zvi — Nvidia

Comment Type **T** *Comment Status* **A** *Conditional PMA (bucket)*

The comment refers to Table 116û3.
The SM_PMA and BM_PMA introduce a new case of optional PMA implementation. For instance 200GBASE-KR2 PHY cannot implement SM_PMA without implementing 200GAUI-1 C2C interface.
It will be beneficial to add a note about the conditions which allow/require implementation of BM_PMA and SM_PMA
Same apply to Table 116û3a, Table 116û4, Table 169û2

SuggestedRemedy

Add a footnote labeled æbÆ next to the æOÆ marking for 200GBASE-R SM-PMA in the entries for 200GBASE-KR2, 200GBASE-KR4, 200GBASE-CR2, and 200GBASE-CR4. The footnote æbÆ should state: æApplicable only when 200GAUI-1 C2C interface is used within the PHY

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #312.

Cl **116** *SC* **116.1.4** *P* **94** *L* **6** # 312

D'Ambrosia, John Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *Conditional PMA (bucket)*

200/400G BASE-R BM-PMA and 200/400G BASE-R-SM-PMA are noted as optional in Tables 116-3, 116-4,and 116-4a, but that is not quite correct. They are conditional dependent on the PHY type and on whether specific AUIs are implemented or not. .

SuggestedRemedy

For 100Gb/s based PHYs the 200GBASE-R BM-PMA is mandatory, all AUIs are optional, and 200GBASE R SM PMA is "C" / conditional if either 200GAUI-1 is implemented.
For 200Gb/s based PHYs the 200GBASE-R SM-PMA is mandatory, all AUIs are optional, and 200GBASE R BM PMA is "C" / conditional if either 200GAUI-2 is implemented.

For 100Gb/s based PHYs the 400GBASE-R BM-PMA is mandatory, all AUIs are optional, and 400GBASE R SM PMA is "C" / conditional if either 400GAUI-2 is implemented.
For 200Gb/s based PHYs the 400GBASE-R SM-PMA is mandatory, all AUIs are optional, and 400GBASE R BM PMA is "C" / conditional if either 400GAUI-4 is implemented.

Change entries as described above in Tables 116-3, 116-4 and116-4a for 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA to C / with notes as stated above
Modify entry in Table 178-1 to 200GBASE-R BM PMA to Conditional. Add note "c" A 200GBASE-R BM PMA must be implemented if a 200GAUI-2 C2C is implemented.
Modify entry in Table 178-2 to 400GBASE-R BM PMA to Conditional. Add note "c" A 400GBASE-R BM PMA must be implemented if a 400GAUI-4 C2C is implemented.
Modify entry in Table 179-1 to 200GBASE-R SM PMA to Conditional. Add note "c" A 200GBASE-R SM PMA must be implemented if a 200GAUI-1 C2C is implemented.
Modify entry in Table 179-2 to 400GBASE-R SM PMA to Conditional. Add note "c" A 400GBASE-R SM PMA must be implemented if a 400GAUI-2 C2C is implemented.
Modify entry in Table 181-1 to 200GBASE-R BM PMA to Conditional. Add note "c" A 200GBASE-R BM PMA must be implemented if a 200GAUI-2 C2C/C2M is implemented.
Modify entry in Table 180-2 to 400GBASE-R BM PMA to Conditional. Add note "c" A 400GBASE-R BM PMA must be implemented if a 400GAUI-4 C2C/C2M is implemented.
Modify entry in Table 182-1 to 200GBASE-R BM PMA to Conditional. Add note "c" A 200GBASE-R BM PMA must be implemented if a 200GAUI-2 C2C/C2M is implemented.
Modify entry in Table 182-2 to 400GBASE-R BM PMA to Conditional. Add note "c" A 400GBASE-R BM PMA must be implemented if a 400GAUI-4 C2C/C2M is implemented.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #317.

Cl **116** *SC* **116.1.4** *P* **98** *L* **18** # 313

D'Ambrosia, John Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *(bucket)*

there is no PMD called 400GBASE-LR4

SuggestedRemedy

Change 400GBASE-LR4 to 400GBASE-LR4-6

Response *Response Status* **C**

ACCEPT.

Cl **116** *SC* **116.2.4** *P* **99** *L* **1** # 314

D'Ambrosia, John Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *PMA introduction (bucket)*

In support of 200 Gb/s per lane signaling - 200GBASE-R BM-PMA and 400GBASE-R PMA, Clause 176 was developed. No addition was made to 116.2 Summary of 200GbE and 400 GbE sublayers was made.

SuggestedRemedy

Modify last sentence of 116.2.4 and add additional text
The 200GBASE-R and 400GBASE-R PMAs, which supports bit multiplexing, is specified in Clause 120.
The 200GBASE-R and 400GBASE-R PMAs, which supports symbol multiplexing, is specified in Clause 176.
Note that "PMA" is used as a general term to represent both types of PMAs for each speed.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The comment appropriately proposes to add the new PMA types defined in Clause 176 and to differentiate the two based on multiplexing type. It is not necessary to point out that they may both be referred to as PMA and in fact this could be considered incorrect, since any PMA in the 802.3 standard might be called a PMA.
Implement the following with editorial license:
Replace the second sentence in 116.2.4 with appropriate editorial instructions to the following:
200GBASE-R and 400GBASE-R PMAs that use bit multiplexing (BM-PMA) are specified in Clause 120.
200GBASE-R and 400GBASE-R PMAs that use symbol multiplexing (SM-PMA) are specified in Clause 176.
Implement with editorial license.

Cl **116** *SC* **116.3.2** *P* **99** *L* **52** # 195

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *ILT RTS SI (common)*

segment-by-segment training requires passing the RTS status of each device/sublayer in both directions.
When there is a physical interface with a training protocol, RTS is communicated using the protocol. But when two sublayers are attached, e.g. PMD and PMA, the status has to be communicated through the service interface.

This can be achieved if the inter-sublayer service interface includes both IS_SIGNAL.indication and IS_SIGNAL.request.

The values of the parameter SIGNAL_OK should be extended to allow communicating that a sublayer is in the process of training. A new value IN_PROGRESS would enable that.

Similar changes should be applied in clauses 169 and 174. The mapping of RTS to SIGNAL_OK should be defined in annex 176A.

SuggestedRemedy

A presentation with proposed content is planned.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The following presentation was reviewed by the 802.3dj task force at the IEEE 802.3 May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/ran_3dj_05_2405.pdf

Implement the proposal on slides 7 to 10 of ran_3dj_05_2405 with editorial license.

[Editor's note: CC]

Cl **116** *SC* **116.5** *P* **106** *L* **5** # 531

Rechtman, Zvi Nvidia

Comment Type **TR** *Comment Status* **A** *Skew (common)*

The comment refers to Table 116û8.
There is an additional logical skew present in the 200GBASE-R and 400GBASE-R2 BM_PMA of 2 RS-FEC CWs. These skew values should not be included in the skew budget calculations for this table. To prevent misinterpretations, an explicit note is required

SuggestedRemedy

Insert a note in Table 116û8 that states: æThe additional 2 RS-FEC CWs logical skew in clause 176 BM_PMA for 200GBASE-R and 400GBASE-R should not to be factored in the skew budget calculations for this table

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Motion #10 at the July 2023 plenary adopted the 4 CW interleaving for the 200GBASE-R 1:8/8:1 and 400GBASE-R 2:16/16:2 PMAs.
https://www.ieee802.org/3/dj/public/23_07/motions_3cwdfdj_2307.pdf#page=31

The motion explicitly calls out slide 10 of https://www.ieee802.org/3/dj/public/23_07/he_3dj_02a_2307.pdf, which lays out how skew be specified given the resulting systematic and reversible skew.

This consideration is applicable only to PHYs that include the following SM-PMA types:
400GBASE-R 16:2 and 2:16
200GBASE-R 8:1 and 1:8

Provide appropriate text in 116.5, explaining that for the PHYs summarized above, the skew specified in Table 116-8 excludes the intentional skew used to create the four codeword interleaving.

Implement with editorial license.

Cl **116** *SC* **116.5** *P* **107** *L* **46** # 510

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **A** *(bucket1p)*

A new footnote has appeared "At the PCS receive input, 1 UI is equivalent to 1 bit." attached to an unchanged number. There is no equivalent footnote for Table 116-8. In 802.3, "bit" means MAC bit. I don't know what point the footnote is making - that PCS lanes use binary signalling not PAM4? Nor why it is here. If it were kept, it should say "1 bit on a PCS lane" or similar.

SuggestedRemedy

Delete footnote f

Response *Response Status* **C**

ACCEPT.

Cl **119** *SC* **119.2.4.1** *P* **111** *L* **26** # 333

de Koos, Andras — Microchip Technology

Comment Type **T** *Comment Status* **R** *(bucket)*

I understand why the use of the stateless encoder decoder is restricted to 200GBASE-R, and 400GBASE-R over 200Gbps lanes. Allowing it on other PMDs/AUIs would be out-of-scope for the 802.3dj project.
HOWEVER, shouldn't common sense prevail, here?
The stateless encoder/decoder was designed such that it is all-but-identical to the stateful encoder, only differing in their treatment of /E/ blocks. Since the 200GBASE-R and 400GBASE-R links are always protected by FEC, it is not as if /E/ blocks can occur at random causing divergent behaviour of the two encoder/decoder types.
There is absolutely no danger of causing backward-compatibility issues, becasue the stateful encoder/decoder are still allowed for all PMDs
The stateless encoder/decoder was added to the standard to allow greater implementation flexibility (removing long timing paths). But any new PCS implementation that may attach to either 100Gbps/lane or 200Gbps/lane PMDs would have to implement the stateful encoder/decoder! With the stateless encoder, the standard is offering more implementation flexibility that implemetors cannot actually use.

SuggestedRemedy

Consider removing the restriction on PMD type when using the stateless encoder and decoder in subclauses 119.2.4.1 and 119.2.5.8, respectively.

Response *Response Status* **C**

REJECT.
As stated in the comment itself, adding an option to support stateless encoding/decoding for PHYs that are not part of the 802.3dj project is out-of-scope .

Cl **119** *SC* **119.2.5.8** *P* **112** *L* **27** # 470

Slavick, Jeff — Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

Extranious "either"

SuggestedRemedy

remove the word "either"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion

Cl **120** *SC* **120.1.1a** *P* **114** *L* **30** # 66

Dudek, Mike — Marvell

Comment Type **T** *Comment Status* **A** *PMA introduction (bucket)*

Table 116-1 and Table 116-2 include the 200Gb/s per lane PMDs which require the symbol muxing PMA. This bit muxing PMA would only be used for lower speed AUIs. Saying it supports any of the PMDs in the tables is confusing.

SuggestedRemedy

Change to "The 200GBASE-R PMA(s) can support any of the two, or four lane 200Gb/s PMDs in Table116û1 and the 400GBASE-R PMA(s) can support
any of the four, or 8 lane 400Gb/s PMDs in Table 116û2". As a less preferred apporach PMD's could be changed to PHYs in the original sentence and an additional sentence could be added saying "The single lane 200Gb/s PMDs in Table 116-1 and the two lane 400Gb/s in table 115-2 require the symbol-muxing PMAs described in clause 176."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Indeed, the PMA defined in Clause 120 can support only PMDs with per-lane signaling rates of 100 Gb/s or less.
The referenced paragraph should therefore be corrected.
In Clause 116...
Remove 200GBASE-KR1/CR1 from Table 116-3 and change table title to:
"PHY type and clause correlation (200GBASE copper with 2 or 4 lanes)"
Remove 400GBASE-KR2/CR2 from Table 116-3a and change table title to:
"PHY type and clause correlation (200GBASE copper with 4 lanes)
Create new Table 116-3c with title "PHY type and clause correlation (200GBASE copper with 1 lanes)"
Include 200GBASE-KR1/CR1 in this table.
Create new Table 116-3d with title "PHY type and clause correlation (400GBASE copper with 2 lanes)"
Include 400GBASE-KR2/CR2 in this table.
In Clause 120...
Change the referenced sentence to:
"The 200GBASE-R PMA(s) can support any of the 200Gb/s PMDs in Table 116-3 and Table 116-4, and the 400GBASE-R PMA(s) can support any of the 400Gb/s PMDs in Table 116-3a and Table 116-5."
Implement with editorial license.
[Editor's note: CC 116, 120]

Cl **120F** *SC* **120F.1** *P* **522** *L* **7** # 67

Dudek, Mike — Marvell

Comment Type **T** *Comment Status* **R** *Precoding (bucket)*

Clause 176 is for the symbol mux PMA it should not be used for Annex 120F

SuggestedRemedy

Remove the reference to 176.9.1.2

Response *Response Status* **C**

REJECT.
Annex 120F is amended to include 1.6TAUI-16.
176.8.4 defines the 1.6TBASE-R 16:16 PMA, which has a 16-lane interface that can use 1.6TAUI-16 as a physical interface.
176.9.1.2 describes the precoding function for all symbol-muxing PMAs, which can also be used in the aforementioned PMA.

Cl **169** *SC* **169** *P* **116** *L* **15** # 155

Mi, Guangcan — Huawei Technologies Co., Ltd

Comment Type **TR** *Comment Status* **R** *PHY descriptions (bucket)*

same as the previous comment on 800GBASE-CR4

SuggestedRemedy

make the description consistent

Response *Response Status* **C**

REJECT.
It is assumed that the referenced "previous comment" is Comment #154.
The language used here is consistent with other similar PHY types in this table. There is similar differences between the PHYs described in this table and the definitions in 1.4.

Cl **169** *SC* **169** *P* **116** *L* **17** # 154

Mi, Guangcan — Huawei Technologies Co., Ltd

Comment Type **TR** *Comment Status* **R** *PHY descriptions (bucket)*

In Table 169-1, Row of 800GBASE-CR4 was described as 800Gb/s PHY using 800GBASE-R encoding over four lanes of twinaxial copper cable, which is inconsistent with the description in page 49, 1.4.184aa

SuggestedRemedy

make the language consistent.

Response *Response Status* **C**

REJECT.
The language used here is consistent with other similar PHY types in this table. There are similar differences between the PHYs described in this table and the definitions in 1.4.

Cl **169** *SC* **169** *P* **118** *L* **4** # 156

Mi, Guangcan — Huawei Technologies Co., Ltd

Comment Type **TR** *Comment Status* **A** *(bucket)*

In table 169-3, Phy type and clause correlation was marked incorrectly for the columns of 8000GBASE-DR8 PMD and 800GBASE-DR8-2 PMD

SuggestedRemedy

remove the unnecessary M in the following rows for 800GBASE-DR8 PMD: 800GBASe-DR4, 800GBASE-FR4-500. remove the unnecessary M in the following rows for 800GBASE-DR8-2 PMD: 800GBASe-DR4-2, 800GBASE-FR4, and 800GBASE-LR4.

Response *Response Status* **C**

ACCEPT.

Cl **169** *SC* **169** *P* **123** *L* **5** # 158

Mi, Guangcan — Huawei Technologies Co., Ltd

Comment Type **TR** *Comment Status* **R** *(bucket)*

In Table 169-4, the delay constraints on 800GBASE-R BM-PMA and 800GBASE-R SM-PMA are missing

SuggestedRemedy

add appropriate rows with TBD if no consensus has been built.

Response *Response Status* **C**

REJECT.
800GBASE-R 32:4, 4:32, and 4;4, all SM-PMA types are listed in Table 169-4. Note that the term SM-PMA is used to reference any symbol multiplexing PMA, where it would otherwise be ambiguous. In the referenced text the multiplex ratio is unambiguous and the reference to Clause 176 in the notes column backs that up.

Cl **169** *SC* **169** *P* **127** *L* **4** # 157

Mi, Guangcan — Huawei Technologies Co., Ltd

Comment Type **TR** *Comment Status* **A** *(bucket)*

In Table 116-6, there should be no applicable SP1 and SP6 for 113.4375GBd PMD lane

SuggestedRemedy

change the content of row SP1 and SP6 in the column of 113.4375GBd PMD lane to N/A

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
It is assumed that the comment is referring to Table 169-6 rather than the referenced Table 116-6.
Implement the suggested remedy with editorial license.

Cl **169** *SC* **169.1.3** *P* **116** *L* **42** # 315

D'Ambrosia, John
Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *ER1 PHY (bucket)*

800GBASE-ER1-20 and 800GBASE-ER1 are both defined as using 800GBASE-R encoding, but per 802.3df-2024, 1.4.184e - "The term 800GBASE-R represents a family of Physical Layer devices using the Physical Coding Sublayer (PCS) defined in Clause 172 for 800 Gb/s operation." These two PHYs as noted in Table 169-3a, they use PCS encoding as defined in Clause 186.

SuggestedRemedy

Define new name for family / encoding based on Clause 186 encoding.
Eliminate table entries for ER1-20 and ER1 from Table 169-3a.
Create new table for PHY type and clause correlation for new family based on Clause 186 encoding.
Modify description of entry for 800GBASE-ER1-20 in Table 169-1 to reflect new family name.
Modify description of entry for 800GBASE-ER1 in Table 169-1 to reflect new family name.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
This table lists ALL 800 Gb/s Ethernet PHY types (i.e., 800GBASE), not specifically 800GBASE-R PHY types. The description for 800GBASE-ER1 and 800GBASE-ER1-20 is deceiving and should be updated in line with the definitions in Clause 1. Table 169-3a, lists 800GBASE optical coherent PHY types (not specifically 800GBASE-R), so a separate nomenclature table is not required for 800GBASE-ER1/ER1-20.
Note that comments 111, 310, and 311 propose changes to the definitions in Clause 1.
In Table 169-1, change the definitions as follows:
800GBASE-ER1-20 | 800 Gb/s PHY using 800GBASE-ER1 PCS and PMA encoding, dual polarization 16-state quadrature amplitude modulation (DP-16QAM) modulation, and coherent detection with reach up to at least 20 km (see Clause 187)
800GBASE-ER1 | 800 Gb/s PHY using 800GBASE-ER1 PCS and PMA encoding, dual polarization 16-state quadrature amplitude modulation (DP-16QAM) modulation, and coherent detection with reach up to at least 40 km (see Clause 187)
Implement with editorial license.

Cl **169** *SC* **169.1.3** *P* **116** *L* **43** # 76

Huber, Thomas
Nokia

Comment Type **T** *Comment Status* **A** *ER1 PHY (bucket)*

The descriptions of 800GBASE-ER1-20 and 800GBASE-ER1 should refer to 800GBASE-ER1 encoding rather than 800GBASE-R encoding since the ER1[-20] PCS is distinct from the 800GBASE-R PCS

SuggestedRemedy

Change 800GBASE-R to 800GBASE-ER1 in the last two rows of the table.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #315.

Cl **169** *SC* **169.1.4** *P* **117** *L* **12** # 317

D'Ambrosia, John — Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *Conditional PMA (bucket)*

800GBASE-R BM-PMA and 800GBASE-R-SM-PMA are noted as optional in Tables 169-2, 169-3, and Table 169-3a, but that is not quite correct. They are conditional dependent on the PHY type and on whether specific AUIs are implemented or not. .

SuggestedRemedy

For 100Gb/s based PHYs the 800GBASE-R BM-PMA is mandatory, all AUIs are optional, and 800GBASE R SM PMA is "C" / conditional if either 800GAUI-4 is implemented.
For 200Gb/s based PHYs the 800GBASE-R SM-PMA is mandatory, all AUIs are optional, and 800GBASE R BM PMA is "C" / conditional if either 800GAUI-8 is implemented.

Change entries as described above in Tables 169-2, 169-3 and 169-3a for 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA to C / with notes as stated above.

Modify entry in Table 178-3 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C is implemented.
Modify entry in Table 179-3 to 800GBASE-R SM PMA to Conditional. Add note "c" A 800GBASE-R SM PMA must be implemented if a 800GAUI-4 C2C is implemented.
Modify entry in Table 180-3 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C/C2M is implemented.
Modify entry in Table 181-1 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C/C2M is implemented.
Modify entry in Table 182-3 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C/C2M is implemented.
Modify entry in Table 183-1 to 800GBASE-R BM PMA to Conditional. Add note "c" A 800GBASE-R BM PMA must be implemented if a 800GAUI-8 C2C/C2M is implemented.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Some guidance as to when the two PMA types are used would be helpful. However, it is not as simple as proposed in the suggested remedy. Guidance is required for all PMAs used within the various xAUIs. Annex 176B provides all of the necessary guidance.
Each of the tables listing physical layer clauses associated with PMD types (e.g., Table 180-3 for 800GBASE-DR4) already include a reference to Annex 176B for the AUIs, but not for the two PMA types. Additional guidance in these tables would be helpful.
In the nomenclature tables in Clause 169 it is not necessary to repeat all of these details nor is there any space in these already crowded tables; instead it would be sufficient, efficient, and future-proof to point back to the PMD clauses for guidance.
For each new PMD (Clauses 178, 179, 180 to 183, 185, 186), update the PMD tables in the PMD clause and the associated nomenclature table in Clause 116, 169, and 174, similar to the following for the 800GBASE-DR4 defined in Clause 180.
In Table 180-1, for the 800BASE-R BM-PMA row, change "Optional" to "Conditional" with the following footnote:
"If one or two 800GAUI-n is implemented in a PHY, additional 800GBASE-R BM-PMA or SM-PMA sublayers are required according to the guidelines in Annex 176B.6.1."
Attach the same footnote to "Required" in the row for 800GBASE-R SM-PMA.
In Table 169-3...
In the cell (800GBASE-DR4 row, 800GBASE-R BM-PMA column), change "O" to "C".
In footnote "a" add ", C = Conditional (refer to PMD clause for details)."
Implement with editorial license.

Cl **169** *SC* **169.1.4** *P* **117** *L* **12** # 316

D'Ambrosia, John — Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *PMA introduction (bucket)*

Table 169-2 introduces the 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA in Table 169-2, but there is no real explanation to the use of the sub-layers - just the required PMA service interfaces, as noted in Items C&E. The clarification of these two sublayers is actually defined in 176.2 Conventions, which doesnt make sense.

SuggestedRemedy

Move definitions of 800GBASE-R BM-PMA and 800GBASE-R-SM-PMA from 176.2 to 169.1.3 Nomenclature

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The terms BM-PMA and SM-PMA are defined in 120.1.1 and 176.1.1. The same terms are listed in 176.2, but the items in this larger list are terms for use only within Clause 176.
The definition of BM-PMA and SM-PMA should remain in the subclauses listed above. But they should also be introduced Clause 169.
Resolve using the response to comment #318.

Cl **169** *SC* **169.1.4** *P* **118** *L* **22** # 69

Dudek, Mike — Marvell

Comment Type **T** *Comment Status* **A** *(bucket)*

There are errors in Table 169-3. 800GBASE-DR8-PMD is not needed for 800GBASE-DR4 or 800GBASE-FR4-500, 800GBASE-DR8-2 PMD is not needed for 800GBASE-DR4-2, 800GBASE-FR4, or 800GBASE-LR4,

SuggestedRemedy

Delete the offending "M"s

Response *Response Status* **C**

ACCEPT.

Cl **169** *SC* **169.1.4** *P* **118** *L* **22** # 68

Dudek, Mike — Marvell

Comment Type **T** *Comment Status* **A** *(bucket)*

There are errors in Table 169-3. 800GBASE-DR8-PMD is not needed for 800GBASE-DR4 or 800GBASE-FR4-500, 800GBASE-DR8-2 PMD is not needed for 800GBASE-DR4-2, 800GBASE-FR4, or 800GBASE-LR4,

SuggestedRemedy

Delete the offending "M"s

Response *Response Status* **C**

ACCEPT.

Cl **169** *SC* **169.1.4** *P* **119** *L* **19** # 320

D'Ambrosia, John — Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *Conditional PMA (bucket)*

For 800GBASE-LR1 in Table 169-3a
800GBASE-R BM-PMA is conditional, pending implementation of 800GAUI-8 C2C/C2M
800GBASE-R SM PMA is conditional, pending implementation of 800GAUI-4 C2C/C2M

SuggestedRemedy

Change entries for 800GBASE-LR1 to C for 800GBASE-R BM-PMA and 800GBASE-R SM-PMA
Add note "C= Conditional, 800GBASE-R BM-PMA is conditional, pending implementation of 800GAUI-8 C2C/C2M
800GBASE-R SM PMA is conditional, pending implementation of 800GAUI-4 C2C/C2M"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #317.
[Editor's note: Changed subclause from 169.1.3 to 169.1.4]

Cl **169** *SC* **169.1.4** *P* **119** *L* **20** # 77

Huber, Thomas — Nokia

Comment Type **T** *Comment Status* **R** *(bucket)*

The 800GXS can contain AUIs - so the C2C and C2M clauses should be marked as optional for the ER1 and ER1-20 PHYs, as should the associated PMAs.

SuggestedRemedy

Indicatge that 800GBASE-R BM-PMA, 800GAUI-8 C2C, 800GAUI-8 C2M, 800GBASE-R SM-PMA, 800GAUI-4 C2C, and 800GAUI-4 C2M are optional for both ER1 and ER1-20 PHYs.

Response *Response Status* **C**

REJECT.
The table references the optional 800GMII Extender which specifies the optional/condition AUIs and PMAs.

Cl **169** *SC* **169.2** *P* **119** *L* **28** # 319

D'Ambrosia, John — Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *ER1 PHY (bucket)*

800GBASE-ER1 and 800GBASE-ER1-20 use the Clause 186 800GBASE-ER1 PCS/PMA. This layer is not described as part of 169.2.

SuggestedRemedy

Create 169.2.4c 800GBASE-ER1 PCS/PMA
The 800GBASE-ER1 PCS performs encoding of data from the 800GMII, performs GMP mapping, applies FEC, and transfers the encoded data to the PMA. The 800GBASE-ER1 PMA sublayer perform the mapping of transmit and receive data streams between the PCS and PMA via the PMA service interface, and the mapping and multiplexing of transmit and receive data streams between the PMA and PMD via the PMD service interface.
The 800GBASE-ER1 PCS is specified in Clause xxx.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Amend subclause 169.2.3 (from 802.3df) to the following with appropriate editorial instructions and mark-ups.
The PCS performs encoding of data from the 800GMII data into a form compatible with the PMA and PMD.
The 800GBASE-R PCS is specified in Clause 172.
The 800GBASE-ER1 PCS is specified in Clause 186.
Implement with editorial license.

Cl **169** *SC* **169.2** *P* **119** *L* **28** # 318

D'Ambrosia, John — Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *PMA introduction (bucket)*

In support of 200 Gb/s per lane signaling - 800GBASE-R BM-PMA, Clause 176 was developed. No addition was made to 169.2 Summary of 800 GbE archicture

SuggestedRemedy

Modify 169.2.4 to read -
The PMA sublayer provides a medium-independent means to support the use of a range of physical media.
The 800GBASE-R PMA, which supports bit multiplexing, is specified in Clause 173.
The 800GBASE-R PMA, which supports symbol multiplexing , is specified in Clause 176.
Note that "PMA" is used as a general term to represent both types of PMAs.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The comment appropriately proposes to add the new PMA types defined in Clause 176 and to differentiate the two based on multiplexing type. It is not necessary to point out that they may both be referred to as PMA and in fact this could be considered incorrect, since any PMA in the 802.3 standard might be called a PMA.
Implement the following with editorial license:
Replace the second sentence in 169.2.4 with appropriate editorial instructions to the following:
The 800GBASE-R PMA that uses bit multiplexing (BM-PMA) is specified in Clause 173.
The 800GBASE-R PMA that uses symbol multiplexing (SM-PMA) is specified in Clause 176.
Implement with editorial license.

Cl **169** *SC* **169.2** *P* **119** *L* **31** # 193

Ran, Adee — Cisco

Comment Type **TR** *Comment Status* **A** *ER1 PHY (bucket)*

A new 800GBASE-ER1 PCS is defined in clause 186. It should be mentioned in the introduction clause, 169.2.3 ("Physical Coding Sublayer (PCS)" in 802.3df) which currently only refers to the 800GBASE-R PCS.

SuggestedRemedy

Bring 169.2.3 into the draft and amend it to include the clause 186 PCS.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #319.

Cl **169** *SC* **169.3.2** *P* **122** *L* **14** # 322

D'Ambrosia, John — Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *(bucket)*

There is no inter-sublayer interface for the PMA sublayer shown in the figure

SuggestedRemedy

Add placeholder text for future text.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Figure 169-2b is correct as drawn, except that the PMA definition in the legend should be deleted.
However, this same figure is repeated in the 800GBASE-LR1 PMD clause. We should not be repeating figures. Since this form is unique to a single PHY type, not a family, it makes more sense to include the figure in the PMD clause.
Delete Figure 169-2b and instead include a reference to Figure 185-2 and Figure 185-3 in 169.3.2.
Also, in Figure 184-1 delete the PMA definition from the legend.
Implement with editorial license.

Cl **169** *SC* **169.3.2** *P* **122** *L* **35** # 78

Huber, Thomas — Nokia

Comment Type **T** *Comment Status* **A** *ER1 PHY (bucket1p)*

A similar diagram is needed for 800GBASE-ER1 and 800GBASE-ER1-20 PHYs.

SuggestedRemedy

Use figure 169-2b as a basis. Replace 800GBASE-R PCS with 800GBASE-ER1 PCS, 800GBASE-LR1 Inner FEC with 800GBASE-ER1 PMA, and 800GBASE-R PMD with 800GBASE-ER1 PMD (and of course renams all the service interfaces to align with that).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

A similar diagram for 800GBASE-ER1 and 800GBASE-ER1-20 is provided in Clause 187 which specifies both of these PMD types. No other 800GBASE PMD is of this form so it is not necessary to show a common diagram in Clause 169.

However, some clarification for non-800GBASE-R PHY types would be helpful.

In 169.3 add text pointing out that service interfaces used by PMDs not part of 800GBASE-R family are defined and illustrated in the PMD clauses.

Implement with editorial license.

Cl **169** *SC* **169.3.2** *P* **122** *L* **54** # 321

D'Ambrosia, John — Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *ER1 PHY (bucket1p)*

There is no figure describing 800GBASE-ER1/-20 describing inter-sublayer service interaces including 800GBASE-ER1 PCS/PMA

SuggestedRemedy

Add placeholder text for future text.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #78.

Cl **169** *SC* **169.4** *P* **123** *L* **5** # 532

Rechtman, Zvi — Nvidia

Comment Type **TR** *Comment Status* **A** *(bucket)*

The comment refers to Table 169û4.
The Inner-FEC delay appears to be missing from the table

SuggestedRemedy

add 800GBASE-R inner FEC (values are TBDs)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **170** *SC* **170.1** *P* **135** *L* **12** # 461

Slavick, Jeff — Broadcom

Comment Type **T** *Comment Status* **R** *(bucket)*

The title of Clause 173 does include BM.

SuggestedRemedy

Remove the BM- from Table 171-1 for the Clause 173 entry and footnote A

Response *Response Status* **C**

REJECT.
The term BM-PMA is used in Table 171-1, because this table includes reference to both BM and SM PMAs, and the convention we agreed on was in such cases to call out both PMAs explicitly. The same convention is used in tables 178-1, 179-1, 180-1, 181-1, 182-1 and 183-1.
This is explained in 173.1.1 as follows:
"When necessary for disambiguation, to differentiate the bit-multiplexing PMA (BM-PMA) types defined in this clause from the symbol-multiplexing PMA (SM-PMA) types defined in Clause 176, the term BM-PMA is used. Within this clause the term PMA refers specifically to the BM-PMA."

Cl **171** *SC* **171.3** *P* **137** *L* **41** # 386

Nicholl, Gary — Cisco

Comment Type **T** *Comment Status* **A** *(bucket)*

There is an issue with subclause 171.3.3 generated by 802.3df. There is an incorrect reference of "171.6.2" in the following bullets:

ù An additional signal TXRD indicates the state of the rx_rm_degraded variable (see 171.6.2) as
detected by the PHY 800GXS in the transmit direction
ù An additional signal TXLD indicates the state of the FEC_degraded_SER variable (see 171.6.2) as
detected by the PHY 800GXS in the transmit direction

SuggestedRemedy

Import subclause 171.3.3 and correct the two bullets as follows:

ù An additional signal TXRD indicates the state of the rx_rm_degraded variable (see 172.2.6.2.2) as detected by the PHY 800GXS in the transmit direction
ù An additional signal TXLD is the logical OR of the FEC_degraded_SER and rx_local_degraded variables (see 172.2.6.2.2) as
detected by the PHY 800GXS in the transmit direction.

Response *Response Status* **C**

ACCEPT.

Cl **171** *SC* **171.5** *P* **141** *L* **47** # 385

Nicholl, Gary — Cisco

Comment Type **T** *Comment Status* **A** *Link fault signaling*

There sentence below the editor's not is a repeat of what is captured in 171.3.2. It is also not releated to ôlink fault signalingö as defined in 81.3.4, which is the topic of this subclause.

SuggestedRemedy

Delete the sentence below the editor's note.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Delete the sentence below the editor's note, and remove the Editor's note.

Cl **171** *SC* **171.8** *P* **144** *L* **23** # 79

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **R** *(bucket)*

In tables 171-3 and 171-5, it is not clear what has changed in the rows that are shown.

SuggestedRemedy

Indicate the changes with revision marks

Response *Response Status* **C**

REJECT.

Although it may be hard to see, the draft is following 802.3 editing guidelines. The thing that changed in tables 171-3 and 171-5 is that an "_" was added between "FEC_symbol_error_counter" and "<0:31>" in the status variable column. Being added text, the "_" is underlined in keeping with 802.3 editing convention. The missing underscore was missed in the 802.3df draft, including during the final publication review.

Cl **171** *SC* **171.8** *P* **145** *L* **6** # 462

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **R** *(withdrawn)*

The MDIO mapping table is different from Clause 175, it should use the new form that Clause 175 is using.

SuggestedRemedy

Have Tables 171-5a through 171-5d use the same format as Clause 175

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **174** *SC* **174** *P* **164** *L* **20** # 159

Mi, Guangcan Huawei Technologies Co., Ltd

Comment Type **TR** *Comment Status* **A** *(bucket)*

In Table 174-4, the notes for 1.6TBASE-KR8 and 1.6TBASE-CR8 says includes the medium in one direction. No length of the medium was provided, nor any explicit delay due to the medium was provided. While In Table 169-4, a definitive of 14ns allocated for one direction through cable medium was provided for 800GBASE-CR4. One would assume 1.6TBASE-CR8 would be consistent with 800GBASE-CR4. The same problem applies to 1.6TBASE-KR8.

SuggestedRemedy

Put in explicit allocation of delay constraints for the medium used in 1.6T BASE-CR8 and 1.6TBASE-KR8. Align with that of 800GBASE-CR4 and 800GBASE-KR4, if technically feasibly.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Use the same text used for 800GBASE-KR8/CR8 in IEEE Std 802.3df-2024.
For the 800GBASE-KR4 row change the text in the note column to:
"Includes allocation of 14 ns for one direction through backplane medium. See 178.6."
For 800GBASE-CR4 row change the text in the note column to:
"Includes allocation of 14 ns for one direction through backplane medium. See 179.6."

Cl **174** *SC* **174.1.2** *P* **155** *L* **47** # 180

Brown, Matt Alphawave Semi

Comment Type **T** *Comment Status* **A** *List of interfaces*

This list of interface widths has been traditionally included in "new ethernet rate introduction" clauses since 10 Gb/s Ethernet. It seems unecessary and present and extra burden to amend with each new interface added. The number of lanes is abundantly clear in each clause that defines and interface. The original intent was to point out that the structural detail of the specified interfaces are to be as specified while others that are not are not specified.

SuggestedRemedy

Delete the paragraph and lists from page 155 line 47 to page 156 line 12.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Retain the first sentence:
"While this specification defines interfaces in terms of bits, octets, and frames, implementations may choose
other data-path widths for implementation convenience."
Add a future-proof exception and delete the lettered-list of interfaces.
Implement with editorial license.

Cl **174A** SC **174A.1** P **539** L **10** # 205

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *BER/FLR*

The first subclause of Annex 174 is currently a mini "table of contents" of the clause. This isn't required.

Instead, an introduction to the annex would be helpful for readers. It should provide the relationship between bit error ratio as defined in the project's objective and the frame loss ratio, as well as the purpose of defining error requirements for internal interfaces within the physical layer.

SuggestedRemedy

A presentation with proposed content is planned.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The following presentation was reviewed by the IEEE 802.3dj task force as the May Interim meeting.
https://www.ieee802.org/3/dj/public/24_05/ran_3dj_04a_2405.pdf

Implement the following with editorial license.

Update Annex 174A as proposed on slides 7 to 13 of ran_3dj_04a_2405 excluding option A in slides 11, 12, and 13.

Update clauses/annexes 171, 178, 179, 179D, 179E, 180 to 183, 185, 187 appropriately.

[Editor's note: CC many]

Cl **174A** SC **174A.2** P **539** L **19** # 206

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *BER/FLR*

174A.2 "Frame loss ratio for RS to RS link" is empty.

Since this annex defines several performance metrics, the titles of specific subclauses should be based on the sub-link in question, while the specific requirement (FLR, BER, etc.) should preferably be in the subclause text.

SuggestedRemedy

A presentation with proposed content is planned.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #205.

Cl **174A** SC **174A.3** P **539** L **25** # 190

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *BER/FLR*

174A.3 "Frame loss ratio for a Physical Layer implementation" is empty.

I assume a "Physical Layer implementation" means the path between the RS and the MDI. It is unclear how frame loss ratio can be defined for this path, because the two interfaces are not equivalent; frames are defined only at the RS, and cannot be identified, checked for errors, or counted on the MDI. Similarly, the signals on the MDI cannot be compared to the data stream on the RS, so no other "error metric" can be defined.

This is in contrast to "RS to RS link" and other subclauses, in which such checking and counting is possible.

This subclause should be deleted.

SuggestedRemedy

Delete 174A.3.

Response *Response Status* **C**

ACCEPT.

Cl **174A** SC **174A.4** P **539** L **30** # 191

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *BER/FLR*

174A.4 "Frame loss ratio for an xMII Extender" is empty.

Since this annex defines several performance metrics, the titles of specific subclauses should be based on the sub-link in question, while the specific requirement (FLR, BER, etc.) should preferably be in the subclause text.

SuggestedRemedy

A presentation with proposed content is planned.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #205.

Cl **174A** *SC* **174A.5** *P* **539** *L* **36** # 192

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *BER/FLR*

174A.5 "Frame loss ratio for PHY" is empty.

Since this annex defines several performance metrics, the titles of specific subclauses should be based on the sub-link in question, while the specific requirement (FLR, BER, etc.) should preferably be in the subclause text.

SuggestedRemedy

A presentation with proposed content is planned.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #205.

Cl **175** *SC* **175** *P* **169** *L* **1** # 332

de Koos, Andras Microchip Technology

Comment Type **T** *Comment Status* **R** *timesync (bucket1p)*

Has any thought been given to how to calculate the latency through the 1.6TBASE-R PCS, i.e. the path data delay values for the purposes of TimeSync?
I do not see anything within the 1.6TBASE-R PCS that would prevent proper calculation of the path data delay values.
Clause 90.7.1 is instructive here, explaining that the path data delays should be "reported as if the DDMP is at the start of the FEC codeword". However, the existing language in 90.7.1 is awkward for PCSs with more than one FEC engine like the 1.6TBASE-R PCS, which has four FEC codewords in parallel.

SuggestedRemedy

No proposed change to Clause 175.
Clause 90.7.1 could be cleaned up to account for when there are multiple FEC codewords in parallel, but I assume that is out-of-scope for the 802.3dj project? I'll submit a maintenance request.

Response *Response Status* **C**

REJECT.
The suggested remedy does not propose an actionable (within the draft) remedy.

This comment is related to the calculation of the path data delay values in Clause 90, and points out that Subclause 90.7.1 is not clear on how the path data delays values are calculated for PCSs with more than one FEC engine and interleaved FEC codewords. This applies to the 200GbE/400GbE PCS (Clause 119), the 800GbE PCS (Clause 172) as well as the new 1.6TbE PCS being added by this project (Clause 175). As pointed out in the suggested remedy it would be better to address this with a maintenance request that equally applies to all PCS clauses with multiple interleaved FEC codewords and all of their related PHYs (many of which are out of scope for 802.3dj).

Cl **175** *SC* **175.2.1** *P* **172** *L* **26** # 376

Ofelt, David Juniper Networks

Comment Type **T** *Comment Status* **A** *(bucket)*

Text says to interleave two codewords from flow 0 and two from flow 1, but it isn't clear that those two should be from different FEC encoders.

SuggestedRemedy

After FEC encoding, a FEC codeword from each of the two encoders in flow 0 and a FEC codeword from each of the two encoders in flow 1 are then interleaved and distrubted to individual PCS lanes.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement the suggested remedy with editorial license.

Cl **175** *SC* **175.2.4.2** *P* **173** *L* **26** # 481

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **R** *timesync (bucket)*

A note that modifying the data stream could affect TimeSync would be useful.

SuggestedRemedy

Add the following note:
"NOTE -- Insertion or removal of characters may affect protocols like times synchronization (see 90.4.1.2)"

Response *Response Status* **C**

REJECT.
It is not helpful to sprinkle notes related to time synchronization throughout the various sublayer clauses; this was not done in previous clauses/projects. Rather it would be preferable to add the necessary text into Clause 90/Annex 90A. A consensus presentation with a complete proposal is encouraged.

Cl **175** *SC* **175.2.4.4** *P* **173** *L* **41** # 463

Slavick, Jeff — Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

The last sentence is giving the tranccoded blocks sent to each flow a name. So it's not really make a flow of blocks. If anything it's making a series or stream of blocks.

SuggestedRemedy

Change the last sentence to read: "The transcoded blocks sent to flow 0 are referred to as tx_xcoded_f0<256:0> and the ones sent to flow 1 as tx_xcoded_f1<256:0>."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement the following with editorial license.

Change:
"This creates two flows of transcoded blocks, tx_xcoded_f0<256:0> to flow 0, and tx_xcoded_f1<256:0> to flow 1."
to:
"This creates two streams of transcoded blocks, tx_xcoded_f0<256:0> to flow 0, and tx_xcoded_f1<256:0> to flow 1."

Cl **175** *SC* **175.2.4.5** *P* **173** *L* **50** # 331

de Koos, Andras — Microchip Technology

Comment Type **T** *Comment Status* **A** *Scrambler seeds (bucket)*

Different scrambler seeds for the two flows are NOT strictly necessary for the 1.6TBASE-R PCS. The output PCSLs are never bit muxed, so having identical outputs from FEC A and FEC C, for example, should never have any adverse effect on "clock content" of the SerDes output.
It doesn't hurt to have the scramblers be seeded differently, however.

SuggestedRemedy

Consider changing the last sentence on page 173 from:
When reset is asserted, the two scramblers shall be initialized to a value other than zero and different from each other.
To:
When reset is asserted, the two scramblers shall be initialized to values other than zero.

(snuck in an editorial correction there, too!)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #454.

Cl **175** *SC* **175.2.4.5** *P* **174** *L* **3** # 377

Ofelt, David — Juniper Networks

Comment Type **T** *Comment Status* **A** *Scrambler seeds (bucket)*

Editor's Note askes if we should require different reset values for the scramblers.

SuggestedRemedy

Yes, we should!

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #454.

Cl **175** *SC* **175.2.4.5** *P* **174** *L* **3** # 454

Opsasnick, Eugene — Broadcom

Comment Type **T** *Comment Status* **A** *Scrambler seeds (bucket)*

The Editor's note at the end of subclause 175.2.4.5 "Scrambler" states that there are no requirements or restrictions in the 1.6TE PCS baselines for the scrambler seeds for each flow. The note also mentions that the corresponding sub-clause in 802.3df for 800GE PCS states that the two flows would have identical outputs if the seeds are identical and the data input is identical (such as after reset). The 1.6TE PCS does not have two separate sets of PCSLs like 800GE PCS, but the PCSL formation could have back-to-back repeating RS-symbol values if identical seeds are used. Suggest to require different seeds after reset in the scramblers of each flow as written in the paragraph above the editor's note.

SuggestedRemedy

Remove the editor's note at the top of page 174, and leave the wording in 175.2.4.5 as-is with the requirement that the two scrambers are initialized with different seeds.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Comment #331 notes that the 1.6T PCS lanes are never bit-muxed so different seeds may not be necessary. While the effect of identical scrambler seeds is worse with bit-muxing than symbol-muxing, there may still be some determental effects with symbol muxing. If there are identical seeds and identical data, then the FEC-A and FEC-B codewords would be identical to the FEC-C and FEC-D codewords, respectively. With symbol muxing, the resulting data on a output lane would be symbols {A, B, C, D} where A=C and B=D.
In general, it is safer to require different seeds to avoid any potential side-affect. As the comment #331 points out, it doesn't hurt to have the scramblers seeded differently.

Delete the editor's note near top of page 174.

Cl **175** *SC* **175.2.4.6** *P* **174** *L* **42** # 464

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **R** *(bucket)*

tx_am_sf doesn't allow but provides a way to communicate the mandatory degrade status.

SuggestedRemedy

Change "allows the local PCS to communicate the status of the FEC degraded feature to the remote PCS" to "communicates the local PCS FEC degraded status to the remote PCS".

Response *Response Status* **C**

REJECT.
The draft is correct as written, and the proposed change does not improve clarity.

Cl **175** *SC* **175.2.4.6** *P* **175** *L* **22** # 453

Opsasnick, Eugene Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

Sub-clause 172.2.4.6 has a reference to a text file containing the 800GBASE-R alignment marker values. CL 175 should add a similar note with a corresponding text file for the 1.6TBASE-R alignment markers.

SuggestedRemedy

Add text near line 22: "NOTEùA text file containing the alignment marker patterns, as shown in Table 175û1 is available at https://standards.ieee.org/downloads/802.3/."

A presentation will be submited with a corresponding text file containing the 1.6TBASE-R AM values.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Add note as suggested with additional reference to the text file from the May interim (https://www.ieee802.org/3/dj/public/24_05/opsasnick_3dj_02_2405.txt) as presented in https://www.ieee802.org/3/dj/public/24_05/opsasnick_3dj_01_2405.pdf
Implement with editorial license.

Cl **175** *SC* **175.2.4.6** *P* **176** *L* **5** # 465

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

am_mapped_f0 and am_mapped_f1 aren't solely based on the 10b-distribution and we never talk about how this two variables are us splitting the alingment marker group up.

SuggestedRemedy

Change:
ôThe variables am_mapped_f0 and am_mapped_f1 are then derived from 10-bit interleaving the group of 16 alignment markers, am_x, using the following procedureö
To:
ôThe alignment marker group is mapped into variables am_mapped_f0 and am_mapped_f1 as follows. First a 10-bit interleaving the group of 16 alignment markers, am_x, is done using the following procedure ô

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **175** *SC* **175.2.4.6** *P* **176** *L* **25** # 466

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

am_mapped_f0 and am_mapped_f1 contain data that is sent into flow 0/1 and through codewords AB and CD.

SuggestedRemedy

Change:
ôNote that am_mapped_f0 contains the 10-bit symbols of FEC codewords A and B, and am_mapped_f1 contains the 10-bit symbols of FEC codewords C and D. ô
To:
ôNote that am_mapped_f0 is sent to flow 0 which produces FEC codewords A and B, and am_mapped_f1 is sent to flow 1 which produces FEC codewords C and D.ö

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **175** *SC* **175.2.4.6.2** *P* **177** *L* **6** # 467

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

Add a intro to what tx_scrambled is.

SuggestedRemedy

Change:
"The variables tx_scrambled_am_f0<10279:0> and
tx_scrambled_am_f1<10279:0> are constructed in one of two ways."
To:
"In each flow a 10280-bit block of data is formed with two FEC codewords worth of message data, tx_scrambled_am_f0<10279:0> in flow 0 and
tx_scrambled_am_f1<10279:0> in flow 1 and they are constructed in one of two ways. "

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **175** *SC* **175.2.5.3** *P* **181** *L* **40** # 468

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *FEC error counters*

The counters for correctd, uncorrected and error have always been mandatory, while the cw counter and bin counters have been optional. So Should is not appropiate.

SuggestedRemedy

Change:
"The following counters should be implemented to aid a network operator in determining the link quality. "
To:
"The PCS provides the following counters that track FEC decoder statistics."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
There is a list of 5 FEC counters in 175.2.5.3.
The first three are definitely required (as they were also required in CL 91, 108, 119, 134, and 172) which makes the "should" wording incorrect.
(FEC_corrected_cw_counter, FEC_uncorrected_cw_counter, and FEC_symbol_error_counter_i)
The 4th and 5th counters (FEC_cw_counter and FEC_codeword_error_bin_i) are explictly "optional" in 161.6.21, 172.3.5 and 172.3.6.
The importance of these counters is well recognized in the industry so should be mandatory for the 1.6TBASE-R PCS
Make all 5 counters required for the 1.6TBASE-R PCS.
Implement with editorial license.

Cl **175** *SC* **175.2.5.3** *P* **182** *L* **9** # 469

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

The Note about tracking statistics across all 4 decoders is missing from the bin counter.

SuggestedRemedy

Add this to the definition of the FEC_codeword_error_bin_i
"Note that this counter tracks codewords with errors across all four codewords."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **175A** *SC* **175A** *P* **539** *L* **8** # 455

Opsasnick, Eugene Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

Annex 175A contains tabular data for an example created by the 1.6TBASE-R PCS TX functions, including the scrambler output, RS-FEC codeword generation, and PCS lane interleaving. The editor's note on page 539 has a placeholder for a link to a text file that has the machine readable text data. That data file needs to be created.

SuggestedRemedy

A presentation is planned to submit a data file which corresponds to the Annex 176A example and can be referenced in the editor's note

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Update the Editor's note with link to the text file (https://www.ieee802.org/3/dj/public/24_05/opsasnick_3dj_03_2405.txt) as presented in https://www.ieee802.org/3/dj/public/24_05/opsasnick_3dj_01_2405.pdf at the May interim.
Implement with editorial license.

Cl **176** *SC* **176** *P* **195** *L* **1** # 597

de Koos, Andras — Microchip Technology

Comment Type **T** *Comment Status* **R** *timesync (bucket1p)*

Has any thought been put into how to calculate the path data delay values (MII-MDI latencies for timestamping) for the SM-PMAs? For bit-mux PMAs, it is very simple - i.e. it is all implementation delay, since the intrinsic delay from bit muxing/demultiplexing is negligible. But at first glance, determining the latency across the Clause 176 PMA looks like more of a challenge.

a. I don't believe that the intrinsic (i.e. non-implementation) delay is deterministic, due to the partial deskew.

b. But apart from the partial deskew, the latency across the SM-PMA should be deterministic using the principles in Annex 90A.7 (max latency value used for Tx path data delay, min latency value used for Rx path data delay).

c. Traditionally, how to calculate the delays through the PHY layers has been an implementation concern, but this is because the calculation was straightforward at lower rates. At 200Gbps lanes, the standard does not have the luxury of being able to ignore this. If it is overly complicated or ambiguous, and opposite ends of a link do not implement it in the same fashion, the system Time Synchronization will be impaired.

SuggestedRemedy

Consider a note in Clause 176 (or next to the PMA path data delay MDIO registers - 45.2.1.176, 45.2.1.177) that the path data delay values for the SM-PMA should be calculated via the method in Annex 90A.7.
I don't think it is necessary, but if a more detailed explanation is deemed useful, then a subclause could be added to Clause 90.7 spelling out explicitly how the path data delay values should be calculated for the SM-PMA.

Response *Response Status* **C**

REJECT.

As mentioned in the suggested remedy, it would be preferable to make any necessary updates to Clause 90/Annex 90A. It may also be beneficial to add appropriate references to Clause 90/Annex 90A in the Physical Layer clause tables in all the PMD subclauses, to make it clear that Clause 90/Annex 90A are optional for the associated PHY.

There is no consensus to make a change at this time.

A consensus presentation with a complete proposal is encouraged.

Cl **176** *SC* **176** *P* **242** *L* **10** # 21

Liu, Cathy — Broadcom

Comment Type **T** *Comment Status* **A** *Precoding*

In this section, precoding is mentioned to CR, KR and C2C links. How about C2M link? It should add C2M since C2M LT session specifies precoding as one of the options.

SuggestedRemedy

Add C2M link into the statement: ôThe precoding specifications in this subclause apply to the input and output lanes of a PMA that are connected to the service interface of an xBASE-CRn or xBASE-KRn PMD, or are part of an xAUI-n C2C/C2M link.ö

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Background and proposed changes are provided on slides 4 to 10 in the the following presentation:
https://www.ieee802.org/3/dj/public/24_06/brown_3dj_02_2406.pdf

Implement the proposed text on slide 4 of brown_3dj_02_2406.
Implement with editorial license.

Cl **176** *SC* **176.2** *P* **196** *L* **46** # 471

Slavick, Jeff — Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

Is respectively necessary here? X is just a list of different rates.

SuggestedRemedy

remoe the ", repsectively,"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.2** *P* **196** *L* **53** # 472

Slavick, Jeff — Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

Is respectively necessary here? X is just a list of different rates.

SuggestedRemedy

remoe the ", repsectively"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.2** *P* **197** *L* **3** # 473

Slavick, Jeff Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

Is respectively necessary here? X is just a list of different rates.

SuggestedRemedy

remoe the '', repsectively"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.5.1.1** *P* **200** *L* **1** # 533

Rechtman, Zvi Nvidia

Comment Type **TR** *Comment Status* **R** *DelayOddPCSLs (bucket)*

The comment refers to Figure 176û2.
The functions of "Delay odd PCSLs
by 2 RS-FEC codewords" on Tx path and "Delay even PCSLs by 2 RS-FEC codewords" can be misleading, as they could be interpreted as a delay by 10,880 symbols.
The intention is to delay the odd (Tx) and even (Rx) PCSLs by 136 symbols in order to get multiplex and demultiplex symbols from different 2 RS-FEC CWs.
Same apply to Figure 176û9

SuggestedRemedy

Modify the description in the Tx path box from "Delay odd PCSLs by 2 RS-FEC codewords" to "Delay odd PCSLs by 136 symbols" and in the Rx path box from "Delay even PCSLs by 2 RS-FEC codewords" to "Delay even PCSLs by 136 symbols"

Response *Response Status* **C**

REJECT.
The function in Fig 176-2 uses the words "2 RS-FEC codewords" as opposed to "136 RS-FEC symbols" because the function aims to align the 2 codewords on even lanes with 2 different codewords on odd lanes by delaying odd lanes by 2 codewords. This enables symbol multiplexing across 4 codewords. Same applies to Fig 176-9, 176-11 and 176-13.
While it is not inaccurate to call it a "136 symbol delay", an advantage of using "2 RS-FEC codewords" as opposed to "136 symbols" is that the function name is equally applicable to both 200GE and 400GE SM-PMAs. Moreover, the first line of subclause 176.5.1.3.4 clearly specifies the delay as being 136 RS-FEC symbols, and the subsequent line shows this mathematically as "2 codewords × 544 symbols per codeword / 8 PCS lanes = 136 symbols." Similarly, subclause 176.6.1.2.4 (400GE 16:2 PMA) specifies the delay to be 68 symbols. Hence, the delay value is clearly specified and there is no room for misinterpreration.
The comment proposes an alternate description which is technically correct but does not improve the accuracy or readability of the standard.

Cl **176** *SC* **176.5.1.1** *P* **200** *L* **11** # 367

He, Xiang Huawei

Comment Type **TR** *Comment Status* **A** *Deskew (logic)*

20b deskew is incorrect. According to Motion #10 in https://www.ieee802.org/3/dj/public/23_07/motions_3cwdfdj_2307.pdf, it is required to deskew to codeword boundaries.

SuggestedRemedy

Change "20b deskew" to "deskew to codeword boundaries" or simply "deskew"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 368

Cl **176** *SC* **176.5.1.1** *P* **200** *L* **35** # 478

Slavick, Jeff Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

test pattern generate is overlapping with the IS_SIGNAL_requst line in Figure 176-2

SuggestedRemedy

Move "test pattern genrate" to not overlap with the inst.IS_SIGNAL.request line
Same in Figure 176-9,10,13,14,15,19,20,24,25,26

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.5.1.1** *P* **200** *L* **35** # 479

Slavick, Jeff Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

test pattern generate is overlapping with the IS_SIGNAL_requst line in Figure 176-2

SuggestedRemedy

Move "test pattern genrate" to not overlap with the inst.IS_SIGNAL.request/indication line
Same in Figure 176-9,10,13,14,15,19,20,24,25,26

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.5.1.3.1** *P* **201** *L* **24** # 594

de Koos, Andras Microchip Technology

Comment Type **T** *Comment Status* **A** *Deskew (logic)*

Functionally, is there anything preventing the SM-PMAs from performing a full deskew instead of only to 20/40-bit boundaries?
A full deskew at the SM-PMA would NOT change end-to-end latency, since the skew is all untimately undone at the Rx PCS.
Keeping the PMA as light as possible (less buffering required) is OK, but if an implementation chooses to do so, performing a full deskew (i.e. to AMs, or CW boundaries) should be allowed for both Rx and Tx.

SuggestedRemedy

Add the following note the 20/40 bit deskew clauses (176.5.1.3.1, 176.6.1.2.1, 176.7.1.2.1, 176.8.1.2.1):
Full deskew (to AM boudaries) of PCSLs may optioanlly be performed by the SM-PMA transmit function.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolve using the response to comment # 368

Cl **176** *SC* **176.5.1.3.1** *P* **201** *L* **24** # 598

de Koos, Andras Microchip Technology

Comment Type **T** *Comment Status* **A** *Deskew (logic)*

Skew in series within the PHY sub-layers may not have deterministic sum, making accurate path data delay calculation impossible. See Annex 90A.6 for a more detailed explanation.
Towards the MDI, the transmit SM-PMA function should thus have the option to undo any skew introduced by the Tx PCS layer and AUI links. (i.e. do a full de-skew).
In the Rx direction, the same problem exists. If the SM-PMA does not do a full deskew, then the remaining skew, in series with skew from other layers in the PHY (from AUIs, for example) and from the medium, will have a non-deterministic sum.
Adding an option for the SM-PMA to do a full deskew (not just a 20/40-bit deskew) would be a way to allow implementations to avoid the TimeSync impairment due to skew between the PHY layers.
This is a lot to digest - I can present the reasoning here if leadership thinks it would be worthwhile.

SuggestedRemedy

Consider requiring (or allowing as an option) a full deskew instead of the 20/40 bit deskew in clauses (176.5.1.3.1, 176.6.1.2.1, 176.7.1.2.1, 176.8.1.2.1).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #368.

Cl **176** *SC* **176.5.1.3.1** *P* **201** *L* **24** # 596

de Koos, Andras Microchip Technology

Comment Type **T** *Comment Status* **A** *Deskew (logic)*

In the AM lock and deskew clauses, is a full deskew not necessary? The goal of the Clause 176 PMA, if I understand correctly, is that at the output lane(s), each set of 4 consecutive 10-bit symbols must come from 4 different RS-FEC codewords. In the current draft, this is not achieved.

Without skew, everything works because the symbol delay is in the same direction as the FEC CW delay. But with n*20b of skew, where some odd PCSLs arrive before even PCSLs, after the 10bit delay on odd PCSLs, (Clause 176.5.1.3.4) and the 2 CW delay (Clause 176.5.1.3.4), there will still be a period of overlap where symbols from the same FEC codeword appear at the same time. Symbols from the same RS_FEC CW can thus appear within 2 symbols after the output mux.

Before skew (showing boundary between FEC words 1 and 2):
PCSL0: B2 A2 B1 A1 B1 A1
PCSL1: A2 B2 A1 B1 A1 B1

20-bit skew : PCSL1 arrives before PCSL0 (when PCSL0 is finishing A1/B1, PCSL1 has already started A2/B2)
PCSL0: B2 A2 B1 A1 B1 A1
PCSL1: A2 B2 A1 B1 A1 B1

10-bit delay on odd lane (Clause 176.5.1.3.4):
PCSL0: B2 A2 B1 A1 B1 A1
PCSL1: A2 B2 A1 B1 A1 B1

2 FEC CW delay on odd lane (Clause 176.5.1.3.4):
PCSL0: B2 A2 B1 A1 B1 A1
PCSL1: A1 B1 A0 B0 A0 B0
-> B1s line up on PCSL 0 and 1 for one 8:1 two-symbol mux cycle.

with more than 20 bits of skew, there will be more "codeword overlap".

Adding a "full deskew" may not be too costly.
Or, is this potential overlap due to skew understood and planned for in the AUI/PMD loss budgets?

SuggestedRemedy

Consider requiring a full deskew instead of the 20/40 bit deskew in clauses (176.5.1.3.1, 176.6.1.2.1, 176.7.1.2.1, 176.8.1.2.1).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

For the 800GBASE-R and 1.6TBASE-R PMAs, the 20bit and 40bit deskew provides sufficient alignment to ensure 4 Codeword interleaving on output lane of the PMAs and

therefore no changes to the deskew function are required.

For 200GBASE-R and 400GBASE-R resolve using the response to comment #368.

Cl **176** *SC* **176.5.1.3.1** *P* **201** *L* **28** # 534

Rechtman, Zvi Nvidia

Comment Type **T** *Comment Status* **A** *(bucket)*

There is reference in the text to lock process in Figure 119-12. However, there are exceptions to Figure 119-12 as outlined in 176.5.1.6.
It can be beneficial to refer to 176.5.1.6 which include both the reference to Figure 119-12 and the list of exceptions list

SuggestedRemedy

Add a reference to 176.5.1.6 instead of Figure 119-12

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add note in parenthesis "(see 176.5.1.6.4)" after Fig 119-12.

Implement with editorial license.

Cl **176** *SC* **176.5.1.3.1** *P* **201** *L* **29** # 475

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

There is more details to the AM lock function add a reference

SuggestedRemedy

add a "(see 175.5.1.6.4)" after Table 119-1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #534.

[Editor's note: Changed clause, subclause from 175, 175.5.1.3.1 to 176, 176.5.1.3.1]

Cl **176** *SC* **176.5.1.3.1** *P* **201** *L* **32** # 368

He, Xiang Huawei

Comment Type **TR** *Comment Status* **A** *Deskew (logic)*

20b deskew is incorrect. According to Motion #10 in https://www.ieee802.org/3/dj/public/23_07/motions_3cwdfdj_2307.pdf, it is required to deskew to codeword boundaries.

SuggestedRemedy

Remove the second and third paragraph in 176.5.1.3.1 and reuse 119.2.5.1.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The presentation https://www.ieee802.org/3/dj/public/24_06/shrikhande_3dj_01a_2406.pdf was reviewed by the CRG.

Implement Option 3 as described in slide 11 of shrikhande_3dj_01a_2406 and add a statement that full deskew to alignment markers is a valid 4-codeword boundary.

Implement with editorial license.

Cl **176** *SC* **176.5.1.3.3** *P* **202** *L* **45** # 535

Rechtman, Zvi Nvidia

Comment Type **T** *Comment Status* **A** *(bucket)*

The comment refers to Figure 176-4
The diagram represent a specific skew case between PCS lane, for instance in the absence of skew between the original PCS lanes, the "first" symbol A might be created by different A codeword which should be denote by A'.

SuggestedRemedy

Option1:
Modify only the first A symbol of the odd PCS lanes to be A'.
Option2:
Split the drawing into two: one for 200GBASE-R and another for 400GBASE-R. Then, add index numbers to the A, B symbols.
This could make it easier to understand the drawings and the roles of the symbols in each context.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Update the text referencing Fig 176-4 (in 176.5.1.3.3) and Fig 176-3 (in 176.5.1.3.2) to state that the RS-FEC symbols A and B belong to FEC-A and FEC-B. The "A" symbols could be from the same or different FEC-A codewords and the "B" symbols could be from the same or different FEC-B codewords.
Implement with editorial license.

Cl **176** *SC* **176.5.1.3.4** *P* **202** *L* **48** # 599

de Koos, Andras — Microchip Technology

Comment Type **T** *Comment Status* **R** *(bucket)*

The SM-PMA adds a lot of latency due to the 2x RS-FEC CW delay in the 8:1 and 16:2 SM-PMAs, as compared to the bit-mux PMAs
For setups with an MII-Extender it is actually worse, since the penalty would also exist between the DTE_XS and PHY_XS. If latency is a concern, it actually becomes preferable to use 100Gbps links for the DTE_XS <-> PHY_XS AUI interface, negating the advantages of 200Gbps links!
The latency penalty for the 8:1 and 16:2 PMAs should be noted in Clauses 176.5.1.3.4 and 176.6.1.2.4.

SuggestedRemedy

Add the following note to the 2xFEC CW delay sub-clauses (176.5.1.3.4 and 176.6.1.2.4):
Note that the delay added to the odd PCSLs (and to the even PCSLs at the far-end) causes an end-to-end latency increase of 51.4ns as compared to BM-PMAs.

Response *Response Status* **C**

REJECT.
The standard is not expected to note pros and cons of one PMA versus another (in this case the latency of SM-PMA versus a BM-PMA).
The comment proposes a change that does not improve the clarity or accuracy of the draft.

Cl **176** *SC* **176.5.1.3.4** *P* **202** *L* **51** # 537

Rechtman, Zvi — Nvidia

Comment Type **TR** *Comment Status* **R** *DelayOddPCSLs (bucket)*

The sentence "This is equivalent to adding a delay of 2 RS-FEC codewords to the odd PCS lanes (2 codewords Î 544 symbols per codeword / 8 PCS lanes = 136 symbols)."
can be misinterpreted:
136 symbol delay x 4 odd PCS lanes = 544 symbols delay in total (not 2 RS-FEC codewords delay)

SuggestedRemedy

Remove "This is equivalent to adding a delay of 2 RS-FEC codewords to the odd PCS lanes (2 codewords Î 544 symbols per codeword / 8 PCS lanes = 136 symbols)."

Modify: "Adding the two codeword delay to odd numbered lanes enables the multiplexing of four consecutive RSFEC symbols from four different codewords at the output of the 8:1 symbol multiplexer."
To: "Adding the 136 symbol delay to odd numbered lanes enables the multiplexing of four consecutive RSFEC symbols from four different codewords at the output of the 8:1 symbol multiplexer."

Response *Response Status* **C**

REJECT.
The first line of subclause 176.5.1.3.4 clearly specifies that the odd lanes are delayed by 136 RS-FEC symbols, and the subsequent line describes mathematically that this (136 symbol delay) is equivalent to adding a delay of 2 codewords to the odd lanes by showing that "2 codewords × 544 symbols per codeword / 8 PCS lanes = 136 symbols". There is little room left for misinterpretation, since the delay in symbols is stated upfront.

Cl **176** *SC* **176.5.1.3.4** *P* **203** *L* **4** # 293

Galan, Jose Vicente — Maxlinear Inc

Comment Type **T** *Comment Status* **A** *Figures (bucket)*

For Figure 176û5 , it has to be explained what AÆ/BÆ shall be.

SuggestedRemedy

Add an explanation for AÆ/BÆ, e. g. ''AÆ/BÆ'are the symbols from previous 2 CWs that are delayed''

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Update the text referencing Fig 176-5 (in 176.5.1.3.4) to state that RS-FEC symbols A and A' belong to different codewords from FEC-A, and B and B' belong to different codewords from FEC-B.
Implement with editorial license.

Cl **176** *SC* **176.5.1.3.4** *P* **203** *L* **45** # 536

Rechtman, Zvi — Nvidia

Comment Type **T** *Comment Status* **A** *Figures (bucket)*

The comment refers to Figure 176-5
The diagram represents a specific skew case between PCS lanes. For instance in the absence of skew between the PCS lanes in the PMA:IS_UNITDATA_0:7.request primitive, the first symbol of A' of the odd PCS lane should be marked as A'' because of the additional one symbol delay prior to the 136 symbols delay

SuggestedRemedy

Option1:
Modify only the first A' symbol of the odd PCS lanes to be A''.

Option2:
Split the drawing into two: one for 200GBASE-R and another for 400GBASE-R. Then, add index numbers to the A, B and A', B' symbols.
This could make it easier to understand the drawings and the roles of the symbols in each context.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 293

Cl **176** *SC* **176.5.1.3.5** *P* **203** *L* **25** # 476

Slavick, Jeff — Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

It's a multiplexor or a multiplexing function

SuggestedRemedy

add the word function after multiplexing

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.5.1.3.5** *P* **204** *L* **1** # 291

Galan, Jose Vicente — Maxlinear Inc

Comment Type **T** *Comment Status* **A** *Figures (bucket)*

In Figure 176-6, the output lane arrow is indicated in the opposite direction than the actual transmission order of the output PCSL symbols

SuggestedRemedy

Change the direction of the arrow to follow the actual transmission order.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Update Fig 176-6 to clarify the order of transmission on the output lane, with editorial license.

Cl **176** *SC* **176.5.1.4.2** *P* **204** *L* **42** # 595

de Koos, Andras — Microchip Technology

Comment Type **T** *Comment Status* **R** *Deskew (bucket)*

Is there anything preventing an implementation from performing a full deskew at the Rx PMA? It is not technically required, but does not cause any adverse functional effects.
A full deskew at the Rx SM-PMA would NOT change end-to-end latency, since the skew is all untimately undone at the Rx PCS. A deskew upstream would simply offload the deskew from the Rx PCS.
Implementations with a SM-PMA attached to an RxPCS will undoubtedly perform the Alignment marker lock only once (not once in the PMA and again in the PCS). AM-lock plus deskew is a very natural coupling of functions.

SuggestedRemedy

Consider adding the following note to the Rx Alignment marker lock clauses (176.5.1.4.2, 176.6.1.3.2, 176.7.1.3.2, 176.8.1.3.2):
After the Alignment Marker lock, no deskew of the PCSLs is required. However, deskewing the PCSLs before the would not have and adverse functional effects.

Response *Response Status* **C**

REJECT.
An implementation of the PMA Rx could deskew the PCS lanes during alignment lock (as the comment suggests). However this is an implemention choice, and should not be called out in the standard.

Cl **176** *SC* **176.5.1.5** *P* **205** *L* **20** # 484

Slavick, Jeff Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

Detailed functions and state diagrams has no content

SuggestedRemedy

Change 176.5.1.6 to be a sub-heading of 176.5.1.5 (4th tier I think).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.5.1.6.1** *P* **205** *L* **31** # 485

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *Reorg*

The Variables state that these all of them, not inheriting Cl119 functions except for some replacements.

SuggestedRemedy

Copy Figure 119-12 into Cl 176 and modify it to use:
restart_lock_dir **with dir in italics **
amps_lock_dir ** with dir in italics **
pcs_lane_mapping_dir ** with dir in italics **
add a NOTE that italics dir is either mux or demux

In Variables, Constants and Counters sections define everything that is used, referring to Cl 119 when possible.

Change referenes to Figure 119-12 to point to the new figure.

With editorila license

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 80.

Cl **176** *SC* **176.5.1.6.1** *P* **208** *L* **14** # 487

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *Reorg*

To support 400G also using the same state machines we need to make Figure 176-8 and the definition of symbol_pair_lock_demux have a <y> in it.

SuggestedRemedy

Add a <y> to symbol_pair_lock_demux defintion and in Figure 176-8. Upate the definition in 176.5.1.6.1 for symbol_pair_lock_demux<y> to have a range of of y=0

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 80.

Cl **176** *SC* **176.5.1.6.4** *P* **206** *L* **38** # 474

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

Figure 119-12 uses functions and variables defined in CL119 but those aren't called out to be used, just that restart_lock_mux is used to replace restart_lock

SuggestedRemedy

add "using the state variables defined in 119.2.6.2" after Table 119-1 with edtiorial license

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **176** *SC* **176.5.1.6.5** *P* **206** *L* **48** # 477

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

Figure 119-12 uses functions and variables defined in CL119 but those aren't called out to be used, just that restart_lock_mux is used to replace restart_lock

SuggestedRemedy

add "using the state variables defined in 119.2.6.2" after Table 119-1 with edtiorial license

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.

Cl **176** *SC* **176.5.1.6.5** *P* **208** *L* **9** # 483

Slavick, Jeff Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

I think it's best if the Start of the counter is the last thing in the Box

SuggestedRemedy

Move "Start symbol_pair_lock_counter_demux" to be the last thing in LOSS_OF_SYMBOL_PAIR_LOCK box

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.5.1.6.5** *P* **208** *L* **11** # 482

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *(bucket)*

Counter _done needs to be at the end of the counter name.

SuggestedRemedy

Change symbol_pair_lock_counter_done_demux to symbol_pair+lock_counter_demux_done

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
In Fig 176-8, change "symbol_pair_lock_counter_done_demux" to "symbol_pair_lock_counter_demux_done". Remove the definition of the variable "symbol_pair_lock_counter_done_demux" from 176.5.1.6.1. Implement with editorial license.

Cl **176** *SC* **176.5.1.6.6** *P* **207** *L* **6** # 378

Ofelt, David Juniper Networks

Comment Type **T** *Comment Status* **R** *(bucket)*

Should there be an arc from ALIGNMENT_FAIL to LOSS_OF_ALIGNMENT?

SuggestedRemedy

If so, add the arc

Response *Response Status* **C**

REJECT.
In the ALIGNMENT_FAIL state, restart_lock_mux is set to true which results in AM lock process of Fig 119-12 to be restarted on all lanes. This results in all_locked_mux to be set to false, which causes the state machine of 176-7 to go from ALIGNMENT_FAIL to LOSS_OF_ALIGNMENT state.

Cl **176** *SC* **176.5.1.6.6** *P* **208** *L* **34** # 538

Rechtman, Zvi Nvidia

Comment Type **TR** *Comment Status* **A** *Reorg*

The comment refers to Figure 176û8ùPMA receive symbol-pair lock state diagram
The state diagram is defined as single state machine per the entire PMA. However, each PMA lane may have a different reference skew, leading to varying SLIP operation requirements per PMA lane (e.g. one PMA lane doesn't require SLIP because all PCS lanes of that lane are locked, but other PMA lane still need to skew to find the 20 symbol bit boundaries)therefore the state diagram should be define per PMA lane and not for per PMA.

SuggestedRemedy

Modify the state diagram per PMA lane and not per PMA, this include change in the variables to be defined per <y>:
restart_lock_demux<y>
symbol_pair_lock_demux<y>
start symbol_pair_lock_counter_demux<y>
symbol_pair_lock_demux<y>

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 80.

Cl **176** *SC* **176.5.2** *P* **208** *L* **40** # 601

de Koos, Andras Microchip Technology

Comment Type **E** *Comment Status* **A** *(editorial)*

Is specifying the 1:8 SM-PMA really necessary? Apart from the layers it attaches to and the labels on the interfaces, it is identical to the 8:1 PMA. Same thing for 16:2 vs 2:16 for 400G, 32:4 vs 4:32 for 800G, and 16:8 vs 8:16 for 1.6T.
Alternately, could SM-PMAs be specified unidirectionally, rather than specifying transmit and receive? So 8:1 would only specify the PCS-PMD direction, and 1:8 would specify the PMD-PCS direction.
Having so many sub-clauses that just point to other sub-clauses is an easy way to cause confusion.

SuggestedRemedy

Consider specifying the 1:8 and 8:1 (and equivalent SM-PMAs for other rates) together.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.6** *P* **213** *L* **1** # 600

de Koos, Andras Microchip Technology

Comment Type **E** *Comment Status* **A** *(editorial)*

Would it not be possible to merge Clause 176.5 and 176.6? They are 95% similar, so repeating everything is hardly necessary.
Even the figures for 200GBASE-R SM-PMA (Figure 176û3, Figure 176û4, Figure 176û5) have a general form with a variable number of PCSLs that are suitable for 400GBASE-R

SuggestedRemedy

Consider merging subclauses 176.5 and 176.6

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.6.1** *P* **213** *L* **4** # 602

de Koos, Andras Microchip Technology

Comment Type **E** *Comment Status* **A** *(editorial)*

Clauses 176.6, 176.7 and 176.8 are missing the 'overview' sub-clauses (with tables) that exist in Clause 176.5 (e.g. 176.5.1.1). The equivalent content is there but is placed directly in each PMA sub-clause (e.g. 176.6.1)

SuggestedRemedy

Structure the subclauses consistently between 200GBASE-R and 400GBASE-R, 800GBASE-R, 1.6TBASE-R.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.6.1** *P* **213** *L* **5** # 80

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *Reorg*

The 800G 32:4 PMA, 400G 16:2 PMA and the 200G 8:1 PMA are basically the same, other than the numbers of lanes. The 1.6T 16:8 is different since it has 40b deskew and 4-symbol interleaving. All of the PMAs with the same number of lanes on both sides are essentially the same. It would simplify maintenance and likely reader understanding as well if the number of lanes were parameterized as m and n

SuggestedRemedy

Reorganize 176.5 through 176.8 into 3 clauses: one for 200/400/800 m:n PMAs, one for 1.6T m:n PMAs, and one for 200/400/800/1.6T m:m PMAs, and use a single set of text and figures with the parameters m and n for the number of lanes. Include a table showing PHY rates and the values of m an n (e.g, with columns PHY, m, and n, and rows 200GBASE-R, 8, 1; 400GBASE-R, 16, 2; etc.).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Reorganize the Clause to reduce repetition of text and figures, and make the state diagrams more generic across the SM-PMAs.
Implement with editorial license.

Cl **176** *SC* **176.6.1** *P* **214** *L* **53** # 539

Rechtman, Zvi Nvidia

Comment Type **TR** *Comment Status* **R** *DelayOddPCSLs (bucket)*

The comment refers to Figure 176û11.
The functions of "Delay odd PCSLs
by 2 RS-FEC codewords" on Tx path and "Delay even PCSLs by 2 RS-FEC codewords" can be misleading, as they could be interpreted as a delay by 10,880 symbols.
The intention is to delay the odd (Tx) and even (Rx) PCSLs by 68 symbols in order to get multiplex and demultiplex symbols from different 2 RS-FEC CWs.
Same apply to Figure 176û13

SuggestedRemedy

Modify the description in the Tx path box from "Delay odd PCSLs by 2 RS-FEC codewords" to "Delay odd PCSLs by 68 symbols" and in the Rx path box from "Delay even PCSLs by 2 RS-FEC codewords" to "Delay even PCSLs by 68 symbols"

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #533.

Cl **176** *SC* **176.6.1.2.1** *P* **215** *L* **22** # 486

Slavick, Jeff — Broadcom

Comment Type **T** *Comment Status* **A** *Reorg*

The deskew process doesn't need an exception since the referred texts says to do it across "ALL" PCSLs

SuggestedRemedy

Remove the deskew across 16 lanes exception in 176.6.1.2.1
Remove the deskew across 32 lanes exception in 176.7.1.2.1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 80.

Cl **176** *SC* **176.6.1.2.5** *P* **216** *L* **1** # 290

Galan, Jose Vicente — Maxlinear Inc

Comment Type **T** *Comment Status* **A** *Figures (bucket)*

In Figure 176-12, the output lane arrow is indicated in the opposite direction than the actual transmission order of the output PCSL symbols

SuggestedRemedy

Change the direction of the arrow to follow the actual transmission order.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Update Fig 176-12 to clarify the order of transmission on the output lane, with editorial license.

Cl **176** *SC* **176.7.1** *P* **221** *L* **20** # 379

Maniloff, Eric — Ciena

Comment Type **E** *Comment Status* **A** *(editorial)*

Table 176-7 Includes two references to 400GBASE-R, these should be replaced with 800GBASE-R

SuggestedRemedy

Replace the text "400GBASE-R" with "800GBASE-R" in Table 176-7.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.7.1.2.2** *P* **223** *L* **39** # 459

Opsasnick, Eugene — Broadcom

Comment Type **T** *Comment Status* **A** *Figures (bucket)*

In Figure 176-16 and Figure 176-17, on the following page, the symbol pattern of the even PCSLs in the upper half (PCSL 16-31) is not shown. It would be easier to see the RS symbol patterns if the figures included at least one even PCSL in the range of 16-31.

SuggestedRemedy

These two figures show PCSLs for lanes 0,1, and 31. Suggest to show the PCSL sybol pattern for lanes 0,1,à15, 16, 17,à31.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **176** *SC* **176.7.1.2.2** *P* **223** *L* **52** # 593

de Koos, Andras — Microchip Technology

Comment Type **T** *Comment Status* **A** *Figures (bucket)*

The 800GBASE-R PCS has 4 FEC engines, so figures 176û16, 176û17, 176û18 should use C,D to illustrate the symbols on PCSLs 16-31, rather than A',B'. The A',B' notation is used in 200GBASE-R and 400GBASE-R figures to denote CWs from engines A and B but with the 2CW delay.

SuggestedRemedy

Ammend Figures 176û16, 176û17, 176û18 to avoid the A',B' notation

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Clause 176 avoids using "C" or "D" for 800GBASE-R PMAs because Clause 172 (800GBASE-R PCS) does not use FEC-C and FEC-D. Whereas, "C" and "D" are used in 1.6TBASE-R PMAs because Clause 175 (1.6TBASE-R PCS) uses FEC-C and FEC-D. However, the clarity of the draft will be improved by defining what A, B, A', B' are in the figures Fig 176-16, 176-17 and 176-18.
Therefore, implement the following:
Update the text referencing figures Fig 176-16, Fig 176-17 and 176-18 (in 176.7.1.2) to state the RS-FEC symbols A and B are from FEC-A and FEC-B in flow 0 of the 800GBASE-R PCS, while the RS-FEC symbols A' and B' are from flow 1 of the 800GBASE-R PCS.
Implement with editorial license.

Cl **176** *SC* **176.7.1.2.2** *P* **224** *L* **38** # 294

Galan, Jose Vicente Maxlinear Inc

Comment Type **T** *Comment Status* **A** *Figures (bucket)*

In all Figures in the 800G PMA section, it is referred to AÆ/BÆ symbols, although we have 4 RS CWs

SuggestedRemedy

Change to use A,B,C,D for the 4 RS CWs, instead of A, B, AÆ, BÆ

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 593

Cl **176** *SC* **176.7.1.2.4** *P* **225** *L* **1** # 289

Galan, Jose Vicente Maxlinear Inc

Comment Type **T** *Comment Status* **A** *Figures (bucket)*

In Figure 176-18, the output lane arrow is indicated in the opposite direction than the actual transmission order of the output PCSL symbols

SuggestedRemedy

Change the direction of the arrow to follow the actual transmission order.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Update Figure 176-18 to clarify the order of transmission on the output lane, with editorial license.

Cl **176** *SC* **176.8.1.1** *P* **231** *L* **14** # 480

Slavick, Jeff Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

test pattern check is overalpping with IS_SIGNAL.request

SuggestedRemedy

Move "test pattern check" to no overlap withPMA.IS_SIGNAL.request in Figure 176-21

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176** *SC* **176.9.1.2** *P* **242** *L* **12** # 540

Rechtman, Zvi Nvidia

Comment Type **TR** *Comment Status* **A** *Precoding*

The text currently refers to xAUI-n C2C. However, the adopted PMA baseline proposal stated that the ôPrecoding capability in all physically instantiated interfaces is æTx:required, Rx:optionalÆö (per ran_3dj_01a_2303 slide 10). This specification should also encompass xAUI-n C2M.

SuggestedRemedy

Add xAUI-n C2M

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #21

Cl **176** *SC* **176.9.1.2** *P* **242** *L* **23** # 541

Rechtman, Zvi Nvidia

Comment Type **T** *Comment Status* **A** *Precoding*

The paragraph refers only to the case of PMD control function operation, need to refer to Annex 176A for all electrical interfaces

SuggestedRemedy

Replace:
"If the PMA is connected to the service interface of an xBASE-CRn or xBASE-KRn PMD and training is enabled by the management variable mr_training_enable (see 136.7), then recoder_tx_out_enable_i and precoder_rx_in_enable_i shall be set as determined by the PMD control function in the LINK_READY state on lane i (see 136.8.11.7.5 and Figure 136û7). The method by which the MD control function affects these variables is implementation dependent."

With:
"If the PMA support the Control function and start-up protocol for electrical interfaces and training is enabled by the management variable mr_training_enable (see Annex 176A), then precoder_tx_out_enable_i and
precoder_rx_in_enable_i shall be set as determined by the control function in the LINK_READY state on lane i (see 176A.10.4 and Figure 176Aû6). The method by which the PMA control function affects these
variables is implementation dependent"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #21

Cl **176** *SC* **176.11** *P* **243** *L* **31** # 181

Brown, Matt — Alphawave Semi

Comment Type **T** *Comment Status* **R** *Skew (common)*

A similar subclause has traditionally been included in the PMA subclauses, defining the skew at each instantiated interface from the PMD to the PCS. Until now, there was only one type of PMA for each Ethernet rate. Now we have two types defined in two separate clauses for 200G, 400G, and 800G. A rate-neutral and type-neutral specification is required. This seems beyond a subclause in Clause 176.

SuggestedRemedy

Create a new annex (or perhaps a subclause in 176B) used to defined the skew and skew relationships through the PHY sublayer stack. A presented supporting this will be provided.

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **176** *SC* **176C** *P* **594** *L* **1** # 298

Loewenthal, Arnon — alphawave semi

Comment Type **T** *Comment Status* **A** *Test Vectors*

Annex 176C "SM-PMA test vectors" is currently empty.

SuggestedRemedy

Add test vectors for 200GBASE-R 8:1, 400GBASE-R 16:2, 800GBASE-R 32:4, and 1.6TBASE-R 16:8 to Annex 176C based on supporting contribution on May interim.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The CRG reviewed the presentation:
https://www.ieee802.org/3/dj/public/24_06/loewenthal_3dj_01a_2406.pdf

The associated vector files located at:
https://www.ieee802.org/3/dj/public/24_06/loewenthal_3dj_02_2406.zip

Add test vectors to Annex 176C with editorial license.

Cl **176A** *SC* **176A** *P* **548** *L* **6** # 196

Ran, Adee — Cisco

Comment Type **T** *Comment Status* **A**

The annex title includes "Control function and start-up protocol", while in the subclauses and text there are alternative terms such as "interface control function", "Start-up protocol", and "training" (176A.9).

This mega-function requires nomenclature to describe it. It would be good to have an acronym-friendly name so that it can be included in tables of other clauses (e.g. Table 116-3, Table 179-1).

SuggestedRemedy

A presentation with proposed nomenclature is planned.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The following presentation was reviewed by the 802.3dj task force at the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/law_3dj_01_2405.pdf

May Interim Straw poll # has the following results:
Straw Poll #4
The nomenclature that I prefer for function defined in Annex 176A is:
A. "Inter-sublayer link training" (ILT or ISLT)
B. "Sublink training" (SLT)
Results (all): A: 81, B: 5

See:
https://www.ieee802.org/3/dj/public/24_05/motions_3dj_2405.pdf

Update the draft such that references to the link training function (AKA control function) use the following name and acronym instead:
"inter-sublayer link training"
"ILT".
Implement with editorial license.

[Editor's note: The comment type was change from ER to T as it was deemed somewhat technical.]

Cl **176A** *SC* **176A** *P* **555** *L* **29** # 446

Simms, William NVIDIA

Comment Type **E** *Comment Status* **A** *(editorial)*

3 states of Coefficient select echo are undefined

SuggestedRemedy

note in table 176A-3 that 010, 011, 100 are undefined/invalid

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176A** *SC* **176A.1** *P* **548** *L* **12** # 577

Law, David HPE

Comment Type **TR** *Comment Status* **A** *ILT General*

The use of the terms 'segment' and 'link' in Annexe 176A, for example in 176A.1 where it says, 'in single-segment or multiple-segment links', are problematic.
á
IEEE Std 802.3 subclause 1.4.505 'segment' defines it as 'The medium connection, including connectors, between Medium Dependent Interfaces (MDIs) in a CSMA/CD local area network.'. Subclause 1.4.372 'link' defines it as 'The transmission path between any two interfaces of generic cabling. (From ISO/IEC 11801.)'.
á
As a result, I believe it would only be correct to call an electrical channel between two PMD sublayers a 'segment'. I do not believe that the electricaláchannel between any other combinations of sublayers is a 'segment'.

SuggestedRemedy

I would suggest 'section' as an alternate to 'segment', but that was used for 'The portion of the link between the PSE Power Interface (PI) and the PD PI.' (see 1.4.378) when PoE had a similar definition problem. Alternatives, therefore, might be 'Division' and 'Sector'.

As another approach, the following is a rewording of 176A.1 to avoid the use of the terms 'segment' and 'link' without the use of a new term. I acknowledge, however, that such an approach would require a significant rewrite of the Annexxe.

The start-up protocol facilitates timing recovery and equalization of the electrical channel between adjacent sublayers, or chains of multiple adjacent sublayers while providing a mechanism through which the receiver can configure the transmitter to optimize performance. The protocol supports these functions through the continuous exchange of fixed-length training frames across the electrical channel between adjacent sublayers and the transport of end-to-end indications across chains of multiple adjacent sublayers.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The following contribution was reviewed by the 802.3dj Task Force during the May 2024 Interim meeting https://www.ieee802.org/3/dj/public/24_05/law_3dj_01_2405.pdf

Implement the following with editorial license.

In Annex 176A (and other clauses where appropriate), replace "segment" with "section" and "link" with "path".

Cl **176A** *SC* **176A.2** *P* **548** *L* **24** # 198

Ran, Adee Cisco

Comment Type **ER** *Comment Status* **A** *(editorial)*

"tx_symbol and rx_symbol variables" do not appear in this annex. They are in fact parameters of the service interface primitives of the sublayer that implements the control function.

SuggestedRemedy

Tie the text defining the symbols to the service interface of the sublayer.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement with editorial license and discretion.

Cl **176A** *SC* **176A.2.1** *P* **547** *L* **3** # 563

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT PICS (Bucket)*

The first 'shall' statement in Annex 176A (normative) 'Control function and start-up protocol for electrical interfaces' is in 176A.2.3.1 'PRBS13 function'. It seems, however, that there should be 'shall' statements in relation to the entire Training frame structure.

SuggestedRemedy

[1] In subclause 176A.2.1, change 'The training frame marker is a run ...' to read 'The training frame marker shall be a run ...'.
[2] In subclause 176A.2.2, change 'The control field comprises ...' to read ' The control field shall be comprised of ...'.
[3] In subclause 176A.2.2, change 'The status field comprises ...' to read ' The status field shall be comprised of ...'.
[4] In subclause 176A.2.3, change 'The training pattern is the result of a ...' to read 'The training pattern shall be the result of a ...'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggeted remedy with editorial license.

Cl **176A** *SC* **176A.2.2** *P* **549** *L* **9** # 561

Law, David HPE

Comment Type **T** *Comment Status* **R** *ILT Frame (bucket)*

Subclause 176A.2.2 'Control and status fields' says that 'The control field comprises 16 bits with the structure defined in 176A.3.', yet figure 176Aû1 'Training frame structure' above shows the control field comprising of 16 cells. It, therefore, appears that the field is comprised of 16 cells that convey 16 bits.

SuggestedRemedy

[1] Change the first paragraph of 176A.2.2 to read 'The control field is comprised of 16 cells which convey 16 bits with the structure defined in 176A.3. The status is comprised of 16 cells which convey 16 bits with the structure defined in 176A.4.

[2] Change the last sentence of the penultimate paragraph of 176A.2.2 to read 'Within each field, the order of transmission is from bit 15 to bit 0, conveyed by cell 15 to cell 0 respectively.'.

Response *Response Status* **C**

REJECT.

The cell concept is described in detail in the following paragraph (second paragraph of 176A.2.2). Note that the text is identical to the text in 136.8.11.1.2.

Text is correct as written, proposed remedy does not improve the clarity of the draft.

Cl **176A** *SC* **176A.2.2** *P* **549** *L* **25** # 562

Law, David HPE

Comment Type **T** *Comment Status* **R** *ILT Frame (common)*

Subclause 176A.2.2 says '... if a violation of the DME encoding rules is detected within the control field or the status field, the contents of both fields in that frame are ignored.'. If this is requirement, suggest it should be stated using a 'shall' statement.

SuggestedRemedy

Change '... the contents of both fields in that frame are ignored.' to read '... the contents of both fields in that frame shall be ignored.'.

Response *Response Status* **C**

REJECT.

Note that this text is identical to the text in 136.8.11.1.2.

Text is correct as written, proposed remedy does not improve the clarity of the draft.

Cl **176A** *SC* **176A.2.3.2** *P* **552** *L* **14** # 199

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *ILT Pattern (Bucket)*

"The default identifier for each lane is its lane number (e.g., the default value for identifier_0 is 0 which selects polynomial_0)"

Some interfaces have 8 lanes.

The default mapping provided in Table 176Aû1 can be used instead.

SuggestedRemedy

Change to "The default identifier for each lane is the same as that of the PRBS13 function, as shown in Table 176A-1".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Change: "The default identifier for each lane is its lane number"
To: "The default identifier for each lane is the same as that shown in Table 176A-1"

Cl **176A** *SC* **176A.2.3.2** *P* **552** *L* **26** # 494

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *ILT Pattern (Bucket)*

The PRBS gen should "stop" if trainng stops.

SuggestedRemedy

Add "while training is in progress while this mode is selected" after "is not stopped or reset".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Add "while training is in progress and this mode is selected" after "is not stopped or reset".

Cl **176A** *SC* **176A.2.3.2** *P* **552** *L* **31** # 497

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *ILT Pattern (common)*

There is only 1 mode of operation for PRBS13 free-running, PAM4. We do have 1 free mode.

SuggestedRemedy

Add PRBS13-free running with precode as an option for a training pattern.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #358

Cl **176A** *SC* **176A.2.3.3** *P* **552** *L* **34** # 548

Rechtman, Zvi Nvidia

Comment Type **TR** *Comment Status* **A** *ILT Pattern (common)*

In the case of multi-lane operation, if all lanes exits the QUIET state simultaneously and use the same PRBS31 initial seed, there will be an undesired crosstalk effect. This potential issue needs to be addressed

SuggestedRemedy

Explicitly define that each lane must use different initial seed.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #358

Cl **176A** *SC* **176A.2.3.3** *P* **552** *L* **40** # 200

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *ILT Pattern (common)*

"These three variations are produced as described for the PRBS13 free-running function in 176A.2.3.2"

PRBS13 free-running is defined only with PAM4 and does not have PAM2 or PAM4+precoding variants. These variants are defined for the PRBS13 function in 176A.2.3.1, but the definition of the precoding variant includes resetting of the precoder state at the beginning of each training frame, which would be inadequate.

SuggestedRemedy

Change to the following:

The initial state of the PRBS31 generator shall not be all zeros. It may be any other value.

When the training pattern selector is set to PAM4, the training pattern is generated in a similar manner to the definition in 176A.2.3.2, except that PRBS31 generator output is used instead of PRBS13 generator output.

When the training pattern selector is set to PAM2, the training pattern is generated in a similar manner to the definition in 176A.2.3.2, except that PRBS31 generator output is used instead of PRBS13 generator output, and the pair of bits {A, A} is used instead of {A, B}.

When the training pattern selector is set to PAM4 with precoding, the training pattern is generated from the PRBS31 PAM4 pattern by precoding the Gray-mapped PAM4 symbols as specified in 135.5.7.2. The precoder initial state is not specified. The state is not re-initialized or reset during generation of the training pattern.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #358

Cl **176A** *SC* **176A.2.3.3** *P* **552** *L* **41** # 496

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *ILT Pattern (common)*

PRBS13 free-running can only provide PAM4 it does not have a select for PAM2 or PAM4 with precode while PRBS31 does have those options. So how can we refer to PRBS13 free running for how to map the PRBS data to training pattern.

SuggestedRemedy

Split the 2nd paragraph of 176A.2.3.3 into 3 paragraphs tha defines how the pattern for each of the the possible encoding options as is done in 176A.2.3.1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #358

Cl **176A** *SC* **176A.2.3.3** *P* **552** *L* **43** # 495

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *ILT Pattern (Bucket)*

The PRBS gen should "stop" if trainng stops.

SuggestedRemedy

Add "while training is in progress while this mode is selected" after "is not stopped or reset".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Add "while training is in progress and this mode is selected" after "is not stopped or reset".

Cl **176A** *SC* **176A.2.3.3** *P* **552** *L* **46** # 498

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **R** *ILT Pattern (common)*

There is no zero pad for PRBS31 free-running. This means we could have a run length of 31 3's in a row when the maximal run length of the PRBS pattern runs into Frame Marker. The Zero pad is really part of the Framer Marker ensuring there is a distinct edge ahead of 16 UI run 3's for the start of the frame marker.

SuggestedRemedy

Bring the zero-pad back into the definition of the training frame. Stating that it is immediately precedes the training frame marker to provide a disticnt transition from training pattern to frame marker of the next training frame.

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #358.

Cl **176A** *SC* **176A.3** *P* **553** *L* **20** # 358

Healey, Adam Broadcom Inc.

Comment Type **T** *Comment Status* **A** *ILT Frame (common)*

Training pattern options have been added to give receiver additional flexibility to successfully complete training. However, that flexibility is limited by a menu of fixed combinations of encoding and test pattern options. It would be better if encoding and test pattern selections were separated to allow receivers to request whatever combination best suits their needs. There is space in the control and status field structures to accommodate this.

SuggestedRemedy

In Table 176A-2, restore bits in control field bits 8 and 9 to the original "Modulation and precoding request" encoding defined in Clause 162. Define bits 5 and 6 to be "Test pattern request" with 00=PRBS13, 01=Free-running PRBS13, 10=Reserved, and 11=Free-running PRBS31. Restore bits 10 and 11 in the status field (Table 176A-3) to the "Modulation and precoding status" encoding defined in Clause 162. Define bits 12 and 13 to be "Test pattern status" using the same encodings as the control field. Update Figure 176A-2, 176A.3.2, and 176A.10.3.1 accordingly. Also add subclauses corresponding the Modulation and precoding request/status fields.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The CRG reviewed the editorial team's notes on slides 15-32 of https://www.ieee802.org/3/dj/public/24_06/brown_3dj_02b_2406.pdf.

The following straw poll was taken:
Straw poll TF-1 (direction)
I support the following direction for resolution of the training-pattern related comments in brown_3dj_02b_2406
A. Option 1, as shown on slides 19-29
B. Option 2, as shown on slides 30-32
C. Need more information
D. Abstain
A: 13 B: 5 C: 4 D: 16

In discussion there was no consensus for adding the pad symbols as shown on slide 26.

Implement option 1 as shown on slides 20-27, with the exception that pad symbols are not added when the free-running PRBS13 or PRBS31 pattern generators are used.
Implement with editorial license.

Cl **176A** *SC* **176A.3.1** *P* **553** *L* **45** # 499

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *ILT Coefficients (Bucket)*

Remove the specifity of how many presets there are.

SuggestedRemedy

Change:
ôThe initial condition request bits are used to select one of the five predefined transmitter equalizer configurations (presets) specified in the AUI or PMD clauses. ô
To:
ôThe initial condition request bits are used to select a predefined transmitter equalizer configurations (presets) specified in the AUI or PMD clauses. ô

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Change: "The initial condition request bits are used to select one of the five predefined transmitter equalizer configurations (presets) specified in the AUI or PMD clauses." to:
"The initial condition request bits are used to select one of the up to five predefined transmitter equalizer configurations (presets) specified in the AUI or PMD clauses."

Cl **176A** *SC* **176A.4** *P* **555** *L* **10** # 549

Rechtman, Zvi Nvidia

Comment Type **T** *Comment Status* **A** *ILT Frame (Bucket)*

The comment refers to Table 176Aû3ùStatus field structure.
The field in bit 14 - "One" require some explanation. ItÆs unclear whether it refers to the support of the newly adopted test patterns, the support of multi-segment operation, or both.

SuggestedRemedy

Define the purpose of this bit

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement the following with editorial license.
Add new section after the Receiver Ready section:
"176A.4.2 One
The one bit is set to 1 to signal the local receiver that the link partner supports the multi-segment control function."

Note that comment #196 proposes to change "multi-segment control function" to "inter-sublayer link training". If necessary, adjust the text to reflect the new terminology.

Cl **176A** *SC* **176A.4** *P* **555** *L* **17** # 61

Dudek, Mike Marvell

Comment Type **T** *Comment Status* **A** *ILT Frame (common)*

It would be better to have the existing patterns the same as for previous clause 136.

SuggestedRemedy

In Table 176A-3 use the 1 in bit 12 for the new patterns keeping the bits 11 and 10 the same as they were in clause 136 i.e. change 010 to PAM4 PRBS13, 100 to PAM4 free running PRBS13, 011 to PAM4 PRB13 with precoding and 110 to PAM4 free-running PRBS31

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #358.

Cl **176A** *SC* **176A.4** *P* **555** *L* **27** # 501

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *ILT Frame (Bucket)*

You have self generated data you're sending but you don't have your self setup to send mission data yet.

SuggestedRemedy

Remove the "No data is available," from the option 1 of Extend training bit

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.

Cl **176A** *SC* **176A.4.3** *P* **556** *L* **4** # 574

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Frame (Bucket)*

176A.4.3 'Receiver frame lock' says that 'When the receiver frame lock bit is set to 1, the receiver is indicating that it has identified training frame marker positions and is in a state where the response time requirements specified in 176A.10 are met.'. It then goes on to say 'Receiver frame lock ... is not set to 1 until training and local_tf_lock are both true.'.
á
176A.10 is 'Variables, functions, timers, counters, and state diagrams', so I wonder if the reference should be to 176A.8 'Handshake timing'? In addition, I don't believe the variables training and local_tf_lock are conditioned on the response time requirements specified in 176A.10 being met, at least I didn't see it in their descriptions.

SuggestedRemedy

In 176A.4.3 change the text '... response time requirements specified in 176A.10 are met.' to read '... response time requirements specified in 176A.8 are met.' and the text '... and is not set to 1 until training and local_tf_lock are both true.' To read '... and is not set to 1 until training and local_tf_lock are both true and the response time requirements specified in 176A.10 can be met.'

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Change: "... response time requirements specified in 176A.10 are met."
To: "... response time requirements specified in 176A.8 are met."
Change: "... and is not set to 1 until training and local_tf_lock are both true."
To: "... and is not set to 1 until training and local_tf_lock are both true and the response time requirements specified in 176A.8 can be met."

Cl **176A** *SC* **176A.4.8** *P* **556** *L* **37** # 564

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Frame (Bucket)*

176A.4.8 'Coefficient status' says that 'The acknowledge reflects the value of coef_sts resulting from the procedure described in 176A.6.3.'. I don't see a procedure that sets coef_sts in 176A.6.3, but there is one in 176A.6.4. With that said, is it correct that it is just this procedure that sets coef_sts? On review of Figure 176Aû9 'Coefficient update state diagram', I see it directly sets coef_sts to 'not_upd' in the OUT_OF_SYNC state and indirectly sets coef_sts using the procedure described in 176A.6.4 through calls to the UPDATE_C(k) function in the NEW_REQUEST state. This seems to be confirmed by the first paragraph of 176A.6.4 which says 'The handling of incoming requests is specified by the coefficient update state diagram (Figure 176Aû9). The behavior of the UPDATE_C(k) function shall be consistent with the following algorithm.'.

SuggestedRemedy

Change 'The acknowledge reflects the value of coef_sts resulting from the procedure described in 176A.6.3.' to read 'The coefficient status bits reflect the value of coef_sts variable generated by the coefficient update state diagram (Figure 176Aû9).'.

Response *Response Status* **C**

ACCEPT.

Cl **176A** *SC* **176A.4.8** *P* **556** *L* **37** # 576

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Frame (Bucket)*

176A.4.8 'Coefficient status' says 'The acknowledge reflects the value of coef_sts resulting from the procedure described in 176A.6.3.'. While it is correct that the coef_sts variable is updated by the UPDATE_C(k) function in 176A.6.3, I believe the OUT_OF_SYNC, NEW_INDEX, and WAIT states of the Coefficient update state diagram also update the coef_sts variable. Further, 176A.10.3.2 says that the ENCODE_STS function 'Encodes portions of the status field of transmitted training frames.' and that '... coef_sts is mapped to the coefficient status bits ...'.

SuggestedRemedy

Since calls of the UPDATE_C(k) function and direct updates of the coef_sts variable all occur in the Coefficient update state diagram, suggest that 'The acknowledge reflects the value of coef_sts resulting from the procedure described in 176A.6.3.' in 176A.4.8 should be changed to just read 'The acknowledge reflects the value of coef_sts generated by the Coefficient update state diagram '.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
This comment appears to address the same concern expressed in comment #564.
Resolve using the response to comment #564.

Cl **176A** *SC* **176A.4.1+** *P* **555** *L* **46** # 447

Simms, William NVIDIA

Comment Type **E** *Comment Status* **A** *(editorial)*

Should the status field name be uniquified? The field name in the text of the table and text sections below the table do not clearly identify text as a field.

SuggestedRemedy

Change Receiver ready to RECEIVER_READY or at maybe receiver_ready and use the same in the text below the table 176A-3- Status field structure. Pertains to all field names.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176A** *SC* **176A.6** *P* **557** *L* **3** # 201

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *ILT Coefficients (Bucket)*

"When the interface control state diagram (Figure 176Aû6) is in the TRAIN_LOCAL state, the device may request its link partner to..."

It is important to also note at which states requests from the link partner should be processed, and what happens in the other states - this may not be obvious.

SuggestedRemedy

Insert the following paragraphs after the first one:

When the interface control state diagram is in either the TRAIN_LOCAL or TRAIN_REMOTE state, the device shall respond to requests received from the link partner.

When the interface control state diagram is in any state other than TRAIN_LOCAL or TRAIN_REMOTE, the device shall not send any requests to the link partner and shall ignore requests from the link partner.

Response *Response Status* **C**

ACCEPT.

Cl **176A** *SC* **176A.6.2** *P* **557** *L* **53** # 500

Slavick, Jeff Broadcom

Comment Type **T** *Comment Status* **A** *ILT Coefficients (common)*

To support AUI or PMDs only providing a subset of the availabile PRESETs we should define a behavior in that scenario

SuggestedRemedy

Add a statement that if the AUI or PMD does not specify coefficient values for a given preset setting then no change is made to the existings settings and ic_sts response of updated is provided.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
It was clarified a that the comment addresses the case where a specification of a PMD or AUI does not include a specific preset.
Implement the suggested remedy with editorial license.

Cl **176A** *SC* **176A.6.4** *P* **558** *L* **17** # 457

Opsasnick, Eugene Broadcom

Comment Type **T** *Comment Status* **A** *ILT Coefficients (common)*

This the entire block of pseudo-code in this subclause is exactly the same as the code in subclause 136.8.11.4.4, and the entire subcluse only differs by adding one coefficient (-3) to the k_list. I suggest replacing the text of the entire subclause with a refernece to subclause 136.8.11.4.4.

SuggestedRemedy

New text for this subclause:
"The handling of incoming requests is specified by the coefficient update state diagram (Figure 136-9).

The behavior of the UPDATE_C(k) function shall be consistent with the algorithm specified in 136.8.11.4.4 with one execption:
- The set of of valid equalizer coefficient indices, k_list, is expanded by one from {-2, -1, 0, 1} to {-3, -2, -1, 0 ,1}.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Annex 176A is intended to be the specification for link training for 200 Gb/s per lane PMDs/AUIs and potentially higher signaling rate PMDs/AUIs.

Since it is substantially different from the earlier PMD control function, this annex is written as a complete specification. Although referencing an older subclause in some subclauses is an option, it would be beneficial for readers of the standard to have a complete specification in this annex.

Add informative notes where content is identical to content in a particular subclause in Clause 136 with editorial license.

Cl **176A** *SC* **176A.6.4** *P* **558** *L* **21** # 565

Law, David HPE

Comment Type **E** *Comment Status* **A** *(editorial)*

176A.6.4 says that 'The variables coef_req, coef_sts, and k are defined in 176A.10.3.1.', however, 176A.10.3.1 'Variables' uses all lowercase for the coef_sts values (e.g., updated, coefficient at limit and equalization limit) and coef_req (e.g, decrement, increment) whereas 176A.10.3.1 uses all uppercase for the coef_sts values (e.g., UPDATED, COEFFICIENT AT LIMIT AND EQUALIZATION LIMIT) and coef_req (e.g., DECREMENT, INCREMENT).

SuggestedRemedy

The formatting of the variable values defined in 176A.10.3.1 'Variables' and used in 176A.6.4 should match.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176A** *SC* **176A.6.4** *P* **558** *L* **46** # 568

Law, David HPE

Comment Type **E** *Comment Status* **A** *(editorial)*

Change 'coef_sts = COEFFICENT AT LIMIT' (COEFFICIENT misspelt) to read 'COEFFICIENT AT LIMIT'

SuggestedRemedy

See comment.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176A** *SC* **176A.6.4** *P* **558** *L* **54** # 448

Simms, William NVIDIA

Comment Type **E** *Comment Status* **A** *(editorial)*

It took me longer than usual to realize the algorithm continues on page 559

SuggestedRemedy

Maybe put a '---continued---' at the last line of page 558. Disregard if this is inconsistent with IEEE style

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176A** *SC* **176A.8** *P* **559** *L* **45** # 202

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *ILT Coefficients (Bucket)*

"When the receiver frame lock bit in the status field of transmitted training frames is set to 1, the time from the receipt of a new request to the acknowledgment of that request shall be less than 2 ms"

This requirement was defined in 802.3cd when training was limited in time (to 3 seconds) in order to prevent limiting the number of change requests due to delayed responses.

The new training scheme is not limited in time, and a receiver can use as many requests as it needs.

In some multi-tasking implementations, a hard 2 ms maximum may be challenging to meet. To avoid real-time requirements, it would be sufficient to have 2 ms as the average response time (and it does not need to be normative). The maximum response time can be relaxed without impact to the protocol.

SuggestedRemedy

Change to
"When the receiver frame lock bit in the status field of transmitted training frames is set to 1, the time from the receipt of a new request to the acknowledgment of that request shall be less than 20 ms. It is recommended that the average response time is less than 2 ms".

Response *Response Status* **C**

ACCEPT.

Cl **176A** *SC* **176A.9** *P* **560** *L* **19** # 197

Ran, Adee Cisco

Comment Type **ER** *Comment Status* **A** *(editorial)*

The "Segment by segment training" seems to be an introductory subclause that explains the purpose of the whole thing.

It would help readers if this introduction is placed at the beginning of the annex. The current introduction in 176A.1 seems too brief.

SuggestedRemedy

Move 176A.9 and its subclauses into 176A.1 (with some hierarchy) or after it.

Rephrase the text as necessary to make it a good introduction to the control function (e.g., explain what "RTS" stands for).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176A** *SC* **176A.9.2** *P* **562** *L* **14** # 555

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT (Bucket)*

Figure 176Aû5 'Retimer reference model' shows the data multiplexor driven by the tx_mode value, with the multiplexor select set to 0 when tx_mode = training and set to 1 when tx_mode = data. Subclause 176A.10.2.1 'Variables', however, defines three values for tx_mode, training, local_pattern and data. Figure 176Aû5, therefore, does not define the multiplexor select value for when tx_mode = local_pattern.

SuggestedRemedy

Update the figure to reflect the third value of tx_mode and the local pattern generator for each interface.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Add the local_pattern option to the data selector.
Add a Local pattern box as an input to the data selector.

Cl **176A** *SC* **176A.9.2** *P* **562** *L* **22** # 554

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT (Bucket)*

The arrow pointing to the Interface A 'Driver' block and arrow point-ing from the Interface B 'CDR' block both seem to be pointing in the wrong direction.

SuggestedRemedy

Reverse the direction of both arrows.

Response *Response Status* **C**

ACCEPT.

Cl **176A** *SC* **176A.10.1** *P* **562** *L* **53** # 553

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Diagrams (Bucket)*

Subclause 176A.10.1 'State diagram conventions' says that 'The notation used in the state diagrams follows the conventions of 21.5.', however subclause 21.5 does not address the operation of timers.

SuggestedRemedy

Suggest that the text 'All timers operate in the manner described in 14.2.3.2.' be inserted as the new second sentence of the second paragraph of subclause 176A.10.1.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Insert the text fom clause 136.8.11.7.5: "State diagram timers follow the conventions of 14.2.3.2." as the new second sentence of the second paragraph of subclause 176A.10.1.

Cl **176A** *SC* **176A.10.2.1** *P* **563** *L* **44** # 567

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Diagrams (Bucket)*

Suggest a description of what happens when the tx_disable variableáis set to false is added to the variable description.

SuggestedRemedy

[1] Add 'When it is false, tx_mode controls the content of the transmitter's output on the interface.' or 'When it is false, tx_mode controls the content of the transmitter's output on all lanes of the interface.', depending on the response to my other comment, to the end of the tx_disable variable description.

[2] Change the text '... of the interface.' in the first sentence of the tx_mode variable description to read '... of the interface when tx_disable is false.'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement the following with editorial license.

Add the following sentence at the end of the tx_disable definition:
"When it is false, tx_mode controls the content of the transmitter's output on the lane."

Move the definition of tx_mode to 176A.10.3.1 and change the definition of tx_mode.
from: "Enumerated variable that controls the content of the transmitter's output of the interface."
to: "Enumerated variable that controls the content of the transmitter's output of the lane when tx_disable is false."

Cl **176A** *SC* **176A.10.2.1** *P* **563** *L* **44** # 566

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Diagrams (Bucket)*

The last sentence of the tx_disable variable description says that the '... output on the lane is disabled.'. Is this correct, the first sentence says that tx_disable '... controls the transmitter's output on the interface.' and tx_disable is defined under subclause 176A.10.2 'Per-interface variables, functions and timers'. Suggest that the reference to 'lane' is changed to 'interface', or use 'all lanes of the interface' in the variable description to reflect the segment_ready variable description immediately above.

SuggestedRemedy

á
Either
á
[a] Change the text '... output on the lane is disabled.' in the last sentence of the tx_disable variable description to read '... output on the interface is disabled.'.
á
or
á
[b] Change [1] the text '... the transmitter's output on the interface.' in the first sentence of both the tx_disable and tx_mode variable descriptions to read '... the transmitter output on all lanes of the interface.'; and [2] the text '... output on the lane is disabled.' in the last sentence of the tx_disable variable description to read '... output on all lanes of the interface is disabled.'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

tx_disable is a per lane variable.

Implement the following with editorial license.
Move the definition of tx_disable to 176A.10.3.
Change the first sentence of the definition.
from: "Boolean variable that controls the transmitter's output on the interface."
to: "Boolean variable that controls the transmitter's output on the lane."

Cl **176A** *SC* **176A.10.3** *P* **564** *L* **16** # 571

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Diagrams (bucket)*

176A.10.3 'Per-lane variables, functions, timers and counters' says 'The device implements one instance of each of the interface control state diagrams, and the set of associated ... for each of the n physical lanes on each of its interfaces (see 176A.9)'. I don't think this is correct as I believe that the interface control state diagram is one for each interface of a device (see 176A.10.2), and it is the frame lock and coefficient update state diagrams that are one for each lane of each interface of a device.

SuggestedRemedy

Change "The device implements one instance of each of the interface control state diagrams ...' to read 'The device implements one instance of each of the frame lock and coefficient update state diagrams ...'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The Interface control state diagram in Figure 176A-6 is implemented per lane, only the RTS update state diagram in Figure 176A-7 is implemented per interface.

It would be helpful to separate the state diagrams into the per-interface and per-lane subclauses.

Implement the following with editorial license.
Change the first sentence of 176A.10.2.
from: "A device implements one instance of each of the interface control state diagrams"
to: "A device implements one instance of the RTS update state diagram".

Break subclause 176A.10.4 (State diagrams) into two subclauses, one in 176A.10.2 (Per-interface variables, functions and timers) and one in 176A.10.3 (Per-lane variables, functions, timers and counters).

Change the title of Figure 176A-6 from "Interface control state diagram" to Figure 176A-6 from "Training control state diagram".

Cl **176A** *SC* **176A.10.3.1** *P* **565** *L* **5** # 572

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Diagrams (bucket)*

The variables local_tf_lock, remote_tf_lock, local_rx_ready and remote_rx_ready are all defined in 176A.10.3 'Per-lane variables, functions, timers and counters' and are related to a lane, yet they are used by figure 176A-6 'Interface control state diagram'. 176A.10.2 'Per-interface variables, functions and timers' says 'A device implements one instance of each of the interface control state diagrams independently for each of its interfaces (see 176A.9).'.

SuggestedRemedy

Perhaps figure 176A-6 'Interface control state diagram' should use a 'interface' version of each of these variables that are a logical AND of the respective lane variable in the case of a multi-lane interface.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the responses to comments #566, #567 and #571.

Cl **176A** *SC* **176A.10.3.1** *P* **565** *L* **7** # 573

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Diagrams (Bucket)*

The description of the local_tf_lock variable in 176A.10.3.1 says that 'The value of this variable is encoded as the "training lock" bit in the status field of transmitted training frames.', however, there isn't a "training lock" bit defined for the training frames. Since 176A.4.3 'Receiver frame lock' says 'Receiver frame lock ... is not set to 1 until training and local_tf_lock are both true.' it seems that local_tf_lock is encoded in the 'Receiver frame lock' bit.

SuggestedRemedy

Change the text '... is encoded as the "training lock" bit ...' in the local_tf_lock variable description to read '.... is encoded in the "Receiver frame lock" bit ...'.

Response *Response Status* **C**

ACCEPT.

Cl **176A** *SC* **176A.10.3.3** *P* **566** *L* **21** # 569

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Diagrams (common)*

176A.10.3.3 'Timers' is a subclause of 176A.10.3 'Per-lane variables, functions, timers and counters', yet the three times listed, quiet_timer, propagation_timer and recovery_timer are all used by the interface control state diagram. 176A.10.2 'Per-interface variables, functions and timers' says 'A device implements one instance of each of the interface control state diagrams, and the set of associated variables, functions, counters and timers defined in this subclause, independently for each of its interfaces(see 176A.9).' As a result, it seems these timers should be moved to 176A.10.2.3 'Timers' and the descriptions should be updated to reflect that they operate on a per-interface basis.

SuggestedRemedy

[1] Move the quiet_timer, propagation_timer and recovery_timer definitions to 176A.10.2.3 'Timers' and delete 176A.10.3.3 'Timers'.
[2] Change the text '... the interface control state diagram on a lane enters the ...' in the description of quiet_timer, propagation_timer and recovery_timer to read '... the interface control state diagram on an interface enters the ...'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #571.

Cl **176A** *SC* **176A.10.4** *P* **566** *L* **46** # 458

Opsasnick, Eugene Broadcom

Comment Type **T** *Comment Status* **A** *ILT Diagrams (common)*

The state diagram shown in Figure176A-8 "Training frame lock state diagram" on page 570 and Figure 176A-9 "Coefficient update state diagram" are exactly the same as the state diagrams of the same names in Figure 136-8 and Figure 136-9. Only the reset signal is renamed from "mr_restart_training" to "mr_restart".

SuggestedRemedy

Remove Figure 176A-8 and Figure 176A-9.

Change "mr_restart" to "mr_restart_trainging" in subclause 176A.10.2.1 on page 564, line 21.

Change the text at the bottom of page 566 to refer to the equivilent state diagrams in clause 136 instead of the removed figures (with editorial license).

Any variables defined in subclause 176A.10.3.1 which are only used in the removed state diagrams can also be removed.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #457

Cl **176A** *SC* **176A.10.4** *P* **566** *L* **52** # 570

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Diagrams (common)*

176A.10.2 'Per-interface variables, functions and timers' says 'A device implements one instance of each of the interface control state diagrams independently for each of its interfaces (see 176A.9).' and 176A.10.4 'State diagrams' says 'The interface control state diagram (Figure 176Aû6) defines the operation of the startup protocol for AUIs and PMDs'. 176A.10.4 'State diagrams', however, goes on to say, 'The interface control, frame lock and coefficient update state diagrams shall be implemented for each lane.'. This doesn't seem to be in alignment with the prior text and doesn't seem to be correct.

SuggestedRemedy

Change the last paragraph of 176A.10.4 to read 'The interface control and RTS update state diagrams shall be implemented for each interface of a device. The frame lock and coefficient update state diagrams shall be implemented for each lane of each interface of a device.'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #571.

Cl **176A** *SC* **176A.10.4** *P* **566** *L* **54** # 542

Rechtman, Zvi Nvidia

Comment Type **TR** *Comment Status* **A** *ILT Diagrams (Bucket)*

The operation of precoding after the completion of the start-up protocol is missing

SuggestedRemedy

Add the following text:
"If the LINK_READY state is entered with local_tp_mode set to ôPAM4 with precodingö, then the PMA shall transmit all subsequent data on the corresponding lane with precoding (see
176.9.1.2).
If the LINK_READY state is entered with remote_tp_mode set to ôPAM4 with precodingö, then the PMA shall subsequently received data on the corresponding lane includes precoding (see 176.9.1.2)"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement the following with editorial license.

After the first paragraph of 176A.10, add the following text:
If the LINK_READY state in the Interface control state diagram (see Figure 176A-6) is entered with local_tp_mode set to "PAM4 with precoding", then the PMD or AUI shall cause the adjacent PMA to transmit all subsequent data on the corresponding lane with precoding (see 176.9.1.2).
If the LINK_READY state is entered with remote_tp_mode set to "PAM4 with precoding", then the PMD or AUI shall inform the adjacent PMA that all subsequently received data on the corresponding lane includes precoding (see 176.9.1.2).

Cl **176A** *SC* **176A.10.4** *P* **568** *L* **20** # 551

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Diagrams (Bucket)*

There is a spurious '<' withing the transition condition from the state TRAIN_LOCAL to the state TRAIN_REMOTE.

SuggestedRemedy

Suggest that 'local_tf_lock<* local_rx_ready' should read 'local_tf_lock * local_rx_ready'.

Response *Response Status* **C**

ACCEPT.

Cl **176A** *SC* **176A.10.4** *P* **568** *L* **20** # 552

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Diagrams (Bucket)*

There should be an underscore between the timer name and 'done'.

SuggestedRemedy

Suggest that 'recovery_timer done' should be changed to read 'recovery_timer_done'.

Response *Response Status* **C**

ACCEPT.

Cl **176A** *SC* **176A.10.4** *P* **568** *L* **48** # 550

Rechtman, Zvi Nvidia

Comment Type **T** *Comment Status* **A** *ILT Diagrams (common)*

The comment refers to Figure 176Aû6ùInterface control state diagram.
The RECOVERY state coupled with the absence of timeouts, introduces a new challenge in identifying marginal performance cases. These cases may lead to repeated transitions between TRAIN_LOCAL/TRAIN_REMOTE/SEGMENT_READY state to/from RECOVERY state in scenarios of alternating local_tf_lock.
A possible solution is to limit the number of RECOVERY events by counting and limiting the number of transitions to the RECOVERY state.

SuggestedRemedy

Define a new counter: ôrecovery_event_countö. This counter increments each time the control state diagram transitions into the RECOVERY state.

Effects on the state diagram:
The ôrecovery_event_countö should be initialized to 0 in the ôSEND_TRAININGö state.
Upon entering the RECOVERY state, the ôrecovery_event_countö should be incremented by 1.

State diagram transition change:
The transition condition from the RECOVERY state to the FAIL state needs to be modified as follows:
Change ôrecovery_timer doneö to ôrecovery_timer done || recovery_event_count > Xö, where X is 5 (or to be determined).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The CRG reviewed slides 34 and 35 in the following presentation:
https://www.ieee802.org/3/dj/public/24_06/brown_3dj_02a_2406.pdf

The suggested change has merit, but the suggested threshold of 5 is somewhat arbitrary. Depending on implementatation, other thresholds may be preferred, or this condition may be disabled, without affecting interoperability.

Implement the following with editorial license.

Define a new variable in 176A.10.3.1 as follows:
"max_recovery_events. Integer variable that controls the maximum allowed number of transitions into the RECOVERY state in the Interface control state diagram (Figure 176A-6). A value of zero allows unlimited number of transitions. The value of this variable is implementation dependent."

Define a new counter in 176A.10.3.4 as follows:
"recovery_event_count. This counter increments each time the control state diagram (see Figure 176A-6) transitions into the RECOVERY state."

In Figure 176A-6.
Initialize "recovery_event_count" to 0 in the "SEND_TRAINING" state.
In the RECOVERY state increment the "recovery_event_count" by 1.
Modify the transition condition from the RECOVERY state to the FAIL state as follows.
Change "recovery_timer done"
to "recovery_timer done + (max_recovery_events != 0)*(recovery_event_count >= max_recovery_events)".

Cl **176A** *SC* **176A.10.4** *P* **569** *L* **17** # 556

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Diagrams (Bucket)*

The WAIT_ADJACENT to SWITCH_CLOCK transition condition uses the variable mr_training_enabled, however subclause 176A.10.2.1 'Variables' defines the variable mr_training_enable, not mr_training_enabled.

SuggestedRemedy

Change the transition condition ' (!mr_training_enabled + segment_ready) * ...' to read ' (!mr_training_enable + segment_ready) * ...'.

Response *Response Status* **C**

ACCEPT.

Cl **176A** *SC* **176A.10.4** *P* **570** *L* **9** # 557

Law, David HPE

Comment Type **E** *Comment Status* **A** *(editorial)*

Subclause 176A.10.1 'State diagram conventions' says that 'The notation used in the state diagrams follows the conventions of 21.5.'. Subclause 21.5.3 'State transitions' says 'The following terms are valid transition qualifiers:' and item d) says 'An unconditional transition: UCT'. As a result, it is not necessary to expand UCT on it's first use in Annex 176A.

SuggestedRemedy

Change the text 'UCT (unconditional transition)' to read 'UCT'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176A** SC **176A.10.4** P **571** L **9** # 575

Law, David HPE

Comment Type **T** *Comment Status* **A** *ILT Diagrams (common)*

The UPDATE_IC function is called in the OUT_OF_SYNC state of the Figure 176Aû9 Coefficient update state diagram. The UPDATE_IC function uses the ic_req variable to set the coefficients (see 176A.6.2), and the ic_req variable is derived from the 'initial condition request' bits from the control field of the received training frames (see 176A.10.3.1).

Since, however, the OUT_OF_SYNC state is entered during reset (reset or mr_restart set true), it would seem unlikely that training frames are being received. If that is the case, it isn't clear what the value of the ic_req variable is, and therefore what the coefficients should be set to.
á
176A.6.2 says that 'The transmitter equalizer is set to preset 1 upon entry to the QUIET state of the interface control state diagram.'. Since the QUIET state of the Interface control state diagram is also entered during reset, it seems the coefficients should be set to preset 1 when the Coefficient update state diagram is in the OUT_OF_SYNC state.

SuggestedRemedy

[1] Delete the first sentence of the ic_req definition in 176A.10.3.1.
[2] Add the text 'If the Coefficient update state diagram is in the OUT_OF_SYNC state ic_req is set to preset 1. Otherwise, it is derived from the "initial condition request" bit of the control field of received training frames on the correspondent lane of the interface.' to the end of the ic_req definition in 176A.10.3.1.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Slides 12 through 14 of the following presentation, prepared by the editorial team, was reviewed by the CRG.
https://www.ieee802.org/3/dj/public/24_06/brown_3dj_02a_2406.pdf

Implement the proposal on slides 13 and 14 of brown_3dj_02a_2406 with editorial license.

Cl **176A** SC **176A-6** P **568** L **21** # 449

Simms, William NVIDIA

Comment Type **ER** *Comment Status* **A** *(editorial)*

Figure 176A-6 has an extraneous < in the name 'local_tf_lock<*'

SuggestedRemedy

change to 'local_tf_lock*'

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176D** SC **176D.1** P **595** L **16** # 584

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **R** *Channel ILdd (bucket)*

C2C loss is TBD

SuggestedRemedy

Assuming 28 dB budget and package A length ~300 mm and ~125 mm for package B

Response *Response Status* **C**

REJECT.
The comment addresses an open TBD, but the suggested remedy is unclear.

Also, the suggested remedy assumes the budget is 28 dB, but consensus on that has not been shown.

Cl **176D** SC **176D.2** P **596** L **32** # 583

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *(bucket)*

Functional block diagram shown for C2C indicate ball-ball specifications

SuggestedRemedy

C2C component should be called C2C device and change the TP0 to TP0d and TP5 to TP5d

Response *Response Status* **C**

ACCEPT.

Cl **176D** SC **176D.3.3** P **597** L **22** # 422

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *B-T filter BW*

Transmitter measurement bandwidth is TBD

SuggestedRemedy

Replace TBD with 62 GHz

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #60.

Cl **176D** SC **176D.3.3** P **597** L **33** # 423

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *(bucket)*

Signaling rate of 106.255 ▒ 50 ppm in Table 176Dû1 is incorrect

SuggestedRemedy

Change "106.255 ▒ 50 ppm" to "106.25 ▒ 50 ppm"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #361.

Cl **176D** SC **176D.3.3** P **597** L **33** # 361

Healey, Adam Broadcom Inc.

Comment Type **T** *Comment Status* **A** *(bucket)*

Typo.

SuggestedRemedy

Change "106.255" to "106.25".

Response *Response Status* **C**

ACCEPT.

Cl **176D** SC **176D.3.3** P **597** L **33** # 398

Wu, Mau-Lin MediaTek

Comment Type **TR** *Comment Status* **A** *(bucket)*

The value of '106.255 +/- 50 ppm' is not correct.

SuggestedRemedy

Change '106.255' to '106.25'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #361.

Cl **176D** SC **176D.3.3** P **598** L **16** # 450

Simms, William NVIDIA

Comment Type **E** *Comment Status* **A** *(editorial)*

Where does the value for SNDR of 32.5dB come from?

SuggestedRemedy

No change suggested, looking for source material

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **176D** SC **176D.3.4.4** P **602** L **47** # 424

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *ERL (bucket)*

Reference to ERL methodology is missing

SuggestedRemedy

Add reference to 176D.4.3.

Response *Response Status* **C**

ACCEPT.

Cl **176D** SC **176D.3.4.4** P **603** L **18** # 425

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *B-T filter BW*

4th order Bessel-Thomson filter BW is TBD

SuggestedRemedy

Replace TBD with 62 GHz

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #60.

Cl **176D** *SC* **176D.3.4.4** *P* **603** *L* **30** # 426

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *(bucket)*

"Insertion loss at 26.5625 GHz"

Nyquest frqeuncy in Table 176Dû4 is incorrect

SuggestedRemedy

Change "26.5625 GHz" to "53.125 GHz"

Response *Response Status* **C**

ACCEPT.

Cl **176D** *SC* **176D.3.4.4** *P* **603** *L* **31** # 451

Simms, William NVIDIA

Comment Type **TR** *Comment Status* **A** *(bucket)*

Moot point maybe given table is all TBD, but the frequency should be 53.125GHz

SuggestedRemedy

change to 53.125GHz

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #426.

Cl **176D** *SC* **176D.3.4.4** *P* **603** *L* **34** # 427

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM*

COM values in Table 176Dû4 are TBD

SuggestedRemedy

Replace TBD with 3 dB

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #250.

Cl **176D** *SC* **176D.3.4.5** *P* **604** *L* **1** # 428

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *Editorial (bucket)*

Reference to test procedure is missing

SuggestedRemedy

Add reference to 176D.3.4.4

Response *Response Status* **C**

ACCEPT.

Cl **176D** *SC* **176D.4** *P* **604** *L* **24** # 430

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM*

Minimum COM is TBD

SuggestedRemedy

Replace TBD with 3 dB in Table 176Dû5 and in line 38 of page 604

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #250.

Cl **176D** *SC* **176D.4** *P* **604** *L* **27** # 429

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *Editorial (bucket)*

Table reference is missing

SuggestedRemedy

Add reference of ERL to 176D.4.3.
Add reference of differential-mode to common-mode return loss to 176D.4.4.

Response *Response Status* **C**

ACCEPT.

Cl **176D** *SC* **176D.4.1** *P* **604** *L* **50** # 141

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *COM R_d, R_0*

Missing TBDs

SuggestedRemedy

Ro= 50 ohms
Rdr=50 ohms
RDt=50 ohms
Receiver 3 dB BW=0.55*106.25=58.4375 GHz

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comments #403, #396, and #36.

Cl **176D** *SC* **176D.4.1** *P* **605** *L* **10** # 142

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *COM TxFFE*

Transmitter equalizer coefficients

SuggestedRemedy

Given little benefit of TX FFE C(-3) - NA
C(0)=0.65
C(-1)= [-0.3:0.02:0]
C(-2)=[0:.02:0.14]
C(1)=[-0.14:.02:0.14] also goes positive to allow slowing driver for reflection mitigation

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #37.

Cl **176D** *SC* **176D.4.1** *P* **605** *L* **16** # 122

Sakai, Toshiaki — Socionext

Comment Type **T** *Comment Status* **A** *COM pkg tau (bucket)*

COM reference package parameter vlaue. (transmission line parameter tau)
In "Table 176Dû6" class A package model Transmission line parameter t(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

SuggestedRemedy

Change t(tau) value in Table 176D-6 (class A package) from 6.141e-4 ns/mm to 6.141e-3 ns/mm.
Or simply delete this row, as the t(tau) value in table 93A-3 is 6.141e-3 ns/mm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #118.

Cl **176D** *SC* **176D.4.1** *P* **605** *L* **26** # 123

Sakai, Toshiaki — Socionext

Comment Type **T** *Comment Status* **A** *COM pkg tau (bucket)*

COM reference package parameter vlaue. (transmission line parameter tau)
In "Table 176Dû6" classB package model Transmission line parameter t(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

SuggestedRemedy

Change t(tau) value in Table 176D-6 (class B package) from 6.141e-4 ns/mm to 6.141e-3 ns/mm.
Or simply delete this row, as the t(tau) value in table 93A-3 is 6.141e-3 ns/mm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #118.

Cl **176D** *SC* **176D.4.1** *P* **605** *L* **35** # 431

Li, Tobey — MediaTek

Comment Type **TR** *Comment Status* **A** *R_0*

Single-ended reference resistance R0 value in Table 176Dû6 is TBD

SuggestedRemedy

Replace TBD with 50 Ohm

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #403.

Cl **176D** *SC* **176D.4.1** *P* **605** *L* **50** # 432

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM f_r*

Receiver 3 dB bandwidth fr value in Table 176Dû7 is TBD

SuggestedRemedy

Replace TBD with 0.58*fb

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #36.

Cl **176D** *SC* **176D.4.1** *P* **605** *L* **52** # 144

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *COM ref Rx*

C2C reference equalizer should be aligned with C2M and addressing TBDs

SuggestedRemedy

Propose to use fix 25 tap FFE with 1T DFE
Max # of pre-cursor taps = 6
DFE max tap weight = 0.75

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comments #504 and #279.

Cl **176D** *SC* **176D.4.1** *P* **606** *L* **33** # 433

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM CTLE parameters*

Zero 2 frequency and pole 3 frequency of Continuous time filter are inconsistent with Table 178û13

SuggestedRemedy

Replace zero 2 frequency with fb/80
Change pole 3 frequency from "fb" to "fb/80"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

There are several comments on this topic. The editorial team prepared a proposal in slide 15 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01b_2406.pdf.

Use the CTLE parameters from Table 178-13 (which are identical to those in Table 179-16), without change, in Table 176D-6 and C2M (Table 176E-7 and COM parameters table).

Remove fLF from Table 176D-7.

Implement with editorial license.

Cl **176D** *SC* **176D.4.1** *P* **606** *L* **40** # 434

Li, Tobey MediaTek

Comment Type **T** *Comment Status* **A** *COM voltage parameters*

Transmitter differential peak output in Table 176Dû7 is TBD

SuggestedRemedy

Replace Av with 0.413 V
Replace Afe with 0.413 V
Replace Ane with 0.608 V

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The following presentation was reviewed by the task force in the May 2024 interim meeting: https://www.ieee802.org/3/dj/public/24_06/lusted_3dj_01a_2406.pdf

Use the values from slide 4 of the presentation, A_v=A_fe=0.413 and A_ne=0.45, to replace TBD values in Table 176D-7.

Add the editor's note on slide 5 of the presentation.

Cl **176D** *SC* **176D.4.1** *P* **606** *L* **49** # 435

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM T_r*

Transmitter transition time Tr value in Table 176Dû7 is TBD

SuggestedRemedy

Replace TBD with Tr = 4 ps

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #39.

Cl **176D** *SC* **176D.4.2** *P* **607** *L* **31** # 63

Dudek, Mike Marvell

Comment Type **T** *Comment Status* **A** *Channel ILdd (bucket)*

An insertion loss of only 20dB is less than desirable and the equation is TBD. We shouldn't specify the loss at this time

SuggestedRemedy

Change 20dB to TBD.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The value 20 dB was not adopted, and its appearance here is unintended.
Slide 18 of https://www.ieee802.org/3/dj/public/24_01/ran_3dj_01a_2401.pdf states explicitly that the interconnect length is TBD.
Implement suggested remedy with editorial license.

Cl **176E** *SC* **176E.2** *P* **615** *L* **23** # 129

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *Channel ILdd (bucket1p)*

Figure depicts loss should be bump-bump

SuggestedRemedy

...application and the associated ILdd bump-bump budget at 53.125 GHz
To make it more clear Host C2M Component should be changed to Host C2M Device and Module C2M Device

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The C2M loss budget is currently TBD, but it is expected that it will be inclusive of packages.
However, the suggested remedy does not significantly clarify this fact.

Add an editor's note stating that the losses in the diagram are intended to be die to die, and contributions are encouraged.

Cl **176E** *SC* **176E.2** *P* **615** *L* **33** # 130

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **R** *Channel ILdd*

Loss budgets are TBD

SuggestedRemedy

See Ghiasi C2M May-24 Contribution for background on the numbers
IlDD=28 dB
Connector with one via = 3 dB
Module Ildd = 3.6 dB
Host Ildd=21.4 dB

Response *Response Status* **C**

REJECT.
The comment is against Figure 176E-2.
The following presentation was reviewed by the task force in the May 2024 interim meeting:
https://www.ieee802.org/3/dj/public/24_05/ghiasi_3dj_02a_2405.pdf
The comment addresses several open TBDs and the suggested remedy is reasonable, but consensus is not obvious.

The editorial team prepared a proposal in slide 25 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01b_2406.pdf.

Comment #73 suggests 33 dB for the Channel ILdd.

There is no consensus for adopting values. More work toward consensus loss budget for C2M in conjunction with reference receiver parameters is encouraged.

Cl **176E** *SC* **176E.3.3** *P* **617** *L* **10** # 186

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *C2M output*

Host output characteristics need to be defined with consideration of the variable output settings that can result from training.

This will affect the entire subclause 176E.3.3.

SuggestedRemedy

Define the output characteristics using a methodology similar to that of transmitter specifications in 179.9.4.

Use a table similar to Table 179-7 but with different values due to the higher host channel insertion loss budget for C2M.

A detailed proposal will be provided.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The CRG reviewed the editorial team's notes on slides 32-34 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01d_2406.pdf.

Implement the proposed changes on slides 6 and 8 of https://www.ieee802.org/3/dj/public/24_05/ran_3dj_02_2405.pdf, except that for jitter values use the values adopted by comment #204.

In the methodology subclause 176E.5, delete the current content and point to the relevant subclauses of 179.9.4.

Implement with editorial license.

The following straw poll was taken:
Straw poll #E-5 (decision)
I would support implementing the proposed changes on slides 6 and 8 of ran_3dj_02_2405 except that for jitter values use the values adopted by comment #204.
Y: 17 N: 14 A: 9

Cl **176E** *SC* **176E.3.3** *P* **617** *L* **13** # 131

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *B-T filter BW*

3 dB BW is TBD

SuggestedRemedy

propose to use 0.55*Baudrate=58.4375 GHz but in current OCM code we use Butterworth, should the COM for C2M be changed to BT4 fitler?

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolve using the response to comment #60.

[Editor's note: changed line from 33 to 13]

Cl **176E** *SC* **176E.3.3** *P* **617** *L* **35** # 132

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *C2M output*

Eye height and VEC are TBD

SuggestedRemedy

See Ghiasi C2M May-24 Contribution for background on the numbers
VEC=10.7 dB
VEO=8 mV

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Comments #186 through #189 suggest using the CR methodology for transmitter and receiver specifications. Based on resolution of these comments, the output specifications have been changed and do not include the VEC and EH parameters.

Resolve using the response to comment #186.

Cl **176E** *SC* **176E.3.3.3** *P* **620** *L* **32** # 220

Noujeim, Leesa Google

Comment Type **T** *Comment Status* **R** *ERL Tfx*

Practical test fixtures may have discontinuities close to 0.2ns from the host-facing connection (mating interface). If the intent is to remove the test fixture discontinuities from the ERL calculations, we should adjust the 0.2ns

SuggestedRemedy

Change text to "...Tfx equal to twice the delay between the test fixture connector and the test fixture host -facing connection minus 0.2ns or as needed to remove test-fixture discontinuities from the ERL result"

Response *Response Status* **C**

REJECT.
Resolve using the reponse to comment #227.

Cl **176E** *SC* **176E.3.4** *P* **621** *L* **13** # 187

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *C2M output*

Module output characteristics need to be defined with consideration of the variable output settings that can result from training.

This will affect the entire subclause 176E.3.4.

SuggestedRemedy

Define the output characteristics using a methodology similar to that of transmitter specifications in 179.9.4.

Use a table similar to Table 179-7 but with different values due to the lower insertion loss assumed for the module output test.

A detailed proposal will be provided.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #186.

Cl **176E** *SC* **176E.3.4.2** *P* **622** *L* **49** # 221

Noujeim, Leesa Google

Comment Type **T** *Comment Status* **R** *ERL Tfx*

Practical test fixtures may have discontinuities close to 0.2ns from the host-facing connection (mating interface). If the intent is to remove the test fixture discontinuities from the ERL calculations, we should adjust the 0.2ns

SuggestedRemedy

Change text to "...Tfx equal to twice the delay between the test fixture connector and the test fixture host -facing connection minus 0.2ns or as needed to remove test-fixture discontinuities from the ERL result"

Response *Response Status* **C**

REJECT.
Resolve using the reponse to comment #227.

Cl **176E** *SC* **176E.3.5** *P* **621** *L* **7** # 133

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *B-T filter BW*

BW is TBD

SuggestedRemedy

propose to use 0.55*Baudrate=58.4375 GHz

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #60.

Cl **176E** *SC* **176E.3.5** *P* **624** *L* **3** # 188

Ran, Adee
Cisco

Comment Type **TR** *Comment Status* **A** *C2M input*

Host input characteristics need to be defined with consideration of the availability of training.

This will affect the entire subclause 176E.3.5.

SuggestedRemedy

Define the input characteristics using a methodology similar to that of receiver specifications in 179.9.5, with the required changes due to the lack of a cable assembly.

Use a table similar to Table 179-10 but with additional rows for DC common-mode voltage and AC common-mode voltage tolerance.

A detailed proposal will be provided.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The CRG reviewed the editorial team's notes on slide 31 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01d_2406.pdf.

Implement the proposed changes on slides 6-8 of https://www.ieee802.org/3/dj/public/24_05/ran_3dj_01_2405.pdf, with the following exceptions:
- On slide 6, the host input test calibration (based on Figure 110-3b) on bottom left should not use the frequency-dependent attenuator. Instead, a mathematical channel representing the maximum host channel is to be used, with details TBD.
- On slide 7, use TBD instead of 35 dB for module input test 1 and test 2 and for host input test calibration.

Implement with editorial license.

Cl **176E** *SC* **176E.3.6** *P* **628** *L* **26** # 189

Ran, Adee
Cisco

Comment Type **TR** *Comment Status* **A** *C2M input*

Module input characteristics need to be defined with consideration of the availability of training.

This will affect the entire subclause 176E.3.6.

SuggestedRemedy

Define the input characteristics using a methodology similar to that of receiver specifications in 179.9.5, with the required changes due to the lack of a cable assembly and usage of MCB instead of HCB.

Use a table similar to Table 179-10 but with additional rows for DC common-mode voltage tolerance and AC common-mode voltage tolerance.

A detailed proposal will be provided.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #188.

Cl **176E** *SC* **176E.4.1** *P* **632** *L* **6** # 73

Lusted, Kent
Intel Corporation

Comment Type **TR** *Comment Status* **R** *Channel ILdd*

The IL_dd for AUI C2M channel is a TBD

SuggestedRemedy

Set IL_dd = 33 per https://www.ieee802.org/3/dj/public/24_01/lusted_3dj_03_2401.pdf

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #130.

Cl **176E** SC **176E.4.1** P **632** L **6** # 134

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **R** *(bucket1p)*

Loss is TBD

SuggestedRemedy

See Ghiasi C2M May-24 Contribution for background on the numbers
Bump-bump Insertion loss at Nyquist frequency (53.125 GHz) is less than or equal to 28 dB

Response *Response Status* **C**

REJECT.
[Editor's note: changed page from 621 to 632]
The following presentation was reviewed by the task force in the May 2024 interim meeting:
https://www.ieee802.org/3/dj/public/24_05/ghiasi_3dj_02_2405.pdf
The presentation does not include a proposal for equation 176E-3.
Resolve using the response to comment #130

Cl **176E** SC **176E.4.2** P **632** L **48** # 72

Lusted, Kent — Intel Corporation

Comment Type **TR** *Comment Status* **A** *Multiple COM parameters*

The COM parameter values for the AUI C2M electrical interfaces in Annex 176E are different from the AUI C2C

SuggestedRemedy

Create a new COM parameter values table in 176E.4.2 and use the COM parameter values from https://www.ieee802.org/3/dj/public/24_03/lit_3dj_01a_2403.pdf slide 6 and 11, which are:

f_r = 0.58
c(-3) = 0
c(-2) = 0 min, 0.12 max
c(-1) = -0.4 min, 0 max
c(0) = 0.54
c(1) = 0
A_v = 0.413
A_fe = 0.413
A_ne = 0.45
eta_0 = 1.25e-8
SNR_TX = 33
sigma_RJ = 0.01
A_DD = 0.02
R_LM = 0.95
d_w = 5
Nfix = 10
N_g = 1
N_f = 4
N_max = 60
w_max(1) = 1
w_min(1) = 0
b_max(1) = 0.75
b_min(1) = 0

additionally, set MLSE = 0 (not enabled)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
[Editor's note: Page/line changed from 605/50 to 632/48]
There are several comments on this topic. The editorial team prepared a proposal in slide 13 of
https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01b_2406.pdf.

Add a COM table in 176E.4.2 which will replace the reference to Table 176D-7. Use the values in Table 176D-7 with the exception of DER0=2e-5, and the additional values and editor's note on slides 3, 4, and 5 of
https://www.ieee802.org/3/dj/public/24_06/lusted_3dj_01a_2406.pdf.

Implement with editorial license.

Cl **176E** *SC* **176E.5** *P* **633** *L* **12** # 203

Ran, Adee Cisco

Comment Type **TR** *Comment Status* **A** *C2M output*

Measurement methodology for C2M should consider the variable output settings that can result from training. Eye opening parameters with specific transmitter settings are not the relevant metrics for transmitter quality anymore.

The measurement methodology of CR transmitter, which focuses on training-related equalizer parameters and training-independent signal parameters, is more suitable.

SuggestedRemedy

Move the measurement methodology section into another annex that both Clause 179 and Annex 176E can refer to.

A detailed proposal will be provided.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #186.

Cl **176E** *SC* **176E.5.2** *P* **633** *L* **33** # 522

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **A** *C2M output*

decision-feedback equalizer? The table mentions "feed-forward coefficient"

SuggestedRemedy

Update this text

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Comments #186 through #189 suggest using the CR methodology for transmitter and receiver specifications. Based on resolution of these comments, the text subject of this comment will no longer be in the the next draft.

Resolve using the response to comment #186.

Cl **176E** *SC* **176E.5.2** *P* **633** *L* **39** # 135

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **R** *(bucket)*

Eye opening reference receiver parameters will be different between TP1d and TP4a measurement

SuggestedRemedy

Given that number of module plug implementation will have COC or even if there is package it will be core-less ~8 mm so there is no need to add package after HCB given the loss of the HCB and plug boards are similar.
At TP4a this is just the output of the module should be tested with synthetic
- short trace
- long trace
recommendation is to measure at the ASIC ball otherwise we would need at least 2 test cases with Package A and 2 with Package B

Response *Response Status* **C**

REJECT.
The suggested remedy does not propose an actionable (within the draft) remedy.

Cl **176E** *SC* **176E.5.2** *P* **633** *L* **39** # 365

Healey, Adam Broadcom Inc.

Comment Type **T** *Comment Status* **A** *C2M output*

The title of Table 176E-7 suggests that is should contain reference receiver parameters. Many of the parameters in the table are not relevant to a reference receiver or an eye diagram measurement. It is understood that this may become moot if a different test method is adopted, but until this decision is made the table can be trimmed down to remove "TBDs" that will never need to be defined.

SuggestedRemedy

Remove parameters "maximum start frequency", "maximum frequency step", all "transmitter" parameters including "number of signal levels" and "level separation mismatch ratio", "number of samples per unit interval", and "target detector error ratio". It is also questionable whether device termination and package model parameters are needed (they were not used in Annex 120G).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Comments #186 through #189 suggest using the CR methodology for transmitter and receiver specifications. Based on resolution of these comments, the reference receiver table has been replaced by a COM parameters table.

Resolve using the response to comment #186.

Cl **176E** *SC* **176E.5.2** *P* **634** *L* **6** # 439

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM f_r*

Receiver 3 dB bandwidth fr value in Table 176Eû7 is TBD

SuggestedRemedy

Replace TBD with 0.58*fb

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #36.

Cl **176E** *SC* **176E.5.2** *P* **634** *L* **8** # 138

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *COM TxFFE*

Transmitter equalizer coefficients

SuggestedRemedy

Given little benefit of TX FFE C(-3) - NA
C(0)=0.65
C(-1)= [-0.3:0.02:0]
C(-2)=[0:.02:0.14]
C(1)=[-0.14:.02:0.14] also goes positive to allow slowing driver for reflection mitigation

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #37.

Cl **176E** *SC* **176E.5.2** *P* **634** *L* **8** # 65

Dudek, Mike Marvell

Comment Type **T** *Comment Status* **A** *C2M output*

There shouldn't be any Tx parameters in a specification for a reference receiver.

SuggestedRemedy

Delete the rows for transmitter termination resistance, transmitter equalizer coefficients, transmitter differential peak output voltage, transition time, transmitter signal to noise ratio, RLM,

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Comments #186 through #189 suggest using the CR methodology for transmitter and receiver specifications. Based on resolution of these comments, the reference receiver table has been replaced by a COM parameters table.

Resolve using the response to comment #186.

Cl **176E** *SC* **176E.5.2** *P* **634** *L* **34** # 440

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM CTLE parameters*

Pole & zero frequency values of continuous time filter are TBD

SuggestedRemedy

Replace zero 1 frequency, fz1, with fb/2.5 GHz
Replace zero 2 frequency, fz2, with fb/80 GHz
Replace pole 1 frequency, fp1, with fb/2.5 GHz
Replace pole 2 frequency, fp2, with fb GHz
Replace pole 3 frequency, fp3, with fb/80 GHz

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #433.

Cl **176E** *SC* **176E.5.2** *P* **634** *L* **43** # 441

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM T_r*

Transmitter transition time Tr value in Table 176Eû7 is TBD

SuggestedRemedy

Replace TBD with Tr = 4 ps

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #39.

Cl **176E** *SC* **176E.5.2** *P* **634** *L* **50** # 139

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *C2M output*

Jitter and noise parameters are TBD

SuggestedRemedy

See Ghiasi C2M May-24 Contribution for background on the numbers
Eta0=1.25E-8
Transmitter SNR = NA for reference receiver but may use 33 dB for COM code
Transmitter Sigma = NA for reference receiver but may use 0.01 UI for COM code
Transmitter dual-Dirac jitter = NA for reference receiver but may use 0.02 UI for COM code
Transmitter RLM = NA for reference receiver but may use 95% for COM code

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Comments #186 through #189 suggest using the CR methodology for transmitter and receiver specifications. Based on resolution of these comments, the reference receiver table has been replaced by a COM parameters table. Jitter and noise parameters are included in the host and module output specifications.

Resolve using the response to comment #186.

Cl **176E** *SC* **176E.5.2** *P* **635** *L* **50** # 140

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *COM ref Rx*

Reference equalizer is TBD

SuggestedRemedy

Propose to use fix 25 tap FFE with 1T DFE
Max # of pre-cursor taps = 6
DFE max tap weight = 0.75

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the responses to comments #72 and #279.

Cl **176E** *SC* **176E.5.2** *P* **636** *L* **49** # 523

Dawe, Piers — Nvidia

Comment Type **TR** *Comment Status* **A** *(bucket1p)*

"within the time interval t_s +/-0.05 UI and with accumulated probability for each sample weighted by the function w(t) defined by Equation (176E-4)": this makes the measurement too tolerant to jitter.

SuggestedRemedy

Remove the Gaussian weighting function w(t), increase +/-0.05 to +/-0.07, same as TDECQ. This will make VEC look worse, but will be a better measurement to protect the link. Use this method for CR also, with "software channel" ("far end eye measurement") as appropriate.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Comments #186 through #189 suggest using the CR methodology for transmitter and receiver specifications. Based on resolution of these comments, the text subject of this comment will no longer be in the the next draft.

Resolve using the response to comment #186.

Cl **177** *SC* **177** *P* **257** *L* **28** # 22

Liu, Cathy — Broadcom

Comment Type **T** *Comment Status* **R** *Inner FEC coding gain*

This section only mentions that the inner FEC decoder is soft-decision decoder and the details implementation is beyond the scope of the this standard. However, shall we specify the soft-decision decoder's performance bound? If not, the optical PMD BER target or link budget might be missed.

SuggestedRemedy

To specify the soft-decision decoder shall provide TBD dB (say 2dB) coding gain over end-end FEC provided that the error statistics are sufficiently random.

Response *Response Status* **C**

REJECT.
Specifying the effectiveness of the Inner FEC is not as simple a coding gain. It needs include the relationship between the errors on the input, errors on the output, and the effect those errors have on the RS-FEC.
A consensus presentation to appropriately define the expected Inner FEC performance is encouraged.

Cl **177** *SC* **177.1.3** *P* **249** *L* **10** # 81

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *(bucket)*

The second bullet could be written more clearly

SuggestedRemedy

Revise to read "Distributing (collecting) the convolutional interleaved data to (from) eight Inner FEC flows

Response *Response Status* **C**

ACCEPT.

Cl **177** *SC* **177.1.3** *P* **249** *L* **14** # 82

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *(bucket)*

The fifth bullet could be written more clearly

SuggestedRemedy

Revise to read "8:1 interleaving (1:8 deinterleaving) the eight Inner FEC flows to (from) a single flow"

Response *Response Status* **C**

ACCEPT.

Cl **177** *SC* **177.1.4** *P* **250** *L* **25** # 83

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *PAM4 decoding (bucket)*

Indicating PAM4 decoding as optional seems a bit misleading. The P{MD isn't doing soft-decoding in any case, so the FEC must do some sort of decoding to recover the bits from the PAM4 symbols.

SuggestedRemedy

Generalize the label in the box to "Decoding", and explain in the text in 177.5.x that there are multiple options for decoding.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Remove footnote in Figure 177-2.

Cl **177** *SC* **177.1.4** *P* **250** *L* **32** # 543

Rechtman, Zvi Nvidia

Comment Type **T** *Comment Status* **A** *PAM4 decoding (bucket)*

The comment refers to Figure 177û2.
There is a footnote that PAM4 decoding is optional in case of soft decoding.
However, the DataPath is defined using bit streams, also the FEC:IS_UNITDATA_i.indication primitives has two value of 0 or 1, therefore PAM4 decoding must to take place

SuggestedRemedy

Either remove the footnote, or elaborate on the intention of this footnote.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 83.

Cl **177** *SC* **177.4.1** *P* **251** *L* **36** # 605

de Koos, Andras Microchip Technology

Comment Type **T** *Comment Status* **R** *timesync (bucket)*

Due primarily to the convolutional interleaver/deinterleaver, there is a large variation in the input-to-output latency of the Inner FEC sublayer. As such, there is concern that the method to properly calculate the path data delay for the Inner FEC sublayer should be explained in Clause 90, similarly to what is done for the variation from FEC codewords and PCS-lane distribution in clause 90.7.1.

SuggestedRemedy

Do nothing.
Using the general method in Clause 90A, allocating the maximum value of the intrinsic delay to the transmit PHY and the minimum value of the intrinsic delay to the receive PHY, there is no ambiguity.
So it should not be necessary to add to Clause 90 for every new PHY type. The principles laid out in Annex 90A.7 should apply.
If anything, a general note could be added in Clause 177 (or in Clause 45 with the MDIO registers for path data delay values) explaining that the Tx/Rx path data delay values should be calculated following the guidelines in Annex 90A.7, where the maximum latency value is used for the Tx path data delay, and the minimum latency value is used for Rx path data delay.

Response *Response Status* **C**

REJECT.
The suggested remedy does not propose an actionable (within the draft) remedy.
It is not helpful to sprinkle notes related to time synchronization throughout the various sublayer clauses; this was not done in previous clauses/projects. Rather it would be preferable to add the necessary text into Clause 90/Annex 90A. A consensus presentation with a complete proposal is encouraged.

Cl **177** *SC* **177.4.1** *P* **251** *L* **50** # 610

Huang, Kechao — Huawei Technologies Co., Ltd.

Comment Type **T** *Comment Status* **A** *CI (bucket)*

"The convolutional interleaver is composed of 3 delay lines where the first delays the PHYs data by eight
RS-FEC codewords, the second by four RS-FEC codewords and the last adds no delay" is correct only if the Q values are 544/272/136/68 for 200G/400G/800G/1.6T. However, the Q values should be 192/96/48/24 as shown in slides 6-11 of he_3dj_01_2307 for 200G/400G/800G/1.6TbE.

SuggestedRemedy

Suggest to modify Line 50-51 in page 251 as follows:
The convolutional interleaver is composed of three parallel delay lines (numbered 0 to 2), as illustrated in Figure 177û3. Each delay operator ôDö represents a storage element of 40 bits. From one delay line to the next higher delay line, Q delay operators are deleted.
Modify the Q values to 192/96/48/24 for 200G/400G/800G/1.6T

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #366.

Cl **177** *SC* **177.4.1** *P* **251** *L* **51** # 544

Rechtman, Zvi — Nvidia

Comment Type **TR** *Comment Status* **A** *CI (bucket)*

The values of Q and the description of the Convolutional interleaver functionality doesnÆt match the adopted values in he_3dj_01_2307.pdf
The values should be:
200G BASE-R: Q = 192
400G BASE-R: Q = 96
800G BASE-R: Q = 48
1.6T BASE-R: Q = 24

SuggestedRemedy

Modify the Q values to:
200G BASE-R: Q = 192
400G BASE-R: Q = 96
800G BASE-R: Q = 48
1.6T BASE-R: Q = 24

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #366.

Cl **177** *SC* **177.4.1** *P* **252** *L* **9** # 292

Galan, Jose Vicente — Maxlinear Inc

Comment Type **TR** *Comment Status* **A** *CI (bucket)*

The Q values of Convolutional interleaver are not in line with previous contributions, D0.1, D0.2, with the TP2 test vectors of Annex 177A and have to be corrected.

SuggestedRemedy

Q=24 for 1.6TBASE-R, Q=48 for 800GBASE-R, Q=96 for 400GBASE-R and Q=192 for 200GBASE-R

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #366.

Cl **177** *SC* **177.4.1** *P* **252** *L* **9** # 366

He, Xiang — Huawei

Comment Type **TR** *Comment Status* **A** *CI (bucket)*

The Q values are not the same as the baseline adopted.

SuggestedRemedy

According to the adopted baseline, change the Q values as follows:
- 200G BASE-R: Q = 192
- 400G BASE-R: Q = 96
- 800G BASE-R: Q = 48
- 1.6T BASE-R: Q = 24

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **177** *SC* **177.4.1** *P* **252** *L* **18** # 295

Galan, Jose Vicente — Maxlinear Inc

Comment Type **T** *Comment Status* **R** *CI (bucket)*

Usually, a convolutional interleaver switches round-robin from low to high delay lines and the convolutional de-interleaver switches round-robin from high to low delay lines. Why in Figure 177-3 it is defined the other way round?

SuggestedRemedy

Change the convolutional interleaver order if that is the case.

Response *Response Status* **C**

REJECT.
This is consistent with the adopted baseline. It is correct as documented.

Cl **177** *SC* **177.4.1** *P* **252** *L* **19** # 488

Slavick, Jeff — Broadcom

Comment Type **T** *Comment Status* **R** *CI (bucket)*

The delay line for Cl177 starts with feeding data into the longest delay line while Cl184 sends it to the delay line with the shortest delay.

SuggestedRemedy

Change Cl177 to have the Delay Line 0 be the minimal delay and the Delay Line 2 to be the longest delay.

Response *Response Status* **C**

REJECT.
This is consistent with the adopted baseline. It is correct as documented.

Cl **177** *SC* **177.4.1** *P* **256** *L* **50** # 545

Rechtman, Zvi — Nvidia

Comment Type **TR** *Comment Status* **A** *CI - Editorial (bucket)*

The description in "The convolutional interleaver is composed of 3 delay lines where the first delays the PHYs data by eight RS-FEC codewords, the second by four RS-FEC codewords and the last adds no delay"
Seems to represent block interleave and not convolutional interleave.

SuggestedRemedy

Modify to:
"The convolutional interleaver is composed of 3 delay lines.
For 200GBASE-R the first line (line0) delays the PHYs data by 4x2x192 = 1,536 RS-FEC Symbols, the second line (line1) by 4x1x192 = 768 RS-FEC symbols and the last line (line3) adds no delay.
For 400GBASE-R the first line (line0) delays the PHYs data by 4x2x96 = 768 RS-FEC Symbols, the second line (line1) by 4x1x96 = 384 RS-FEC symbols and the last line (line3) adds no delay
For 800GBASE-R the first line (line0) delays the PHYs data by 4x2x48 = 384 RS-FEC Symbols, the second line (line1) by 4x1x48 = 192 RS-FEC symbols and the last line (line3) adds no delay
For 1.6TBASE-R the first line (line0) delays the PHYs data by 4x2x24= 192 RS-FEC Symbols, the second line (line1) by 4x1x24 = 96 RS-FEC symbols and the last line (line3) adds no delay.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggest remedy with editorial license.

Cl **177** *SC* **177.4.1** *P* **256** *L* **53** # 546

Rechtman, Zvi — Nvidia

Comment Type **T** *Comment Status* **A** *CI - Editorial (bucket)*

The input and output round-robin operation is defined relatively to the delay/buffering size of each lane. However, there are lines index that represent the delay and simplify the definition.

SuggestedRemedy

Change:
"The input data round-robins between the three delay lines beginning with the eight RS-FEC delay line, then the four RS-FEC delay line and lastly the zero delay line. The output of the convolutional interleaver round-robins between the three delay lines receiving one RS-FEC symbol-quartet from each at a time beginning with the eight RS-FEC delay line, then four RS-FC delay line, and lastly the zero delay line"

To:
"The input data round-robins between the three delay lines beginning with the line0, then line1 delay line and lastly line2. The output of
the convolutional interleaver round-robins between the three delay lines receiving one RS-FEC symbol-quartet (4 symbols) from each at a time beginning with line0, then line1, and lastly line2"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggest remedy with editorial license.

Cl **177** *SC* **177.4.3** *P* **252** *L* **37** # 606

de Koos, Andras — Microchip Technology

Comment Type **T** *Comment Status* **R** *Circular Shift (bucket)*

I'm not convinced that the circular shift really adds any robustness. Yes, it distances bit-pairs belonging to the same RS-FEC codeword, butà
Without the shift, the consecutive bit pairs (after 8:1 multiplexing) belonging to the same RS-FEC code words would each protected by different Inner FEC code words, would they not?
So is the circular shift just protecting against uncorrected inner-FEC codewords that would all land on the same RS-FEC codeword? Seems overkill. Are there simulations/models showing the benefit of including circular shift?

SuggestedRemedy

Consider removing the circular shift if it does not offer any worthwhile benefit.

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **177** *SC* **177.4.3** *P* **252** *L* **37** # 607

de Koos, Andras — Microchip Technology

Comment Type **T** *Comment Status* **R** *Circular Shift (bucket)*

Was there not a proposal to make the circular shift optional, in order to minimize latency?

SuggestedRemedy

Consider removing the circular shift if it does offer not any worthwhile benefit.

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **177** *SC* **177.4.4** *P* **253** *L* **48** # 612

Huang, Kechao — Huawei Technologies Co., Ltd.

Comment Type **T** *Comment Status* **A** *inner FEC code (bucket)*

"The generation matrix G(60,8) for the Hamming(68,60) encoder is given in Table 177-1" is not accurate. The generation matrix for the Hamming(68,60) should be with 60 rows and 68 columns, where the most-left 60 columns is the indentity matrix.

SuggestedRemedy

Suggest to change the sentence to "The generator matrix of the Hamming(68,60) code is G=[I_60 ; G_(60x8)],where I_60 is the 60x60 identity matrix, and G_(60x8) is a 60x8 matrix used to generate the 8 parity bits given in Table 177-1."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The following presentation was reviewed by the 802.3dj task force at the May Interim meeting.
https://www.ieee802.org/3/dj/public/24_05/huang_3dj_01a_2405.pdf
Implement the suggested remedy with editorial license.

Cl **177** *SC* **177.4.4** *P* **253** *L* **48** # 611

Huang, Kechao — Huawei Technologies Co., Ltd.

Comment Type **T** *Comment Status* **A** *inner FEC code (bucket)*

The systematic Hamming code is most naturally defined in terms of its parity-check matrix, as pointed out in many textbooks and standard documents. One famous example is the systematic double-extended Hamming(128,119) code in OIF-400ZR and ITU-T G.709.3.

SuggestedRemedy

Suggest to include the construction process and parity-check matrix of the adopted Hamming(68,60) code to enhance the completeness of the document. A Supporting Presentation will be provided.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The following presentation was reviewed by the 802.3dj task force at the May Interim meeting.
https://www.ieee802.org/3/dj/public/24_05/huang_3dj_01a_2405.pdf
Implement the suggested remedy with editorial license.

Cl **177** *SC* **177.4.6** *P* **254** *L* # 608

de Koos, Andras — Microchip Technology

Comment Type **T** *Comment Status* **A** *pad insertion (bucket)*

A figure illustrating the pad bits and their interval for each inner FEC flow would be useful. I always find myself referring to the equivalent RS-FEC Figures (Figure 119û6 and Figure 119û8)

SuggestedRemedy

Consider adding a figure illustrating the pad insertion and interval, in the same style as Figure 119-6

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggest remedy with editorial license.

Cl **177** *SC* **177.4.6** *P* **254** *L* **31** # 604

de Koos, Andras — Microchip Technology

Comment Type **T** *Comment Status* **R** *timesync (bucket)*

Phase of inner FEC pad bits vs outer FEC parity bits:
- An inaccuracy in the path data delay of up to 12ps due to arbitrary phase between the output FEC parity bits and the inner FEC pad bits of the phase is not accounted for.
- This arbirtary phase would affect the path data delay values.
- Almost negligible, if my math is correct.

SuggestedRemedy

3 possible ways to address:
a. Impose a phase relationship between the RS FEC code word boundaries and the inner FEC pad bits, which would mean large-scale changes to the draft.
b. Specify (in clause 90, perhaps) that the path data delay contribution through the inner FEC sublayer shall be strictly additive to the path data delay contribution through the PCS and PMA layers.
c. Ignore. Based on 90A.7, the effect here is small enough to not address specifically. "Whether the potential delay difference between the aggregated delay and the sum of the individual function delays is small enough to satisfy the timing requirements is up to the individual application."
I prefer option (c). It should not be necessary to add specific text or impose new logical rules to the Inner FEC pad bits to address a potential 12ps path data delay impairment.

Response *Response Status* **C**

REJECT.
The following related presentation was reviewed by the 802.3dj task force at the May Interim meeting.
https://www.ieee802.org/3/dj/public/24_05/he_3dj_01a_2405.pdf
It appeared that there was no consensus to make any related changes to the draft.

Cl **177** *SC* **177.4.6** *P* **254** *L* **33** # 296

Galan, Jose Vicente — Maxlinear Inc

Comment Type **T** *Comment Status* **A** *pad insertion (bucket)*

It is not declared when the first pad insertion should happen.

SuggestedRemedy

Indicate in the text that the first pad insertion will happen right at the beginning of CWs, same as in the test vectors.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggest remedy with editorial license.

Cl **177** *SC* **177.4.6** *P* **254** *L* **44** # 84

Huber, Thomas — Nokia

Comment Type **T** *Comment Status* **A** *pad insertion (bucket1p)*

The last parargaph on p254 is not necessary - implementations are always free to do things in different orders, as long as the end result matches the specified behavior.

SuggestedRemedy

Delete the paragraph.

Response *Response Status* **C**

ACCEPT.

Cl **177** *SC* **177.4.6** *P* **254** *L* **44** # 489

Slavick, Jeff — Broadcom

Comment Type **T** *Comment Status* **A** *pad insertion (bucket1p)*

The last paragraph describing options for how the pad insertion could be done is unnecessary. The requirement that it ocurs every 8704 CW and follows the Figure 177-6 is sufficient.

SuggestedRemedy

Remove the last paragraph of 177.4.6

Response *Response Status* **C**

ACCEPT.

Cl **177** *SC* **177.4.6.1** *P* **255** *L* **25** # 174

Ramesh, Sridhar — Maxlinear Inc

Comment Type **E** *Comment Status* **A** *(editorial)*

"Pad frame sequence" naming does not convey purpose in alignment. Suggest to call this field "Frame Alignment Sequence" instead.

SuggestedRemedy

Pad Frame Alignment Sequence

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement with editorial license and discretion.

Cl **177** *SC* **177.4.6.2** *P* **255** *L* **49** # 297

Galan, Jose Vicente Maxlinear Inc

Comment Type **T** *Comment Status* **A** *pad insertion (bucket)*

The details of how ot use the IBSF are beyond the scope of this standard. Does it mean this is vendor discretionary ? Or will it be defined in other standard ?

SuggestedRemedy

Clarify in the text where the use of the IBSF will be defined.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggest remedy with editorial license.

Cl **177** *SC* **177.4.7.2** *P* **256** *L* **12** # 547

Rechtman, Zvi Nvidia

Comment Type **TR** *Comment Status* **A** *precoding*

The 128,120 Hamming code is very sensitive to error propagation since it can correct up to one error in hard decoding and three errors in soft decoding. Hence, precoding is required

SuggestedRemedy

Add precoding, and use the same definition of precoding similar to 176.9.1.2.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Background and proposed changes are provided on slides 4 to 10 in the the following presentation:
https://www.ieee802.org/3/dj/public/24_06/brown_3dj_02_2406.pdf

Implement the proposed text on slides 8 and 9 of brown_3dj_02_2406.

Implement with editorial license.

Cl **177** *SC* **177.4.7.2** *P* **256** *L* **13** # 582

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *precoding*

Pre-coding was shown on riani_3dj_01a_2303 FECI baseline that when was adopted, and pre-coding is essential for FECi PMDs

SuggestedRemedy

Please insert text for pre-coder in this sub-clause. as specified in 135.5.7.2, 120.5.7.2, and 173.5.7.2, 6 and 176.9.1.2, that may be enabled or disabled as needed with OLT, without OLT the optical transmitter should enable 1/(1+D) mod 4 precoding to mitigate burst error. See Ghiasi/Riani May-24 presentation on the need for pre-coder

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using response to comment #547

Cl **177** *SC* **177.5** *P* **256** *L* **24** # 85

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *Precoding*

According to figure 177-2, the first process the receiver performs is PAM4 decoding (or soft-decision decoding).

SuggestedRemedy

Add a subclause for the decoding process.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #547.

Cl **177** *SC* **177.5.1** *P* **256** *L* **25** # 86

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **R** *Inner FEC Sync (bucket)*

This subclause is confusing and seems to be prescribing a specific implementation. The goal of the process is to find codeword boundaries and remove the pad. If we simply reverse the processes of the tx, this process would (in a logical sense) be performed on the interleaved stream, and would search for the (interelaved) FS pattern

SuggestedRemedy

Rewrite the text to describe searching for the FS pattern and finding it at the expected interval

Response *Response Status* **C**

REJECT.
The comment does not provide sufficient justification to support the suggested remedy.
The existing text is consistent with the adopted baseline.

Cl **177** *SC* **177.5.1** *P* **256** *L* **50** # 490

Slavick, Jeff — Broadcom

Comment Type **T** *Comment Status* **A** *Inner FEC Sync (bucket)*

Monitor and drop says you monitor on all flows. But Figure 177-7 is a per flow state diagram. So is each Flow checking for 140 bad out of 150? And 150 is not a multiple of 8 for it to span across all flows evenly.

SuggestedRemedy

Change:
"keeps monitoring 150 consecutive codewords on all flows, if at least 140 codewords are invalid, drop sync and restart from step a). "
To:
"each flow counts the number of invalid codewords seen in consecutive non-overlapping 150 codeword windows, if at least 140 codewords are invalid, drop sync and restart from step a). "

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggest remedy with editorial license.

Cl **177** *SC* **177.5.1** *P* **257** *L* **1** # 609

de Koos, Andras — Microchip Technology

Comment Type **T** *Comment Status* **A** *Inner FEC Sync (bucket)*

A figure illustrating the possible one bit-pair of skew and the relationship to the Inner FEC flows would be very helpful here. I only understand because I recall the Task Force presentations!

SuggestedRemedy

Consider adding a figure illustrating how the position of the 1 bit-pair of skew determines the Inner FEC flow number.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggest remedy with editorial license.

Cl **177** *SC* **177.5.3** *P* **257** *L* **29** # 183

Brown, Matt — Alphawave Semi

Comment Type **T** *Comment Status* **A** *counters (bucket)*

177.5.3 lists a few counter to be supported by the inner FEC. The defintion for some of these could be improved. Further, additional counters should be included provides bins of error counts to help estimate quality of the link.

SuggestedRemedy

A contribution with more details will be provided.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The following presentation was reviewed by the 802.3dj task force at the May Interim meeting: https://www.ieee802.org/3/dj/public/24_05/brown_3dj_05a_2405.pdf.

Implement slides 6, 7, and 9 with editorial license.

Cl **177** *SC* **177.5.3.1** *P* **257** *L* **45** # 493

Slavick, Jeff — Broadcom

Comment Type **T** *Comment Status* **A** *Inner FEC decode (bucket)*

Defining how a miscrorected codeword can occur could be phrased more clearly.

SuggestedRemedy

Change:
ôNote that for soft-decision decoded Inner FEC codewords, when there is more than one bit error in a codeword, there is always a non-zero chance that miscorrection could happen.ô
To:
ôNote that when there is more than one bit error in a codeword there is a chance that the soft decision decoder could miscorrect the codeword.ô

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **177** *SC* **177.6** *P* **262** *L* **5** # 505

Ren, Hao — Huawei

Comment Type **TR** *Comment Status* **A** *Inner FEC Sync*

In Figure 177-8, the input variable of state FS_LOCK_INIT is not correct. It would cause a FS lock error.

SuggestedRemedy

FS_LOCK_INIT state should be entered after all the 8 flows obtain their inner FEC codeword boundaries and inner FEC flow 0 is identified, when fs_lock is false.

Propose change:
Change the input variable from ' !all_synced ' to ' all_synced * !fs_lock '.

Change the definition of all_synced
from
'A Boolean variable that is set to true when sync_flow<x> is true for all eight flows and is set to false when sync_flow<x> is false for any x.'
to
'A Boolean variable that is set to true when inner FEC flow 0 is identified and is set to false when sync_flow<x> is false for any x.'
(in page 258 line 48-50)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Background and proposed changes are provided on slides 4 and 5 in the following presentation:
https://www.ieee802.org/3/dj/public/24_06/nicholl_3dj_01_2406.pdf.

Implement the proposed changes shown on slide 5 of nicholl_3dj_01_2406, with editorial license.

Cl **177** *SC* **177.6.2.1** *P* **258** *L* **52** # 492

Slavick, Jeff — Broadcom

Comment Type **T** *Comment Status* **R** *Inner FEC Sync (bucket1p)*

Countes automagically have a _done variable created for them, so no need to define fc_cnt_done

SuggestedRemedy

Remove fc_cnt_done definition

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **177** *SC* **177.6.2.3** *P* **260** *L* **3** # 176

Ramesh, Sridhar — Maxlinear Inc

Comment Type **TR** *Comment Status* **A** *counters (bucket)*

Counters defined here do not seem consistent with those defined in Table 177-4.

SuggestedRemedy

Please make definitions of counters consistent with status variables shown on Table 177-4, page 263

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 183.

Cl **177** *SC* **177.6.2.3** *P* **260** *L* **3** # 175

Ramesh, Sridhar — Maxlinear Inc

Comment Type **TR** *Comment Status* **A** *counters (bucket)*

Add a counter for uncorrectable codewords (detected with additional one bit parity)

SuggestedRemedy

uncorr_cw_cnt
Countes the number of inner FEC codewords considered uncorrectable by inner FEC decoder

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment # 183.

Cl **177** *SC* **177.6.3** *P* **262** *L* **8** # 491

Slavick, Jeff — Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

In Figure 177-8 the wrong character is showing up for the <= symbol

SuggestedRemedy

Fix <= symbol in Figure 177-8

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement with editorial license and discretion.

Cl **177** *SC* **177.10** *P* **264** *L* **28** # 182

Brown, Matt — Alphawave Semi

Comment Type **T** *Comment Status* **R** *Skew (common)*

In order for the Inner FEC in combination with the SM-PMA above to interoperate with the already specified 200GBASE-R, 400GBASE-R, and 800GBASE-R PCS, the total skew introduced by the Inner FEC plus the SM-PMA above should be no higher than the the BM-PMA defined for each rate. Furthermore, the skew should exclude the systematic skew that is added then removed by the 8:1 and 16:2 SM-PMA for 200G/400G.

SuggestedRemedy

Specify the maximum skew for the combination of Inner FEC sublayer and the SM-PMA sublayer above it, excluding the systematic skew added then removed by the SM-PMA. A number needs to be determined.

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **177A** *SC* **177A** *P* **643** *L* **5** # 306

Maki, Jeffery — Juniper Networks

Comment Type **T** *Comment Status* **A** *(bucket)*

Annex title unnecessarily uses the acronym IMDD. Not clear what purpose is achieved that cannot be achieved simply by omitting the use of the acronym IMDD.

SuggestedRemedy

Delete the acronym IMDD.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Change title to "Test vectors for 200GBASE-R, 400GBASE-R, 800GBASE-R, and 1.6TBASE-R Inner FEC"

Cl **178** *SC* **178** *P* **270** *L* **17** # 23

Liu, Cathy — Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

Table 178-4 "120F-1.6TGAUI-16 C2C'

SuggestedRemedy

change to "120F-1.6TAUI-16 C2C'

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **178** *SC* **178.1** *P* **268** *L* **45** # 364

Healey, Adam — Broadcom Inc.

Comment Type **T** *Comment Status* **A** *(bucket)*

The Annex 176A control function is required and should be included in Table 178-1 (as is done in Table 179-1).

SuggestedRemedy

Add "176A - Control" as "Required" in Tables 178-1, 178-2, 178-3, and 178-4.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **178** *SC* **178.8.9** *P* **275** *L* **33** # 363

Healey, Adam — Broadcom Inc.

Comment Type **T** *Comment Status* **A** *(bucket)*

The reference to 179.8.9 seems inappropriate here since that subclause contains cross-references specific to the Clause 179.

SuggestedRemedy

Replicate the content of 179.8.9 here, replacing references to Clause 179 electrical requirements to the corresponding references in Clause 178.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **178** *SC* **178.9.1** *P* **275** *L* **39** # 395

Kocsis, Sam — Amphenol

Comment Type **T** *Comment Status* **R** *R_0*

The reference impedance should match the system impedance, Rd as defined in COM spreadsheets.

SuggestedRemedy

92-ohm, TBD, or straw poll based on proposed values presented in Task Force contributions

Response *Response Status* **C**

REJECT.
The suggested remedy does not provide sufficient detail for the CRG to understand the requested changes, e.g., which specifications and measurements should use the proposed reference impedance.

There's no consensus to make changes. Further work and consensus building on this topic is encouraged.

Cl **178** SC **178.9.2** P **275** L **48** # 60

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *B-T filter BW*

The Bessel-Thomson filter should track fr. Between 0.5 fb and 0.6 fb have been shown in presenations.

SuggestedRemedy

change TBD to 67GHz

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The comment addresses an open TBD and the suggested remedy is reasonable.

There are several comments on this topic. The editorial team prepared a proposal in slide 4 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01_2406.pdf.

Use 60 GHz for signal measurements in 178, 179, 176D, 176E. Replace all TBDs and the "40 GHz" that wasn't adopted.

Cl **178** SC **178.9.2** P **275** L **48** # 230

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *B-T filter BW*

3dB BW is TBD

SuggestedRemedy

Change it to 65 GHz.
Rational, considering the common and cost effective 1.85mm connector BW, and associated ~7% measurement error, give rise to this number.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #60.

Cl **178** SC **178.9.2** P **275** L **49** # 399

Li, Tobey — MediaTek

Comment Type **TR** *Comment Status* **A** *B-T filter BW*

Transmitter measurement bandwidth is TBD

SuggestedRemedy

Replace TBD with 62 GHz

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #60.

Cl **178** SC **178.9.2** P **276** L **19** # 231

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *ERL*

dERL (min) is TBD

SuggestedRemedy

Change it to -3 dB. See lim_3dj_01_2403a.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #29.

Cl **178** SC **178.9.2** P **276** L **38** # 236

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *TX jitter*

Output jitter (max) TBD

SuggestedRemedy

reapcle TBDs with:
Jrms : 0.023 UI
J2.7u03: 0.102 UI
J2.7u: 0.110 UI
Even--odd jitter, pk-pk: 0.025 UI
See lim_3dj_01_2403a, lim_3dj_01_2405, and [1], [2], [3]

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #204.

Cl **178** SC **178.9.2.1.2** P **277** L **37** # 28

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *ERL*

scale ERL parameter form 0.3ck

SuggestedRemedy

in table 178-7 change TBD's as follows
Tr 0.005 ns
■x 0 GHz
?x 0.618
N 400 UI

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #29.

Cl **178** *SC* **178.9.2.2** *P* **278** *L* **26** # 237

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *ERL*

Tr is TBD

SuggestedRemedy

repalce it with 0.005 ns, see lim_3dj_01_2403a

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #29.

Cl **178** *SC* **178.9.2.2** *P* **278** *L* **26** # 29

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *ERL*

scale ERL parameter form 0.3ck

SuggestedRemedy

in table 163-7 change TBD's as follows
Tr 0.005 ns
■x 0 GHz
?x 0.618
N 400 UI

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
It is assumed based on the subclause/page/line, the suggested remedy seems to ask to change Table 178-8.

The comment addresses an open TBD and the suggested remedy is reasonable.

There are several comments on this topic. The editorial team prepared a proposal in slide 5 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01_2406.pdf.

For the ERL tables in the following subclauses:
178.9.2.2, 178.9.2.1.2, 178.10.3, 179.9.4.8, 179.11.3, 179B.4.2
And the corresponding tables in annex 176D and annex 176E, use the following values:
Tr = 0.005 ns
beta_x = 0
rho_x = 0.618

Additionally, use the following values:
178.9.2.2: N=400, min dERL=-3 dB
178.9.2.1.2: N=400
178.10.3: N=7000, min ERL=11 dB
179.9.4.8: N=1600
179B.4.2: N=1600, tw=1, DER0=2e-5

Cl **178** *SC* **178.9.2.2** *P* **278** *L* **27** # 238

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *ERL*

Betax is TBD

SuggestedRemedy

repalce it with 0 GHz, see lim_3dj_01_2403a

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #29.

Cl **178** *SC* **178.9.2.2** *P* **278** *L* **29** # 239

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *ERL*

Rox is TBD

SuggestedRemedy

repalce it with 0.618, see lim_3dj_01_2403a

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #29.

Cl **178** *SC* **178.9.2.2** *P* **278** *L* **31** # 240

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *ERL*

N is TBD

SuggestedRemedy

repalce it with 400, see lim_3dj_01_2403a

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #29.

Cl **178** *SC* **178.9.2.2** *P* **278** *L* **32** # 241

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *ERL*

Nbx is TBD

SuggestedRemedy

repalce it with 44, see lim_3dj_01_2403a, lim_3dj_01_2405

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #29.

Cl **178** *SC* **178.9.3** *P* **280** *L* **9** # 244

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *ERL*

dERL is TBD

SuggestedRemedy

repalce it with -3dB, see lim_3dj_01_2403a

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #29.

Cl **178** *SC* **178.9.3.3** *P* **281** *L* **40** # 245

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *B-T filter BW*

3dB BW is TBD

SuggestedRemedy

Change it to 65 GHz.
Rational, considering the common and cost effective 1.85mm connector BW, and associated ~7% measurement error, give rise to this number

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #60.
[Editor's note: Page changed from 280 to 281]

Cl **178** *SC* **178.9.3.3** *P* **281** *L* **41** # 32

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *B-T filter BW*

The Bessel-Thomson filter should track fr which betwee 0.5 and 0.6 has been shown in presenations.

SuggestedRemedy

change TBD to 67GHz

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #60.

Cl **178** *SC* **178.9.3.3** *P* **282** *L* **12** # 246

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *BER/FLR*

FEC symbol error ratio is not aligned with DER value

SuggestedRemedy

change it to 2e-3

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The CRG reviewed the editorial team's notes on slide #24 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01d_2406.pdf.

Resolve using the response to comment #205.

Cl **178** *SC* **178.9.3.3** *P* **282** *L* **16** # 400

Li, Tobey — MediaTek

Comment Type **TR** *Comment Status* **A** *COM*

COM values in Table 178û10 are TBD

SuggestedRemedy

Replace TBD with 3 dB

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #250.

Cl **178** *SC* **178.9.3.3** *P* **282** *L* **16** # 249

Li, Mike Intel

Comment Type **TR** *Comment Status* **A** *COM*

COM for test1 and test2 are TBDs

SuggestedRemedy

Repalced both with 3 dB, see lim_3dj_01_2405

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #250.

Cl **178** *SC* **178.9.3.4** *P* **282** *L* **45** # 401

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *RX ITOL/JTOL (bucket)*

"The test channel COM, calculated per items 3) through 7) in 93C.2, is at least 3 dB"

The reference to the test channel COM is wrong.

SuggestedRemedy

Change it to "The test channel COM, calculated peritem e) through h) in 178.9.3.3, is at least 3 dB" to be correct

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **178** *SC* **178.10** *P* **284** *L* **11** # 402

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM*

Minimum COM in Table 178û11 is TBD

SuggestedRemedy

Replace TBD with 3 dB in Table 178-11 and in line 28 of page 284

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #250.

Cl **178** *SC* **178.10** *P* **284** *L* **11** # 33

Mellitz, Richard Samtec

Comment Type **TR** *Comment Status* **A** *COM*

Use 3 dB as minimum COM as in .3ck or

SuggestedRemedy

change TBD to 3 (same in 178.10.1 line 28)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #250.

Cl **178** *SC* **178.10** *P* **284** *L* **11** # 250

Li, Mike Intel

Comment Type **TR** *Comment Status* **A** *COM*

COM(min) is TBD

SuggestedRemedy

Repalced both with 3 dB, see lim_3dj_01_2405

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The comment addresses an open TBD and the suggested remedy is reasonable.

There are several comments on this topic. The editorial team prepared a proposal in slide 7 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01a_2406.pdf.

Use the value 3 dB for minimum COM for channels and for test setup calibration in Annex 176D.

Use the value 3 dB for minimum COM for channels and for test setup calibration in Clauses 178 and 179.

Cl **178** *SC* **178.10** *P* **284** *L* **12** # 34

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *Channel ILdd (bucket)*

reference is wrong and Ildd should reflect tp0d to tp05d.

SuggestedRemedy

change reference to 178.10.2
and TBD to 40 dB
or eliminate the reference to Ildd

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The objective this clause is addressing is 40 dB die-to-die.
Change the reference to 178.10.2 and the TBD to 40 dB with additional text to state that it is specified from TP0d to TP5d.
Implement with editorial license.

Cl **178** *SC* **178.10** *P* **284** *L* **14** # 252

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *ERL*

Channel ERL TBD

SuggestedRemedy

Repalced it with 11 dB, see oif2023.531.00

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #29.

Cl **178** *SC* **178.10.1** *P* **284** *L* **28** # 253

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *COM*

COM TBD

SuggestedRemedy

Repalced it with 3 dB, see lim_3dj_01_2405

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #250.

Cl **178** *SC* **178.10.1** *P* **285** *L* **18** # 118

Sakai, Toshiaki — Socionext

Comment Type **T** *Comment Status* **A** *COM pkg tau (bucket)*

COM reference package parameter vlaue. (transmission line parameter tau)
In "Table 178û12" class A package model Transmission line parameter t(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

SuggestedRemedy

Change t(tau) value in Table 178-12 (class A package) from 6.141e-4 ns/mm to 6.141e-3 ns/mm.
Or simply delete this row, as the t(tau) value in table 93A-3 is 6.141e-3 ns/mm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The value in D1.0 is a typo.
Change 6.141e-4 to 6.141e-3 in Table 178-12, Table 179-15, and Table 176D-6 (twice in each table).

Cl **178** *SC* **178.10.1** *P* **285** *L* **19** # 356

Healey, Adam — Broadcom Inc.

Comment Type **T** *Comment Status* **A** *COM pkg tau (bucket)*

In Table 178-12, the transmission line parameter "tau" is set to 6.141e-4. In the adopted baseline proposal li_3dj_01a_2311 (slides 8 and 9), the value is specified to be 6.141e-3.

SuggestedRemedy

Replace the "tau" values in the Table 178-12 with the adopted value 6.141e-3 (2 instances). Similarly in Table 179-15 and Table 176D-6.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #118.

Cl **178** *SC* **178.10.1** *P* **285** *L* **28** # 119

Sakai, Toshiaki — Socionext

Comment Type **T** *Comment Status* **A** *COM pkg tau (bucket)*

COM reference package parameter vlaue.
"Table 178û12" class B package model Transmission line parameter t(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

SuggestedRemedy

Change t(tau) value in Table 178-12 (class B package)from 6.141e-4 ns/mm to 6.141e-3 ns/mm.
Or simply delete this row, as the t(tau) value in table 93A-3 is 6.141e-3 ns/mm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #118.

Cl **178** *SC* **178.10.1** *P* **285** *L* **31** # 357

Healey, Adam — Broadcom Inc.

Comment Type **T** *Comment Status* **A** *COM ref pkg (bucket)*

In Table 178-12, the transmision line parameters for the "Class B package model" do not match the adopted baseline proposal li_3dj_01a_2311 slide 9.

SuggestedRemedy

Replace the characteristic impedance for stage 1 with 92 Ohms, and the length/characterstic impedances for stage 2 through 4 with 70 Ohms/1 mm, 80 Ohm/1 mm, and 100 Ohm/0.5 mm respectively. Similarly in Table 179-15 and Table 176D-6.

Response *Response Status* **C**

ACCEPT.

Cl **178** *SC* **178.10.1** *P* **285** *L* **38** # 254

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *R_0*

Ro TBD

SuggestedRemedy

Repalced it w 50 ohm, see see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #403.

Cl **178** *SC* **178.10.1** *P* **285** *L* **38** # 35

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *R_0*

(Table 178û12): Computation can be independent of R0. Add a note to explain. S parameter can utilize any R0. For computation purposes s-parameters are converted to 50 ohms which is the native impedance for the most common test equipment.

SuggestedRemedy

Change R0 for TBD to 50 ohms and add a note indicating the imported s-parameter are to be converted into 50 ohm reference before computation.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Use the value in the response to comment #403.
Add the requested note in all clauses and annexes that include the R0 parameter.
Implement with editorial license.

Cl **178** *SC* **178.10.1** *P* **285** *L* **38** # 403

Li, Tobey — MediaTek

Comment Type **TR** *Comment Status* **A** *R_0*

Single-ended reference resistance R0 value in Table 178-13 is TBD

SuggestedRemedy

Replace TBD with 50 Ohm

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The proposed value of 50 Ohm is in agreement with the reference impedance used for deriving the package models adopted by motions #9 and #10 of November 2023 (see https://www.ieee802.org/3/dj/public/23_11/lusted_3dj_02_2311.pdf).
Any other value would require recalculation of the model parameters in Table 178-12, Table 179-15, and Table 176D-6, and would therefore not be adequate.

Change R_0 from TBD to 50 Ohm in Table 178-12, Table 179-17, Table 176D-6, and in the COM table in Annex 176E added by comment #72.

Cl **178** *SC* **178.10.1** *P* **285** *L* **40** # 396

Kocsis, Sam
Amphenol

Comment Type **T** *Comment Status* **A** *COM R_d*

Rd(t) = "TBD"

SuggestedRemedy

Change "TBD" to "92-ohm" to match majority of contributions to the Task Force, and better align with Zc definition in package

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
There are several comments on this topic. The CRG reviewed the editorial team's notes on slide #8-10 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01c_2406.pdf.

Following straw poll #E-2 (see below) there is consensus to make the following change.
Change Rdt and Rdr in COM device parameters tables (Table 178-12, Table 179-15, Table 176D) from TBD to 46.25 Ohm.
Implement with editorial license.

For the record, there was consensus on having the reference impedance statements (178A.1.3, 178.9.1, 179.9.3, 179.11.1, and 176D.3.2) define a reference single-ended impedance of X Ohm for all frequency-domain specifications, e.g., insertion loss, return loss, and ERL, and adding a similar statement in 176E. The value of X was not decided. This response does not prescribe any changes in this regard.

The following straw polls were taken:

Straw poll #E-1 (direction)
I would support changing Rdt and Rdr in COM device parameters tables (Table 178-12, Table 179-15, Table 176D) from TBD to X Ohm (same as the reference single-ended impedance of X Ohm for all frequency-domain specifications).
Y: 12 N: 12 A: 8

Straw poll #E-2 (direction)
I would support changing Rdt and Rdr in COM device parameters tables (Table 178-12, Table 179-15, Table 176D) from TBD to 46.25 Ohm.
Y: 18 N: 5 A: 9

Cl **178** *SC* **178.10.1** *P* **285** *L* **40** # 255

Li, Mike
Intel

Comment Type **TR** *Comment Status* **A** *COM R_d*

RD(T) TBD

SuggestedRemedy

Repalced it w 46.25 ohm, see see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #396.

Cl **178** *SC* **178.10.1** *P* **285** *L* **41** # 256

Li, Mike
Intel

Comment Type **TR** *Comment Status* **A** *COM R_d*

RD(R) TBD

SuggestedRemedy

Repalced it w 46.25 ohm, see see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #396.

Cl **178** *SC* **178.10.1** *P* **285** *L* **41** # 397

Kocsis, Sam
Amphenol

Comment Type **T** *Comment Status* **A** *COM R_d*

RD(r) = "TBD"

SuggestedRemedy

Change "TBD" to "92-ohm" to match majority of contributions to the Task Force, and better align with Zc definition in package

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #396.

Cl **178** *SC* **178.10.1** *P* **286** *L* **12** # 36

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *COM f_r*

T(able 178û13) Presentations so far have used fr of 0.5, 0.55, 0.58, and 0.6. 67 Ghz limits on test equipment and cabling/connector modal physics suggest at least a 9 dB loss is required for good measurements at 67 GHz. Set fr to 0.6 or lower to achieve this.

SuggestedRemedy

change TBD to 0.6.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

There are several comments on this topic. The editorial team prepared a proposal in slide #12 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01c_2406.pdf.

Use the value 0.55 x f_b for f_r in Table 178-13, Table 179-16, Table 176D-6, and Table 176E-7.

Cl **178** *SC* **178.10.1** *P* **286** *L* **12** # 404

Li, Tobey — MediaTek

Comment Type **TR** *Comment Status* **A** *COM f_r*

Receiver 3 dB bandwidth fr value in Table 178-13 is TBD

SuggestedRemedy

Replace TBD with 0.58*fb

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #36.

Cl **178** *SC* **178.10.1** *P* **286** *L* **12** # 257

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *COM f_r*

fr TBD

SuggestedRemedy

Repalced it w 0.5, see see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolve using the response to comment #36.

Cl **178** *SC* **178.10.1** *P* **286** *L* **12** # 71

Lusted, Kent — Intel Corporation

Comment Type **TR** *Comment Status* **R** *Multiple COM parameters*

The COM parameter values for the 200GBASE-KR1, 400GBASE-KR2, 800GBASE-KR4 and 1.6TBASE-KR8 PMDs are TBDs

SuggestedRemedy

In table 178-13, use the COM parameter values from https://www.ieee802.org/3/dj/public/24_01/healey_3dj_01_2401.pdf slide 18, which are:

f_r = 0.58
c(-3) = 0
c(-2) = 0
c(-1) = 0
c(0) = 1
c(1) = 0
A_v = 0.413
A_fe = 0.413
A_ne = 0.45
eta_0 = 6e-9
SNR_TX = 33
sigma_RJ = 0.01
A_DD = 0.02
R_LM = 0.95
d_w = 5
Nfix = 10
N_g = 0
N_f = 0
N_max = 0
b_max(1) = 0.85
b_min(1) = 0

additionally, set MLSE = 0 (not enabled)

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **178** *SC* **178.10.1** *P* **286** *L* **13** # 405

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM TxFFE*

The max/min values and step size of transmitter equalizer in Table 178-13 need to match those in the Table 178û6 and thost in sub-clauses 179.9.4.1.4 & 179.9.4.1.5

SuggestedRemedy

On line 14 replace TBD with -0.06:0.02:0
On line 18 replace TBD with 0:0.02:0.12
On line 22 replace TBD with -0.34:0.02:0
On line 26 replace TBD with 0.5
On line 28 replace TBD with -0.2:0.02:0

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #37.

Cl **178** *SC* **178.10.1** *P* **286** *L* **14** # 258

Li, Mike Intel

Comment Type **TR** *Comment Status* **A** *COM TxFFE*

C(-3) not needed

SuggestedRemedy

Delete it, see see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolve using the response to comment #37.

Cl **178** *SC* **178.10.1** *P* **286** *L* **18** # 259

Li, Mike Intel

Comment Type **TR** *Comment Status* **A** *COM TxFFE*

C(-2) TBD

SuggestedRemedy

Replace it w
0:0.16:0.02(min,max, step),
see see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolve using the reponse to comment #37.

Cl **178** *SC* **178.10.1** *P* **286** *L* **18** # 37

Mellitz, Richard Samtec

Comment Type **TR** *Comment Status* **A** *COM TxFFE*

Presentations so for have not shown the need for Tx FFE. Change to no TXFFE until further data is provided.
Rx noise may suggest a need for the TXFFE which would improve performance. It's not clear from a channel perspective that the TX FFE is not a zero sum gain compared to the Rx noise loss of COM. Until Rx FFE noise is better defined zero out TxFFE.

SuggestedRemedy

Change TBDs for c(-3),c(-2),c(-1), and c(1) to zero. Set C(0) tp 1.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
There are several comments on this topic. The editorial team prepared a proposal in slide #11 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01c_2406.pdf.

The FFE coefficients in the transmitter characteristics may have larger ranges from those of the COM parameter table.

Use the folowing ranges and step sized for COM Tx FFE coefficients in 178, 179, 176D, and 176E.

c(-3): 0 (not used in COM)
c(-2): 0 to 0.14, in 0.02 steps
c(-1): -0.34 to 0, in 0.02 steps
c(0) minimum: 0.54
c(+1): -0.2 to 0, in 0.02 steps.

Add editor's notes similar to that in slide 4 of https://www.ieee802.org/3/dj/public/24_05/lusted_3dj_07_2405.pdf to denote that the COM FFE ranges need further analysis.

Cl **178** *SC* **178.10.1** *P* **286** *L* **22** # 260

Li, Mike Intel

Comment Type **TR** *Comment Status* **A** *COM TxFFE*

C(-1) TBD

SuggestedRemedy

Replace it w
-0.4.0.0.02 (min,max, step),
see see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the reponse to comment #37.

Cl **178** *SC* **178.10.1** *P* **286** *L* **26** # 262

Li, Mike Intel

Comment Type **TR** *Comment Status* **A** *COM TxFFE*

C(1) TBD

SuggestedRemedy

Replace it w
-0.2.0.0.02 (min,max, step),
see see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the reponse to comment #37.

Cl **178** *SC* **178.10.1** *P* **286** *L* **26** # 261

Li, Mike Intel

Comment Type **TR** *Comment Status* **A** *COM TxFFE*

C(0) TBD

SuggestedRemedy

Replace it w 0.54,
see see lim_3dj_01_2405, slide 5.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the reponse to comment #37.

Cl **178** *SC* **178.10.1** *P* **286** *L* **32** # 263

Li, Mike Intel

Comment Type **TR** *Comment Status* **R** *COM CTLE parameters*

g1 inherited from 802.3ck, no simod support, not approproaite

SuggestedRemedy

Replace them w
-15 :0, 1 (min, max, step)
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

REJECT.
The following presentation was reviewed by the task force at the May 2024 interim meeting:
https://www.ieee802.org/3/dj/public/24_05/lim_3dj_01_2405.pdf
The comment and the presentation do not provide sufficient justification to support the suggested remedy.

There are several comments on this topic. The editorial team prepared a proposal in slide 15 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01b_2406.pdf.

There was no consensus to make the suggested change.

Cl **178** *SC* **178.10.1** *P* **286** *L* **32** # 264

Li, Mike Intel

Comment Type **TR** *Comment Status* **R** *COM CTLE parameters*

g2 inherited from 802.3ck, no simod support, not approproaite

SuggestedRemedy

Replace them w
-5 :0, 1 (min, max, step)
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #263.

Cl **178** *SC* **178.10.1** *P* **286** *L* **40** # 265

Li, Mike — Intel

Comment Type **TR** *Comment Status* **R** *COM CTLE parameters*

fz1,fz2 from 802.3ck, no simod support, not approproaite

SuggestedRemedy

Replace them w
fb/4.223, fb/80 (fz1,fz2)
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #263.

Cl **178** *SC* **178.10.1** *P* **286** *L* **42** # 266

Li, Mike — Intel

Comment Type **TR** *Comment Status* **R** *COM CTLE parameters*

f1,fp2, fp3 from 802.3ck, no simod support, not approproaite

SuggestedRemedy

Replace them w
fb/1.8973, fb/2.6562, fb/80 (fp1,fp2, fp3)
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #263.

Cl **178** *SC* **178.10.1** *P* **286** *L* **46** # 406

Li, Tobey — MediaTek

Comment Type **T** *Comment Status* **R** *COM voltage parameters*

Transmitter differential peak output voltage in Table 178-13 is TBD

SuggestedRemedy

Replace Av with 0.413 V
Replace Afe with 0.413 V
Replace Ane with 0.608 V

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #38.

Cl **178** *SC* **178.10.1** *P* **286** *L* **46** # 267

Li, Mike — Intel

Comment Type **TR** *Comment Status* **R** *COM voltage parameters*

Av, Afe, Ane TBDs

SuggestedRemedy

Replace them w
0.413, 0.413, 0.608 V (Av, Afe, Ane)
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #38.

Cl **178** *SC* **178.10.1** *P* **286** *L* **46** # 38

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **R** *COM voltage parameters*

It not clear the power sources have significantly changed from 0.3ck and to avoid the complication of small voltage requirement from packages use the 0.3ck voltages.

SuggestedRemedy

set Av and Afe to 0.413 and Ane to 0.608

Response *Response Status* **C**

REJECT.

There is no consensus to implement the suggested remedy. Further contributions on this topic are encouraged.

Cl **178** *SC* **178.10.1** *P* **286** *L* **50** # 39

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *COM T_r*

scale Tr from .3ck. Understand that this is not the Tr at TP0d.

SuggestedRemedy

set Tr to 0.00375 ns

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
[Editor's note: Clause changed from 179.10.1]

There are several comments on this topic. The CRG reviewed the editorial team's notes on slide #16 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01c_2406.pdf.

Change T_r from TBD to 4 ps in Table 178-13, Table 179-15, Table 176D-7, and Table 176E-7.
Add editor's notes similar to that in slide 4 of https://www.ieee802.org/3/dj/public/24_05/lusted_3dj_07_2405.pdf to denote that this value needs further analysis.

Cl **178** *SC* **178.10.1** *P* **286** *L* **50** # 407

Li, Tobey — MediaTek

Comment Type **TR** *Comment Status* **A** *COM T_r*

Transmitter transition time Tr value in Table 178-13 is TBD

SuggestedRemedy

Replace TBD with Tr = 4 ps

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #39.

Cl **178** *SC* **178.10.1** *P* **286** *L* **50** # 268

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *COM T_r*

Tr TBD

SuggestedRemedy

Replace it w 0.004 ns
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #39.

Cl **178** *SC* **178.10.1** *P* **286** *L* **53** # 408

Li, Tobey — MediaTek

Comment Type **TR** *Comment Status* **R** *COM eta0*

One sided noise spectral density in Table 178-13 is TBD

SuggestedRemedy

Replace TBD with 6e-9 V^2/GHz

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #269.

Cl **178** *SC* **178.10.1** *P* **286** *L* **53** # 269

Li, Mike — Intel

Comment Type **TR** *Comment Status* **R** *COM eta0*

eta0

SuggestedRemedy

Replace it w 5e-9 V^2/GHz
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

REJECT.

The following presentation was reviewed by the task force at the May 2024 interim meeting: https://www.ieee802.org/3/dj/public/24_05/lim_3dj_01_2405.pdf
The presentation is based on COM4.50draft3 using MLSE. The MLSE implementation within that code is however tentative and has not been fully debugged. Making a decision on the critical eta0 parameter is therefore premature.
The comment and the presentation do not provide sufficient justification to support the suggested remedy.
Although Straw Poll #7 in the May 2024 meeting showed consensus for the value 1e-8 for C2C and C2M, CR/KR were not addressed.
The values 5e-9 and 6e-9 are suggested in other comments.
Further analysis and consensus building are encouraged.

Cl **178** *SC* **178.10.1** *P* **287** *L* **7** # 271

Li, Mike Intel

Comment Type **TR** *Comment Status* **A** *Tx jitter*

sigmaRJ TBD

SuggestedRemedy

Replace it w 0.01 UI,
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement the suggested remedy and apply in addition in the COM tables in clause 179, annex 176D and Annex 176E.

Cl **178** *SC* **178.10.1** *P* **287** *L* **8** # 272

Li, Mike Intel

Comment Type **TR** *Comment Status* **A** *Tx jitter*

ADD TBD

SuggestedRemedy

Replace it w 0.02 UI,
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy and apply in addition in the COM tables in clause 179, annex 176D and Annex 176E.

Cl **178** *SC* **178.10.1** *P* **287** *L* **13** # 274

Li, Mike Intel

Comment Type **TR** *Comment Status* **R** *COM ref Rx*

dw TBD

SuggestedRemedy

Replace it w 6,
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

REJECT.
The following presentation was reviewed by the task force at the May 2024 interim meeting:
https://www.ieee802.org/3/dj/public/24_05/lim_3dj_01_2405.pdf
The comment and the presentation do not provide sufficient justification to support the suggested remedy.

There is no consensus to implement the suggested remedy. Further contributions on this topic are encouraged.

Cl **178** *SC* **178.10.1** *P* **287** *L* **13** # 275

Li, Mike Intel

Comment Type **TR** *Comment Status* **R** *COM ref Rx*

Nfix TBD

SuggestedRemedy

Replace it w 24,
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

REJECT.
The following presentation was reviewed by the task force at the May 2024 interim meeting:
https://www.ieee802.org/3/dj/public/24_05/lim_3dj_01_2405.pdf
The comment and the presentation do not provide sufficient justification to support the suggested remedy.

There is no consensus to implement the suggested remedy. Further contributions on this topic are encouraged.

Cl **178** *SC* **178.10.1** *P* **287** *L* **15** # 276

Li, Mike
Intel

Comment Type **TR** *Comment Status* **R** *COM ref Rx*

Ng TBD

SuggestedRemedy

Replace it w 4,
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

REJECT.
The following presentation was reviewed by the task force at the May 2024 interim meeting:
https://www.ieee802.org/3/dj/public/24_05/lim_3dj_01_2405.pdf
The comment and the presentation do not provide sufficient justification to support the suggested remedy.

There is no consensus to implement the suggested remedy. Further contributions on this topic are encouraged.

Cl **178** *SC* **178.10.1** *P* **287** *L* **16** # 277

Li, Mike
Intel

Comment Type **TR** *Comment Status* **R** *COM ref Rx*

Nf TBD

SuggestedRemedy

Replace it w 5,
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

REJECT.
The following presentation was reviewed by the task force at the May 2024 interim meeting:
https://www.ieee802.org/3/dj/public/24_05/lim_3dj_01_2405.pdf
The comment and the presentation do not provide sufficient justification to support the suggested remedy.

There is no consensus to implement the suggested remedy. Further contributions on this topic are encouraged.

Cl **178** *SC* **178.10.1** *P* **287** *L* **17** # 278

Li, Mike
Intel

Comment Type **TR** *Comment Status* **R** *COM ref Rx*

Namx TBD

SuggestedRemedy

Replace it w 60,
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

REJECT.
The comment appears to address the parameter Nmax.
The following presentation was reviewed by the task force at the May 2024 interim meeting:
https://www.ieee802.org/3/dj/public/24_05/lim_3dj_01_2405.pdf
The comment and the presentation do not provide sufficient justification to support the suggested remedy.

There is no consensus to implement the suggested remedy. Further contributions on this topic are encouraged.

Cl **178** *SC* **178.10.1** *P* **287** *L* **18** # 279

Li, Mike
Intel

Comment Type **TR** *Comment Status* **A** *COM ref Rx*

Wamx(j) TBD

SuggestedRemedy

Replace it w 0.7,
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The comment addresses an open TBD and the suggested remedy is reasonable.

There are several comments on this topic. The editorial team prepared a proposal in slide #14 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01c_2406.pdf.

Use the following values to replace TBDs in COM tables in 178, 179, 176D, and COM table + reference receiver in 176E:
w_max(i) = 0.7 for all i except 0
w_min(i) = -0.7 for all i except 0
b_max = 0.85
b_min = 0

implement with editorial license.

Add editor's notes similar to that in slide 4 of https://www.ieee802.org/3/dj/public/24_05/lusted_3dj_07_2405.pdf to denote that these values need further analysis.

Cl **178** *SC* **178.10.1** *P* **287** *L* **19** # 280

Li, Mike
Intel

Comment Type **TR** *Comment Status* **A** *COM ref Rx*

Wmin(j) TBD

SuggestedRemedy

Replace it w -0.7,
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #279.

Cl **178** *SC* **178.10.1** *P* **287** *L* **20** # 281

Li, Mike
Intel

Comment Type **TR** *Comment Status* **A** *COM ref Rx*

bmaxTBD

SuggestedRemedy

Replace it w 0.85,
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #279.

Cl **178** *SC* **178.10.1** *P* **287** *L* **21** # 282

Li, Mike
Intel

Comment Type **TR** *Comment Status* **A** *COM ref Rx*

bminTBD

SuggestedRemedy

Replace it w 0.3,
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #279.

Cl **178** *SC* **178.10.1** *P* **287** *L* **22** # 283

Li, Mike
Intel

Comment Type **TR** *Comment Status* **A** *COM ref Rx*

no foaltoing tap coefficient max limit

SuggestedRemedy

Added a new line for floating tap coefficeint max limit and set it to 0.05
see lim_3dj_01_2405, slide 5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy for the COM tables in clauses 178, clause 179, annex 176D and annex 176E, with editorial license.

(The value for the floating tap indexes overrides the value 0.7 for fixed tap indexes adopted by comment #279).

Cl **178** *SC* **178.10.1** *P* **287** *L* **23** # 284

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *COM ref Rx*

no foaltoing tap coefficient min limit

SuggestedRemedy

Added a new line for floating tap coefficeint min limit and set it to -0.05
see lim_3dj_01_2405, slide

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy for the COM tables in clauses 178, clause 179, annex 176D and annex 176E, with editorial license.

(The value for the floating tap indexes overrides the value -0.7 for fixed tap indexes adopted by comment #279).

Cl **178** *SC* **178.10.2** *P* **287** *L* # 42

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **R** *Multiple COM parameters*

Selecting values the "Receiver discrete-time equalizer parameters" are critical for making progress. Many presentations a have shown quite a variation. Select values based on what seems consistent or use straw ballot to determine.

SuggestedRemedy

use straw polls from the following
Dw 4, 6, or 8
Nfix 10, 15, 24
Ng 1, 2, 3
Nf 3, 4, 5
Nmax 40 60 120
Wmax(j)=1
Wmin(-1,0,1)=0. otherwise -0.5
bmax(1) = 0,5 0.75 0 85
bmin(1)= 0 -0,5 -0.75 -0 85

Response *Response Status* **C**

REJECT.
The suggested remedy does not propose an actionable (within the draft) remedy.

Proposed changes should preferably be backed by technical justification and not just straw polls.

Cl **178** *SC* **178.10.3** *P* **288** *L* **29** # 43

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *ERL*

scale ERL parameter form 0.3ck

SuggestedRemedy

in table 178-14 change TBD's as follows
Tr 0.005 ns
[redacted]x 0 GHz
?x 0.618
N 7000 UI

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #29.

Cl **178A** *SC* **178A.1.5** *P* **650** *L* **7** # 228

Noujeim, Leesa — Google

Comment Type **T** *Comment Status* **A** *(bucket)*

The port labels on Figure 178A-6 are inconsistent with the cascade order implied in 178A-12 and with the text on line 1.

SuggestedRemedy

In Fig 178A-6 replace "Port 2" with "Port 1" and replace "Port 1" with "Port 2"
Alternatively, replace Figure 178A-6 with a copy of Figure 178A-2 and reverse the arrow directions and swap Port 1 with Port 2.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The comment correctly points out that port ordering conventions (1 is an input, 2 is an output) should be consistently applied.
In Figure 178A-6, label the input to the "Host channel (optional)" as "Port 1" and label the output of the "Device termination" as "Port 2".
Change the last sentence of 178A.1.5 to:
"The port order of the resulting model is then reversed so that port 1 becomes the input to the optional host channel (or the device package when the host channel is not included) and port 2 becomes the output of the device termination."
Implement with editorial license.

Cl **178A** *SC* **178A.1.8** *P* **654** *L* **42** # 209

Shakiba, Hossein — Huawei Technologies Canada

Comment Type **T** *Comment Status* **A** *(bucket)*

Reference to the wrong section 178A.1.6.4

SuggestedRemedy

Change reference to section 178A.1.8.1

Response *Response Status* **C**

ACCEPT.

Cl **178A** *SC* **178A.1.9** *P* **657** *L* **51** # 210

Shakiba, Hossein — Huawei Technologies Canada

Comment Type **T** *Comment Status* **A** *(bucket)*

h_ISI in equation (178A-29) should not include the main cursor (h_ISI(main) = 0)

SuggestedRemedy

Add a case to define h_ISI(n) = 0 for n = d+1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **178A** *SC* **178A.1.10** *P* **658** *L* **43** # 362

Healey, Adam — Broadcom Inc.

Comment Type **T** *Comment Status* **A** *DER0*

The relationship between "detector error ratio", "PAM-L symbol error ratio", and "bit error ratio" is not documented and, as a result, not generally understood. While these quantities are related, they are not interchangeable. Prior assumptions that they are interchangeable has led to errors in the translation between COM results and expected (measured) receiver performance. This new annex gives us an opportunity to clarify the relationship between DER0 and other terms or to replace DER0 with a more generally understood term.

SuggestedRemedy

Slide 5 of <https://www.ieee802.org/3/dj/public/23_11/healey_3dj_01a_2311.pdf> suggest expressions for relationship between detector error ratio and other terms. Either replace "DER0" with a target PAM-4 symbol error ratio (or bit error ratio) and adjust the equations for calculating COM accordingly, or document the relationship between DER0 and the other two terms.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

There are several comments on this topic. The editorial team prepared a proposal in slides 28-29 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01b_2406.pdf.

Implement the changes on slide 29 of ran_3dj_01b_2406, with editorial license.

Cl **178A** *SC* **178A.1.10.2** *P* **659** *L* **12** # 285

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *DER0*

DER0 EQ is wrong

SuggestedRemedy

change P(y0)= DER0 to 1-P(y0) =DER0, see slide 3 of lim_3dj_02_2405, see also a marked version in the support data sheet.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The following contribution was reviewed at the May 2024 interim meeting:
https://www.ieee802.org/3/dj/public/24_05/lim_3dj_02_2405.pdf

Resolve using the response to comment #362.

Cl **178A** *SC* **178A.1.11** *P* **660** *L* **27** # 211

Shakiba, Hossein — Huawei Technologies Canada

Comment Type **T** *Comment Status* **A** *)M methodology MLSD_PAM*

The factor 2/3 in equation (178A-36) is specific to PAM4. This change does not apply if the equation is rewritten.
See contributions lim_3dj_02_2405.pdf and shakiba_3dj_01_2405.pdf.

SuggestedRemedy

Change 2/3 to L/2(L-1) to make it general. Note that L=4 still yields 2/3. Please refer to contribution tbd.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The following contribution was reviewed at the May 2024 interim meeting:
https://www.ieee802.org/3/dj/public/24_05/shakiba_3dj_01_2405.pdf

The modifications to Equations (178A-36) and (178A-37) are also influenced by the responses to comments #285 and #362.

Resolve using the response to comment #362.

[Editor's note: changed subclause to 178A.1.11.]

Cl **178A** *SC* **178A.1.11** *P* **660** *L* **27** # 286

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *)M methodology MLSD_PAM*

EQ (178A-36)

SuggestedRemedy

Update the equation per slide 4 of lim_3dj_02_2405, see also a marked version in the support data sheet.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The following contribution was reviewed at the May 2024 interim meeting:
https://www.ieee802.org/3/dj/public/24_05/lim_3dj_02_2405.pdf
The modifications to Equations (178A-36) and (178A-37) are also influenced by the responses to comments #285 and #362.
Resolve using the response to comment #362.

Cl **178A** *SC* **178A.1.11** *P* **660** *L* **33** # 212

Shakiba, Hossein — Huawei Technologies Canada

Comment Type **T** *Comment Status* **A** *)M methodology MLSD_PAM*

The factor 3/4 in equation (178A-37), as is or rewritten, is specific to PAM4.
See contributions lim_3dj_02_2405.pdf and shakiba_3dj_01_2405.pdf.

SuggestedRemedy

Change 3/4 to (L-1)/L to make it general. Note that L=4 still yields 3/4.Please refer to contribution tbd.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The following contributions were reviewed at the May 2024 interim meeting:
https://www.ieee802.org/3/dj/public/24_05/lim_3dj_02_2405.pdf
https://www.ieee802.org/3/dj/public/24_05/shakiba_3dj_01_2405.pdf
The modifications to Equations (178A-36) and (178A-37) are also influenced by the responses to comments #285 and #362.
Resolve using the response to comment #362.

[Editor's note: changed subclause to 178A.1.11.]

Cl **178A** *SC* **178A.1.11** *P* **660** *L* **33** # 287

Li, Mike — Intel

Comment Type **TR** *Comment Status* **A** *)M methodology MLSD_PAM*

EQ (178A-37)

SuggestedRemedy

Update the equation per slide 4 of lim_3dj_02_2405, see also a marked version in the support data sheet.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolve using the response to comment #362.

Cl **178A** *SC* **178A.1.11.1** *P* **660** *L* **52** # 213

Shakiba, Hossein — Huawei Technologies Canada

Comment Type **T** *Comment Status* **A** *MLSD_PDF (bucket)*

Although clear, the result of the PDF convolution conv[p(y),p(y/b1)] is a PDF and assumed to have been normalized to satisfy the PDF sum requirement.

SuggestedRemedy

Either mention that after convolution, the result should be normalized, or add a normalization coefficient of 1/b1 in font of conv.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
On page 660, line 52, change "conv[p(y), p(y/b1)]" to "conv[p(y), p(y/b1)/|b1|)" where |a| is the absolute value of a.
In Equation (178A-39), change "p(y/(1-b1))" to "p(y/(1-b1))/|1-b1|".
Add a note that states that the operation p(y/a)/|a| scales random variable Y by a factor of a, and that the scaled probability distribution function integrates to 1.
Implement with editorial license.

Cl **178A** *SC* **178A.1.11.1** *P* **661** *L* **1** # 214

Shakiba, Hossein — Huawei Technologies Canada

Comment Type **T** *Comment Status* **A** *MLSD_PDF (bucket)*

Although clear, the result of the PDF convolution of equation (178A-39) is a PDF and assumed to have been normalized to satisfy the PDF sum requirement.

SuggestedRemedy

Either mention that after convolution, the result should be normalized, or add a normalization coefficient of 1/(1-b1) in font of conv.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #213.

Cl **179** *SC* **179.9.3** *P* **309** *L* **14** # 387

Kocsis, Sam — Amphenol

Comment Type **T** *Comment Status* **R** *R_0*

The reference impedance should match the system impedance, Rd as defined in COM spreadsheets.

SuggestedRemedy

92-ohm, TBD, or straw poll based on proposed values presented in Task Force contributions

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #395.

Cl **179** *SC* **179.9.4** *P* **309** *L* **23** # 124

Sakai, Toshiaki — Socionext

Comment Type **T** *Comment Status* **A** *B-T filter BW*

Ttransmitter signal measurement filter bandwidth description.
"Unless specified otherwise, transmitter signal measurements are made for each lane separately using a fourth-order Bessel-Thomson low-pass response with 3 dB bandwidth of 40 GHz, with AC-coupled connection from TP2 to the test equipment."
The 4th-BW filter BW should be "TBD GHz", the same as for CL178.9.2, AN176D.3.3 and AN176E.3.3, as the Nyquist frequency of the signal is 53.125GHz and 40GHz is too low..

SuggestedRemedy

Change 40GHz to TBD GHz.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The value 40 GHz is a leftover from an older clause and has not been adopted.
Resolve using the response to comment #60.

Cl **179** *SC* **179.9.4** *P* **309** *L* **23** # 388

Kocsis, Sam — Amphenol

Comment Type **T** *Comment Status* **A** *B-T filter BW*

BT LP 3dB BW of "40GHz"

SuggestedRemedy

"TBD" as cited in other places of the document

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The value 40 GHz is a leftover from an older clause and has not been adopted.
Resolve using the response to comment #60.

Cl **179** *SC* **179.9.4** *P* **309** *L* **23** # 225

Noujeim, Leesa — Google

Comment Type **T** *Comment Status* **A** *B-T filter BW*

Adopted baseline https://www.ieee802.org/3/dj/public/24_01/ran_3dj_01a_2401.pdf has BT filter bandwidth as TBD but D1.0 has 40GHz. 3dB bandwidth of 40GHz is insufficient for 200Gbps/lane PAM4

SuggestedRemedy

Increase to 65GHz, consistent with test equipment capabilities and demonstrated channel rolloff eg in https://www.ieee802.org/3/dj/public/23_11/weaver_3dj_01_2311.pdf and https://www.ieee802.org/3/dj/public/24_01/benartsi_3dj_01_2401.pdf OR change to TBD

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The value 40 GHz is a leftover from an older clause and has not been adopted.
Resolve using the response to comment #60.

Cl **179** *SC* **179.9.4** *P* **309** *L* **23** # 410

Li, Tobey — MediaTek

Comment Type **TR** *Comment Status* **A** *B-T filter BW*

"4th order Bessel-Thomson filter with 3 dB bandwidth of 40 GHz" is inconsistent with Clause 178.9.2, Annex 176D.3.3, and Annex 176E.3.3

SuggestedRemedy

Change "40 GHz" to either "TBD" or "62 GHz"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The value 40 GHz is a leftover from an older clause and has not been adopted.
Resolve using the response to comment #60.

Cl **179** *SC* **179.9.4.7** *P* **310** *L* **25** # 204

Ran, Adee — Cisco

Comment Type **TR** *Comment Status* **A** *Tx jitter*

Jitter specification is TBD.

Based on https://www.ieee802.org/3/dj/public/adhoc/electrical/24_0104/calvin_3dj_elec_01a_240104.pdf, the jitter measurement methodology of existing clauses 162, 163, and 120G (specifically using the two edges R03/F30) is feasible for measurements with a loss 30 dB. It is expected that the same method can be used for higher losses as long as the scope can maintain CDR lock.

This methodology should be used for all electrical interfaces, with adequate adjustments.

SuggestedRemedy

A detailed proposal will be provided.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The CRG reviewed the editorial team's notes on slides 19-21 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01d_2406.pdf.

For the Transmitter output in Clause 178, Clause 179, and Annex 176D:
Use the jitter parameter Jrms03 (measured only on the R03 and F30 transitions).
With a maximum value of 0.023 UI.
Use the jitter parameter EOJ03 (measured only on the R03 and F30 transitions).
With a maximum value of 0.025 UI.

Use the jitter parameter J3u03 with maximum values of 0.106 UI for class A, 0.108 UI for class B for clause 178.
Use the jitter parameter J3u03 with maximum value of 0.115 UI for host-low, 0.122 for host-nom, 0.128 for host-high for clause 179.
Use the jitter parameter J4u03 with maximum value of 0.118 UI for class A, 0.120 UI for class B for annex 176D.

Add editor's notes near each table, stating that the different values of J3u03/J4u03 are based on the assumption that the measured jitter is affected by the loss to the measurement point, and that further work related to this assumption is encouraged.

For Annex 176E:
Use the jitter parameter Jrms03 (measured only on the R03 and F30 transitions).
With a maximum value of 0.023 UI for both host output and module output.
Use the jitter parameter EOJ03 (measured only on the R03 and F30 transitions).
With a maximum value of 0.025 UI for both host output and module output.
Use the jitter parameter J4u03 with maximum values of 0.118 UI for Module output, 0.135 UI for Host output.

Add editor's notes near each table, stating that the different values of J4u03 between host

output and module output are based on the assumption that the measured jitter is affected by the loss to the measurement point, and not strongly affected by crosstalk in the connector, and that further work related to this assumption is encouraged.

Do not specify J6u03 at this time.

The following straw polls were taken:

Straw poll #E-3 (direction)
I would support using the same J3u03 limits for all CR transmitters regardless of the host class, and similarly the same limits for KR transmitter classes.
Y: 9 N: 10 A: 15

Straw poll #E-4 (decision)
I support using the JRMS03, EOJ03, and J4u03 for C2M host output and module output specifications.
Y: 13 N: 9 A: 12

Cl **179** *SC* **179.9.4.8** *P* **315** *L* **35** # 227

Noujeim, Leesa — Google

Comment Type **T** *Comment Status* **R** *ERL Tfx*

Practical test fixtures may have discontinuities close to 0.2ns from the host-facing connection (mating interface). If the intent is to remove the test fixture discontinuities from the ERL calculations, we should adjust the 0.2ns

SuggestedRemedy

Change text to "...Tfx equal to twice the delay between the test fixture connector and the test fixture host -facing connection minus 0.2ns or as needed to remove test-fixture discontinuities from the ERL result"

Response *Response Status* **C**

REJECT.
There are several comments on this topic. The editorial team prepared a proposal in slide 6 of https://www.ieee802.org/3/dj/public/24_06/ran_3dj_01a_2406.pdf.

Comments #227, #219 and #220 are about host ERL. In this case the existing specification of Tfx is suitable, although subtracting less than 0.2 ns may be appropriate in some cases. There was no consensus on how this should be specified.

Comments #218 and #221 are about module and cable assembly ERL. In this case the proposal may result in ambiguity in the definition of ERL. There was no consensus on making a change.

Additional study of this parameter and consensus building is encouraged.

Cl **179** *SC* **179.9.4.8** *P* **315** *L* **41** # 48

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *ERL*

scale ERL parameter form 0.3ck

SuggestedRemedy

in table 163-7 change TBD's as follows
Tr 0.005 ns
■x 0 GHz
?x 0.618
N 1600 UI

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

It is assumed that, based on the subclause/page/line, the suggested remedy is asking to change Table 179-9.

Resolve using the response to comment #29.

Cl **179** *SC* **179.9.5.3** *P* **319** *L* **22** # 411

Li, Tobey — MediaTek

Comment Type **TR** *Comment Status* **A** *COM*

COM values in Table 179û11 are TBD

SuggestedRemedy

Replace TBD with 3 dB

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #250.

Cl **179** *SC* **179.9.5.3** *P* **319** *L* **22** # 49

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *COM*

The COM values need to be set to make progress. Until a more comprehensive proposal is presented use what is in 0.3ck and many other prior standards

SuggestedRemedy

set COM to 3 dB

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #250.

Cl **179** *SC* **179.9.5.3.3** *P* **320** *L* **18** # 412

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *B-T filter BW*

4th order Bessel-Thomson filter BW is TBD

SuggestedRemedy

Replace TBD with 62 GHz

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #60.

Cl **179** *SC* **179.9.5.5** *P* **324** *L* **5** # 219

Noujeim, Leesa Google

Comment Type **T** *Comment Status* **R** *ERL Tfx*

Practical test fixtures may have discontinuities close to 0.2ns from the host-facing connection (mating interface). If the intent is to remove the test fixture discontinuities from the ERL calculations, we should adjust the 0.2ns

SuggestedRemedy

Change text to "...Tfx equal to twice the delay between the test fixture connector and the test fixture host -facing connection minus 0.2ns or as needed to remove test-fixture discontinuities from the ERL result"

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #227.

Cl **179** *SC* **179.11** *P* **326** *L* **21** # 50

Mellitz, Richard Samtec

Comment Type **TR** *Comment Status* **A** *COM*

The COM values need to be set to make progress. Until a more comprehensive proposal is presented use what is in 0.3ck and many other prior standards

SuggestedRemedy

set COM to 3 dB

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #250.

Cl **179** *SC* **179.11** *P* **326** *L* **21** # 413

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM*

Minimum COM is TBD

SuggestedRemedy

Replace TBD with 3 dB in Table 179û13 and in line 41 of page 330

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #250.

Cl **179** *SC* **179.11.1** *P* **326** *L* **27** # 216

Noujeim, Leesa Google

Comment Type **T** *Comment Status* **A** *Nominal impedance (bucket)*

There is no test method or definition for the nominal characteristic impedance of the cable assembly. The components (eg paddle card, twinax) within a cable assembly may have different nominal characteristic impedances. There is no need to specify the nominal characteristic impedance of the cable assembly, since the performance of the cable assembly is determined by cl 179.11.2-7.

SuggestedRemedy

Remove "The nominal characteristic impedance of the cable assembly is 100 ohms"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
It is important to define the reference impedance for return loss specifications etc., but as the comment correctly suggests, there is no need to specify a nominal value.
Implement the suggested remedy.

Cl **179** *SC* **179.11.1** *P* **326** *L* **27** # 516

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **A** *Nominal impedance (bucket)*

"Nominal impedance" is something for a datasheet not a spec. If someone wants to build a cable assembly with 95 ohm bulk cable and it passes the spec - that's OK.

SuggestedRemedy

Delete "The nominal differential characteristic impedance of the cable assembly is 100 [ohm]". Move the one remaining sentence into 179.11.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #216.

Cl **179** SC **179.11.1** P **326** L **27** # 389

Kocsis, Sam — Amphenol

Comment Type **T** *Comment Status* **A** *Nominal impedance (bucket)*

Nominal characteristic impedance of the cable assembly is "100-ohm"

SuggestedRemedy

Contributions to the task force have demonstrated the nominal characteristic impedance of the cable assembly is ~92-ohm

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
It is understood that the suggested remedy is to change the nominal impedance from 100 to 92 Ohm.
However, as noted in comment #216, there is no need to specify a nominal impedance.
Resolve with using the response to comment #216.

Cl **179** SC **179.11.2** P **326** L **42** # 217

Noujeim, Leesa — Google

Comment Type **T** *Comment Status* **A** *B-T filter BW*

The maximum frequency of 40GHz is is insufficient for 200Gbps/lane PAM4

SuggestedRemedy

Increase to 65GHz, consistent with test equipment capabilities and demonstrated channel rolloff eg in https://www.ieee802.org/3/dj/public/23_11/weaver_3dj_01_2311.pdf and https://www.ieee802.org/3/dj/public/24_01/benartsi_3dj_01_2401.pdf OR change to TBD

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The value 40 GHz is a leftover from an older clause and has not been adopted.
Resolve using the response to comment #60.

Cl **179** SC **179.11.3** P **327** L **31** # 218

Noujeim, Leesa — Google

Comment Type **T** *Comment Status* **R** *ERL Tfx*

Practical test fixtures may have discontinuities close to 0.2ns from the host-facing connection (mating interface). If the intent is to remove the test fixture discontinuities from the ERL calculations, we should adjust the 0.2ns

SuggestedRemedy

Change text to "...Tfx equal to twice the delay between the test fixture connector and the test fixture host -facing connection minus 0.2ns or as needed to remove test-fixture discontinuities from the ERL result"

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #227.

Cl **179** SC **179.11.3** P **327** L **41** # 51

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *ERL*

The data rate was doubled and cable length was scale by a factor of 2 from .3ck. Adjust ERL parameters accordingly

SuggestedRemedy

in table 179-14 change TBD's as follows
Tr 0.005 ns
■x 0 GHz
?x 0.618
N 4500 UI

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #29.

Cl **179** SC **179.11.7** P **331** L **18** # 120

Sakai, Toshiaki — Socionext

Comment Type **T** *Comment Status* **A** *COM pkg tau (bucket)*

COM reference package parameter vlaue. (transmission line parameter tau)
In "Table 179û15" class A package model Transmission line parameter t(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, (llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

SuggestedRemedy

Change t(tau) value in Table 179-15 (class A package) from 6.141e-4 ns/mm to 6.141e-3 ns/mm.
Or simply delete this row, as the t(tau) value in table 93A-3 is 6.141e-3 ns/mm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #118.

Cl **179** *SC* **179.11.7** *P* **331** *L* **28** # 121

Sakai, Toshiaki — Socionext

Comment Type **T** *Comment Status* **A** *COM pkg tau (bucket)*

COM reference package parameter vlaue. (transmission line parameter tau)
In "Table 179û15" class B package model Transmission line parameter t(tau) value is 6.141e-4 ns/mm, but based on the adopted motion#10, Nov/2024, (llim_3dj_01a_2311.pdf (page8-9), the value is 6.141e-3. The value should be 6.141e-3 ns/mm.

SuggestedRemedy

Change t(tau) value in Table 179-15 (class B package) from 6.141e-4 ns/mm to 6.141e-3 ns/mm.
Or simply delete this row, as the t(tau) value in table 93A-3 is 6.141e-3 ns/mm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #118.

Cl **179** *SC* **179.11.7** *P* **331** *L* **42** # 414

Li, Tobey — MediaTek

Comment Type **T** *Comment Status* **A** *R_0*

Single-ended reference resistance R0 value in Table 179û15 is TBD

SuggestedRemedy

Replace TBD with 50 Ohm

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #403.

Cl **179** *SC* **179.11.7** *P* **331** *L* **43** # 52

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *R_0*

(Table 179û15): Computation can be independent of R0. Add a note to explain. S parameter can utilize any R0. For computation purposes s-parameters are converted to 50 ohms which is the native impedance for the most common test equipment.

SuggestedRemedy

Change R0 for TBD to 50 ohms and add a note indicating the imported s-parameter are to be converted into 50 ohm reference before computation.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolve using the response to comment #35.

Cl **179** *SC* **179.11.7** *P* **331** *L* **44** # 391

Kocsis, Sam — Amphenol

Comment Type **T** *Comment Status* **A** *COM R_d*

Rd(t) = "TBD"

SuggestedRemedy

Change "TBD" to "92-ohm" to match majority of contributions to the Task Force, and better align with Zc definition in package

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #396.

Cl **179** *SC* **179.11.7** *P* **331** *L* **45** # 392

Kocsis, Sam — Amphenol

Comment Type **T** *Comment Status* **A** *COM R_d*

RD(r) = "TBD"

SuggestedRemedy

Change "TBD" to "92-ohm" to match majority of contributions to the Task Force, and better align with Zc definition in package

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #396.

Cl **179** *SC* **179.11.7** *P* **332** *L* **12** # 53

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *COM f_r*

T(able 179û16) Presentations so far have used fr of 0.5, 0.55, 0.58, and 0.6. 67 Ghz limits on test equipment and cabling/connector modal physics suggest at least a 9 dB loss is required for good measurements at 67 GHz. Set fr to 0.6 or lower to achieve this.

SuggestedRemedy

change TBD to 0.6.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #36.

Cl **179** *SC* **179.11.7** *P* **332** *L* **12** # 415

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM f_r*

Receiver 3 dB bandwidth fr value in Table 179û16 is TBD

SuggestedRemedy

Replace TBD with 0.58*fb

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #36.

Cl **179** *SC* **179.11.7** *P* **332** *L* **12** # 70

Lusted, Kent Intel Corporation

Comment Type **TR** *Comment Status* **R** *Multiple COM parameters*

The COM parameter values for the 200GBASE-CR1, 400GBASE-CR2, 800GBASE-CR4 and 1.6TBASE-CR8 PMDs are TBDs

SuggestedRemedy

In table 179-16, Use the COM parameter values from https://www.ieee802.org/3/dj/public/24_01/healey_3dj_01_2401.pdf slide 18, which are:

f_r = 0.58
c(-3) = 0
c(-2) = 0
c(-1) = 0
c(0) = 1
c(1) = 0
A_v = 0.413
A_fe = 0.413
A_ne = 0.45
eta_0 = 6e-9
SNR_TX = 33
sigma_RJ = 0.01
A_DD = 0.02
R_LM = 0.95
d_w = 5
Nfix = 10
N_g = 0
N_f = 0
N_max = 0
b_max(1) = 0.85
b_min(1) = 0

additionally, set MLSE = 0 (not enabled)

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **179** *SC* **179.11.7** *P* **332** *L* **13** # 416

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM TxFFE*

The max/min values and step size of transmitter equalizer in Table 179-16 need to match those in the Table 179û7 and thost in sub-clauses 179.9.4.1.4 & 179.9.4.1.5

SuggestedRemedy

On line 14 replace TBD with -0.06:0.02:0
On line 18 replace TBD with 0:0.02:0.12
On line 22 replace TBD with -0.34:0.02:0
On line 26 replace TBD with 0.5
On line 28 replace TBD with -0.2:0.02:0

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #37.

Cl **179** *SC* **179.11.7** *P* **332** *L* **46** # 417

Li, Tobey MediaTek

Comment Type **T** *Comment Status* **R** *COM voltage parameters*

Transmitter differential peak output voltage in Table 179û16 is TBD

SuggestedRemedy

Replace Av with 0.413 V
Replace Afe with 0.413 V
Replace Ane with 0.608 V

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #38.

Cl **179** *SC* **179.11.7** *P* **332** *L* **50** # 418

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **A** *COM T_r*

Transmitter transition time Tr value in Table 179û16 is TBD

SuggestedRemedy

Replace TBD with Tr = 4 ps

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #39.

Cl **179** *SC* **179.11.7** *P* **332** *L* **53** # 419

Li, Tobey MediaTek

Comment Type **TR** *Comment Status* **R** *COM eta0*

One sided noise spectral density in Table 179û16 is TBD

SuggestedRemedy

Replace TBD with 6e-9 V^2/GHz

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #269.

Cl **179** *SC* **179.11.7** *P* **333** *L* **11** # 54

Mellitz, Richard Samtec

Comment Type **TR** *Comment Status* **R** *Multiple COM parameters*

(table 179-16)Selecting values the "Receiver discrete-time equalizer parameters" are critical for making progress. Many presentations a have shown quite a variation. Select values based on what seems consistent or use straw ballot to determine.

SuggestedRemedy

use straw polls from the following
Dw 4, 6, or 8
Nfix 10, 15, 24
Ng 1, 2, 3
Nf 3, 4, 5
Nmax 40 60 120
Wmax(j)=1
Wmin(-1,0,1)=0. otherwise -0.5
bmax(1) = 0,5 0.75 0 85
bmin(1)= 0 -0,5 -0.75 -0 85

Response *Response Status* **C**

REJECT.
Resolve using the response to comment #42.

Cl **179A** *SC* **179A** *P* **664** *L* # 24

Liu, Cathy Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

Figure 179A-1 and figure 179A-2 are not showing completely in my PDF file

SuggestedRemedy

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **179A** SC **179A.2** P **662** L **6710** # 56

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *93B (bucket)*

Refence to a diagram with TP0d and TP5d is required

SuggestedRemedy

Add TP0d and TP5d to figure 93B-1 and table 93B-1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Annex 93B is irrelevant for CR.
Also, Annex 93B is not referenced anywhere in the draft, nor in previous backplane PMD clauses 163 and 137.
A diagram with the new test points exists in Figure 179-2 and can be referenced instead.
Add a reference in 179A.2 to Figure 179-2. Implement with editorial license.

Cl **179A** SC **179A.5** P **665** L **24** # 229

Noujeim, Leesa — Google

Comment Type **T** *Comment Status* **A** *Channel ILdd (bucket)*

Doubling ILdd_(host+TFmax) implies both ends of the link have the same host designations.

SuggestedRemedy

Replace "2*ILdd_(host+TFmax)" with "ILdd_(host+tFmax)_end1 + ILdd_(host+tFmax)_end2" or similar notation to accommodate asymmetric Link Configurations in Table 179A-3.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Replace "2*ILdd_(host+TFmax)" with "ILdd_(host+tFmax)_one end + ILdd_(host+tFmax)_other end" with editorial license to accommodate asymmetric Link Configurations in Table 179A-3.

Cl **179A** SC **179A.7** P **668** L **9** # 393

Kocsis, Sam — Amphenol

Comment Type **E** *Comment Status* **A** *(editorial)*

"TP0 and TP5"

SuggestedRemedy

Change to "TP0d and TP5d"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **179A** SC **179A.7** P **668** L **12** # 57

Mellitz, Richard — Samtec

Comment Type **TR** *Comment Status* **A** *COM*

The COM values need to be set to make progress. Until a more comprehensive proposal is presented use what is in 0.3ck and many other prior standards

SuggestedRemedy

set COM to 3 dB

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #250.

Cl **179B** SC **179B** P **670** L # 25

Liu, Cathy — Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

Figure 179B-1 figure is not showing completely in my PDF file

SuggestedRemedy

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **179B** SC **179B** P **672** L # 26

Liu, Cathy — Broadcom

Comment Type **E** *Comment Status* **A** *(editorial)*

Figure 179B-2 figure is not showing completely in my PDF file

SuggestedRemedy

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **179B** SC **179B.1** P **669** L **15** # 222

Noujeim, Leesa Google

Comment Type **T** *Comment Status* **A** *(bucket)*

Incorrect Annex reference 120G

SuggestedRemedy

Replace 120G with 176E

Response *Response Status* **C**

ACCEPT.

Cl **179B** SC **179B.1** P **669** L **17** # 223

Noujeim, Leesa Google

Comment Type **T** *Comment Status* **A** *HCB and MCB (bucket)*

Missing reference to Module compliance at TP1 and TP4

SuggestedRemedy

Add "Module measurements for Modules specified in Annex 176E are made at TP1 and TP4 with test fixtures as specified in 179B.3. "

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Insert the sentence:
Module measurements for modules specified in Annex 176E are made at module compliance points TP1 and TP4 (see Figure 176E-4) with test fixtures as specified in 179B.3.

Cl **179B** SC **179B.4.2** P **673** L **13** # 58

Mellitz, Richard Samtec

Comment Type **TR** *Comment Status* **A** *ERL*

scale ERL parameter form 0.3ck

SuggestedRemedy

in table 178-14 change TBD's as follows
Tr 0.005 ns
■x 0 GHz
?x 0.618
N 1600 UI
Tfx 0
tw 1
DER0 2e-5

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
It is assumed that, based on the subclause/page/line, the suggested remedy is asking to change Table 179B-1.
Resolve using the response to comment #29.

Cl **179B** SC **179B.4.6** P **676** L **26** # 224

Noujeim, Leesa Google

Comment Type **T** *Comment Status* **A** *HCB and MCB (bucket)*

SFPxxx is unclear

SuggestedRemedy

Replace "The SFPxxx mated test fixture" with "The single-lane mated test fixture"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In 179B replace SFPxxx with SFP112

Cl **179B** SC **179B.4.26** P **676** L **41** # 59

Mellitz, Richard Samtec

Comment Type **TR** *Comment Status* **A** *HCB and MCB (bucket)*

At least the symbol rate is known

SuggestedRemedy

set fb to 106.25 GBd

Response *Response Status* **C**

ACCEPT.

Cl **179C** *SC* **179C.1** *P* **680** *L* **15** # 525

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **A** *MDI references (bucket)*

MDIs are mechanical entities. For 106.25 GBd operation, there are SFP2 (SFF-TA-1031) and QSFP2 (SFF-TA-1027). Any "SFP224" would be an SFP2 module or cable end with 200G-capable circuitry. But this annex is for the MDI, not the circuitry. Similarly for "QSFP224" and QSFP2.

SuggestedRemedy

Correct the names. Add references to SFF-TA-1011 which relates the names and specs for the SNIA-SFF modules, and SFF-8665, which defines the components of a QSFPx "solution".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
There was broad consensus to use names of MDI types (part of baseline proposal) currently in the draft as follows: SFP224, SFP-DD224,QSFP224, QSFP-DD1600, OSFP1600.
Resolve using the response to comment #506, which addresses the normative references.

Cl **179C** *SC* **179C.1** *P* **680** *L* **17** # 526

Dawe, Piers Nvidia

Comment Type **TR** *Comment Status* **A** *MDI references (bucket)*

Refer to the specification for each connector type where each is first mentioned.
See another comment against 1.3 for the reference docs.

SuggestedRemedy

Per comment

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #506.

Cl **179C** *SC* **179C.1** *P* **682** *L* **38** # 394

Kocsis, Sam Amphenol

Comment Type **E** *Comment Status* **A** *(editorial)*

"QSFP-DD800"

SuggestedRemedy

Change to "QSFP-DD1600"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.
[Editor's note: Changed subclause to 179C.1]

Cl **179C** *SC* **179C.2.3** *P* **688** *L* **35** # 527

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **A** *MDI references (bucket)*

This says "the mechanical interface". The mechanical spec is SFF-TA-1027, QSFP2. It is a standard, not an MSA.

SuggestedRemedy

Change " the TBD MSA" to "SFF-TA-1027".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #506.

Cl **179C** *SC* **179C.2.4** *P* **689** *L* **35** # 528

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **A** *MDI references (bucket)*

There is no QSFP-DD1600 TBD MSA document. QSFP-DD1600 is defined in the singular QSFP-DD MSA document

SuggestedRemedy

Change "the QSFP-DD1600 TBD MSA" to "the QSFP-DD/QSFP-DD800/QSFP-DD1600 Hardware Specification".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #506.

Cl **179C** *SC* **179C.2.5** *P* **690** *L* **21** # 529

Dawe, Piers Nvidia

Comment Type **T** *Comment Status* **A** *MDI references (bucket)*

There is no OSFP1600 TBD MSA document. OSFP1600 is defined in the singular OSFP MSA document, particularly section 4.

SuggestedRemedy

Change "the OSFP1600 TBD MSA" to "the OSFP Octal Small Form Factor Pluggable Module specification" or "section 4 of the OSFP Octal Small Form Factor Pluggable Module specification".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #506.

Cl **180** *SC* **180.4** *P* **349** *L* **10** # 146

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *Precoding*

Prior to 180.4 add section for PMA function to support precoder to mitigate burst errors

SuggestedRemedy

The transmitter need to supports 1/(1+D) mod 4 precoding, as specified in 135.5.7.2, 120.5.7.2, and 173.5.7.2, 6 and 176.9.1.2, that may be enabled or disabled as needed with OLT, without OLT the optical transmitter should enable 1/(1+D) mod 4 precoding to mitigate burst error.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #21

Cl **180** *SC* **180.4.1** *P* **350** *L* **13** # 160

Yu, Rang-chen — InnoLight

Comment Type **ER** *Comment Status* **A** *Editorial (bucket)*

A typo of 'L3' in figure 180-2, right side, 3rd channel output label.

SuggestedRemedy

It should be 'L2'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **180** *SC* **180.6.1** *P* **353** *L* **33** # 326

Welch, Brian — Cisco

Comment Type **TR** *Comment Status* **A** *TX specs*

In later 100GPL specs (ie, 100GBASE-FR1) the difference between OMA(min) and Pave(min) was 3dB, to reflect the case of infinite extinction ratio. In the adopted baselines this narrowed to 2.5 dB as it was not updated to reflect the changes to effective TDECQ(min).

SuggestedRemedy

Propose changing "Average launch power, each lane (min)" in Table 180-7 from -2.8 dBm to -3.3 dBm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change "Average launch power, each lane (min)" in Table 180-7 from -2.8 dBm to -3.3 dBm.

In Table 180-7, add a footnote to the value "-3.3" on the row for "Average launch power, each lane (min)" with the following text:
"Average launch power of -3.3 dBm corresponds to an OMA of -0.3 dBm with an infinite extinction ratio."

Implement with editorial license.

Cl **180** *SC* **180.6.2** *P* **354** *L* **35** # 517

Dawe, Piers — Nvidia

Comment Type **T** *Comment Status* **A** *RX specs*

In 802.3db we acknowledged that single-lane PMDs are often packaged in multilane modules, and subject to much the same crosstalk as multilane PMDs.

SuggestedRemedy

Delete footnote e, "No aggressors needed for 200GBASE-DR1." In 180.8.13 Stressed receiver sensitivity, add "For a receiver in a multilane device, the OMA outer of the aggressor lanes is specified in Table 180-8."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change footnote e, to "No aggressors needed for 200GBASE-DR1 in a single lane device."

With editorial license.

Cl **180** *SC* **180.6.3** *P* **356** *L* **47** # 170

Yu, Rang-chen InnoLight

Comment Type **T** *Comment Status* **A** *power budget*

Footnote b did not clarify what's the compisiton of total 3.5dB allocation for penalties.

SuggestedRemedy

Recommend to add "Allocations to penalties for DRx series including penalties due to dipersion 3.4dB, DGD and MPI 0.1dB" to footnote b.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #127.

Cl **180** *SC* **180.6.3** *P* **356** *L* **47** # 127

Johnson, John Broadcom

Comment Type **T** *Comment Status* **A** *power budget*

The power budget does not explicitly say what the penalty allocation is for MPI and DGD. It's implied by the difference between Allocation for penalties (for max TDECQ) and TDECQ(max). This makes it hard for average readers to understand the power budget.

SuggestedRemedy

Add toTable 180-9, footnote (b), "This value includes an allocation of 0.1 dB for MPI and DGD penalties."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **180** *SC* **180.7.1** *P* **358** *L* **28** # 335

Ferretti, Vince Corning

Comment Type **TR** *Comment Status* **R** *optical channel specs*

ITU-T G.652.B cabled fiber attenuation is only specified for 1310 nm and 1550 nm wavelengths. It is not specified for wavelengths between 1260 nm and 1310 nm and not meant to be used in xWDM applications

SuggestedRemedy

Remove ITU-T G.652.B (dispersion unshifted) as a fiber option.

Response *Response Status* **C**

REJECT.

There is no xWDM in this PMD clause.

Cl **180** *SC* **180.7.3.1.1** *P* **360** *L* **11** # 590

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *Connector labeling*

To support breakout, loopback, and OAN/OLT connectro should be labled

SuggestedRemedy

DR2-2 connector should be labled as Tx1Tx2 ------ Rx2Rx1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

While the labeling modification as proposed was not part of the adopted Baseline Proposal for Optical Link Training "OLT", it is necessary to support the adopted baseline.

Implement suggested remedy with editorial license.

Cl **180** *SC* **180.7.3.1.2** *P* **260** *L* **27** # 591

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *Connector labeling*

To support breakout, loopback, and OAN/OLT connectro should be labled

SuggestedRemedy

DR2-4 connector should be labled as Tx1Tx2Tx3Tx4 ------ Rx4Rx3Rx2Rx1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #590.

Cl **180** *SC* **180.7.3.1.3** *P* **361** *L* **46** # 592

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *Connector labeling*

To support breakout, loopback, and OAN/OLT connectro should be labled

SuggestedRemedy

DR2-8 connector should be labled as Tx1Tx2Tx3Tx4Tx5Tx6Tx7Tx8
Rx8Rx7Rx6Rx5Rx4Rx3Rx2Rx1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #590.

Cl **180** *SC* **180.7.3.2** *P* **361** *L* **9** # 338

Lambert, Angie — Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-1-1 has been superseded by IEC 61753-1.

SuggestedRemedy

Change "IEC 61753-1-1" to "IEC 61753-1"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change "IEC 61753-1-1" to "IEC 61753-1" in the PMD clause.

Add "IEC 61753-1, Fibre optic interconnecting devices and passive components - Performance standard - Part 1: General and guidance" to 1.3 Normative references.

With editorial license.

Cl **180** *SC* **180.7.3.2** *P* **361** *L* **9** # 339

Lambert, Angie — Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change "IEC 61753-021-2" to "IEC 61753-021-02" in the PMD clause.

Add "IEC 61753-021-02, Fibre optic interconnecting devices and passive components - Performance standard - Part 021-02: Single-mode fibre optic connectors terminated as pigtails and patchcords for category C - Controlled environment" to 1.3 Normative references.

With editorial license.

Cl **180** *SC* **180.7.3.3** *P* **361** *L* **42** # 340

Lambert, Angie — Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #339.

Cl **180** *SC* **180.7.3.4** *P* **361** *L* **50** # 341

Lambert, Angie — Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #339.

Cl **180** *SC* **180.8.5** *P* **364** *L* **23** # 1

Johnson, John — Broadcom

Comment Type **T** *Comment Status* **A** *TDECQ*

121.8.5.2 Table 121-11 specifies ORL of 21.4dB be applied for TX testing. For 200GBASE-DR1, this needs to be 15.1dB.

SuggestedRemedy

Add a new exception to the list in 180.8.5:
"- The optical return loss is as given in Table 180-6."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Add a new exception to the list in 180.8.5:
"- The optical return loss is as given in Table 180-7."

Implement with editorial license.

Cl **180** *SC* **180.8.5** *P* **364** *L* **23** # 17

LeCheminant, Greg — Keysight Technologies

Comment Type **T** *Comment Status* **A** *TDECQ*

The current method for optimizing the tap weighs of equalizer in the TDECQ reference receiver is described in clause 121.8.5. The equalizer tap coefficients are iteratively adjusted to effectively minimize the TDECQ penalty. Although not explicitly stated, one way to view this is that ANY combination of tap weights is valid and that ALL combinations should be tried to ensure the optimum tap weight combination is used when calculating TDECQ. As the equalizer length has been increased from 5 taps to 15 taps, the time required to verify all possible tap weights is likely problematic. This issue was managed in the 802.3 db project, where a 9 tap virtual equalizer is used for TDECQ. The following text was added to clause the definition of the TDECQ method: ôThe lowest measured TDECQ values are achieved with the equalizer optimization method described in 121.8.5. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time, and are expected to report equal or higher values of TDECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibrationö. Note that the MMSE optimization method is used in almost all TDECQ measurements performed today

SuggestedRemedy

Add the following text at line 36 (end of exceptions list):

The lowest measured TDECQ values are achieved with the equalizer optimization method described in 121.8.5. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time, and are expected to report equal or higher values of TDECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibration

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement the suggested remedy with editorial license.

Cl **180** *SC* **180.8.5** *P* **364** *L* **39** # 324

Welch, Brian — Cisco

Comment Type **TR** *Comment Status* **A** *TDECQ*

Current baseline proposal is lacking tap weight restrictions, which were indicated as TBD when adopted.

SuggestedRemedy

Propose adopting the TDECQ tap weight restrictions as presented in welch_3dj_01_0524.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The following presentation was reviewed by the 802.3dj task force at the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/welch_3dj_01_2405.pdf.

Implement slide 7 of the presentation with editorial license with the following exceptions:

n = -1 and n = 1 being TBD for the min values.

Cl **180** *SC* **180.8.11** *P* **365** *L* **51** # 518

Dawe, Piers — Nvidia

Comment Type **T** *Comment Status* **A** *RIN-OMA*

"The upper -3 dB limit of the measurement apparatus is to be approximately equal to the signaling rate": I believe this dates back at least to the first Fibre Channel, ~1 Gb/s, long before adaptive equalisers that optimise the receiver bandwidth. We have a RIN spec to help the accuracy of the TDECQ spec, which is the actual assessment of signal quality. Gigabit Ethernet now uses 937.5 MHz, 75% of the signalling rate. Measuring a peaky noise spectrum in too much bandwidth gives a flattering average, which is not what we want.

SuggestedRemedy

Change the bandwidth for RIN measurement to be the same as the TDECQ receiver's BT4 filter (50% of signalling rate ~ 53.1 GHz) or 75%, or something in between.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The following presentation was reviewed by the 802.3dj task force at the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/johnson_3dj_03a_2405.pdf

Implement slides 8 and 9 of the presentation with editorial license.

Cl **180** *SC* **180.8.11** *P* **365** *L* **52** # 13

LeCheminant, Greg — Keysight Technologies

Comment Type **T** *Comment Status* **A** *RIN-OMA*

The required -3dB BW for the measurement system is not achievable with existing technology. (State of the art power meters with a maximum 120 GHz bandwidth, would require the bandwidth of the photodetetor to be substaitially higher than 120 GHz to achieve the current system bandiwdth required for the test system, as defined in clause 52)

SuggestedRemedy

The bandiwdth of the RIN-OMA test system should be based on the expected bandwidth of the system receivers and consider the expected noise spectrum of transmitters. Spec limits for RIN OMA may need adjustment to adapt to any changes in the test method

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #518

Cl **180** *SC* **180.8.13** *P* **366** *L* **25** # 519

Dawe, Piers — Nvidia

Comment Type **T** *Comment Status* **R** *Jitter (common)*

More exceptions - I found these in 167.8.14

SuggestedRemedy

The applied sinusoidal jitter is specified in 180.8.13.1.
The values of overshoot/undershoot and transmitter power excursion of the stressed receiver conformance signal are within the limits specified in Table 180-7.
For a receiver in a multilane device, the OMA outer of the aggressor lanes is specified in Table 180-8.

Add a sinusoidal jitter section following 167.8.14.1 (but see next comment).

Response *Response Status* **C**

REJECT.

The comment does not provide sufficient justification to support the suggested remedy.

Cl **180** *SC* **180.8.13** *P* **366** *L* **26** # 520

Dawe, Piers — Nvidia

Comment Type **T** *Comment Status* **R** *Jitter (common)*

If the rising LF jitter slope for 113.4375 GBd is based on 4 MHz, 0.05 UI pk-pk, the LF jitter slope for 106.25 GBd must match in absolute time units (not UI) so that there is not an unbounded buffering requirement (or one jitter slope can be modified in shape).

SuggestedRemedy

In the FECi clauses, instead of 2e5/f, 0.05 UI, use 2.13e5/f, 0.053 UI. Or, here and in the other non-FECi PMD and PMA clauses, use 1.875e5/f, 0.047 UI.

Response *Response Status* **C**

REJECT.

The justification provided by the comment is not sufficient to make the proposed changes. A detailed presentation providingbetter justification is encouraged.

Cl **180** *SC* **180.9.1** *P* **366** *L* **31** # 342

Lambert, Angie — Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 60950-1 has been superseded by IEC 62368-1.

SuggestedRemedy

Change "IEC 60950-1" to "IEC 63268-1".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change "IEC 60950-1" to "IEC 62368-1" in the PMD clause.

Cl **180** *SC* **180.10** *P* **368** *L* **11** # 521

Dawe, Piers — Nvidia

Comment Type **T** *Comment Status* **A** *bit number (bucket)*

Bit number should match number of lanes

SuggestedRemedy

Change 1.9.4 to 1.9.n. Below, change 1.10.4 to 1.10.n. Similarly in other clauses.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **181** *SC* **181.1** *P* **372** *L* **16** # 4

Johnson, John Broadcom

Comment Type **T** *Comment Status* **A** *Editorial (bucket)*

The PHY bracket in Figure 181-1 is shown encompassing the MDI layer, which isn't consistent with previous PMDs.

SuggestedRemedy

Shorten the PHY bracket to exclude the MDI layer.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **181** *SC* **181.4** *P* **373** *L* **33** # 145

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *Precoding*

Prior to 181.4 add section for PMA function to support precoder to mitigate burst errors

SuggestedRemedy

The transmitter need to supports 1/(1+D) mod 4 precoding, as specified in 135.5.7.2, 120.5.7.2, and 173.5.7.2, 6 and 176.9.1.2, that may be enabled or disabled as needed with OLT, without OLT the optical transmitter should enable 1/(1+D) mod 4 precoding to mitigate burst error.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #21

Cl **181** *SC* **181.6.1** *P* **378** *L* **13** # 6

Johnson, John Broadcom

Comment Type **T** *Comment Status* **A** *TX specs*

Total average launch power (max) in Table 181-5 is TBD for 800GBASE-FR4-500.

SuggestedRemedy

Replace TBD with a value equal to the Average launch power, each lane (max) + 6 dB, which is 4.9 + 6 = 10.9 dB. This methodology is consistent with previous FR4 PMDs (clauses 122, 151).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **181** *SC* **181.6.1** *P* **378** *L* **16** # 162

Yu, Rang-chen InnoLight

Comment Type **TR** *Comment Status* **A** *TX specs*

recommend relationship between 'Tx_OMAout (min)' and 'Tx_Pavg (min)' (in Table 181ũ5) follow 400G FR4, with delta=3dB, assuming max. OER infinite.

SuggestedRemedy

With 'OMAout (min)'=0.8dBm, then 'Average launch power, each lane (min) ' in Table 181-5 should be changed to -2.2dBm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In Table 181-5 change "Average launch power, each lane (min)" from -1.8 to -2.2

In Table 181-5, add a footnote to the value "-2.2" on the row for "Average launch power, each lane (min)" with the following text:
"Average launch power of -2.2 dBm corresponds to an OMA of 0.8 dBm with an infinite extinction ratio."

With editorial license.

Cl **181** *SC* **181.6.1** *P* **378** *L* **16** # 327

Welch, Brian Cisco

Comment Type **TR** *Comment Status* **A** *TX specs*

In later 100GPL specs (ie, 400GBASE-FR4) the difference between OMA(min) and Pave(min) was 3dB, to reflect the case of infinite extinction ratio. In the adopted baselines this narrowed to 2.6 dB as it was not updated to reflect the changes to effective TDECQ(min).

SuggestedRemedy

Propose changing "Average launch power, each lane (min)" in Table 181-5 from -1.8 dBm to -2.2 dBm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #162

Cl **181** *SC* **181.6.1** *P* **378** *L* **23** # 8

Johnson, John Broadcom

Comment Type **T** *Comment Status* **A** *TX specs*

Difference in launch power between any two lanes (OMAouter) (max) in Table 181-5 is TBD for 800GBASE-FR4-500.

SuggestedRemedy

Replace TBD with a value of OMAouter(max) minus OMAouter(min) or 4 dB, whicher is smaller, consistent with other FRn/LRn clauses (122, 151).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **181** *SC* **181.6.2** *P* **380** *L* **18** # 163

Yu, Rang-chen InnoLight

Comment Type **TR** *Comment Status* **A** *RX specs*

The delta between 'Tx_Pavg(min)' and 'Rx_Pavg(min)' should equal to 'Channel insertion loss' (3.5dB for FR4-500)

SuggestedRemedy

Rx_Pavg (min)' in Table 181û6 should be -2.2dBm-3.5dB=-5.7dBm

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In Table 181-6, change the value for "Average receive power, each lane (min)" to -5.7.

Cl **181** *SC* **181.6.2** *P* **380** *L* **21** # 10

Johnson, John Broadcom

Comment Type **T** *Comment Status* **A** *RX specs*

Difference in receive power between any two lanes (OMAouter) (max) in Table 181-6 is TBD for 800GBASE-FR4-500.

SuggestedRemedy

Replace TBD with a value of 4.1 dB, consistent with other FR4 PMDs (Cl. 122, 151)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **181** *SC* **181.6.3** *P* **381** *L* **36** # 161

Yu, Rang-chen InnoLight

Comment Type **TR** *Comment Status* **A** *power budget*

Power budget (for maximum TDECQ)' for 800GBASE-FR4-500 in Table 181-7 could be incorrect. It should be equal to channel IL + allocation for penalties (for maximum TDECQ).

SuggestedRemedy

Power budget (for maximum TDECQ)' in Table 181-7 should be updated to 7.4 dB

Response *Response Status* **C**

ACCEPT.

Cl **181** *SC* **181.6.3** *P* **381** *L* **48** # 169

Yu, Rang-chen InnoLight

Comment Type **T** *Comment Status* **A** *power budget*

Footnote d did not clarify what's the compisiton of total 3.9dB allocation for penalties.

SuggestedRemedy

Recommend to add "Allocations to penalties for 800G-FR4-500 including penalties due to dipersion 3.4dB, DGD and MPI 0.5dB" to footnote d.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #128

Cl **181** *SC* **181.6.3** *P* **381** *L* **48** # 128

Johnson, John Broadcom

Comment Type **T** *Comment Status* **A** *power budget*

The power budget does not explicitly say what the penalty allocation is for MPI and DGD. It's implied by the difference between Allocation for penalties (for max TDECQ) and TDECQ(max). This makes it hard for average readers to understand the power budget.

SuggestedRemedy

Add toTable 181-7, footnote (d), "This value includes an allocation of 0.5 dB for MPI and DGD penalties."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **181** *SC* **181.7** *P* **383** *L* **16** # 173

Yu, Rang-chen InnoLight

Comment Type **T** *Comment Status* **A** *power budget*

DGDmax (in Table 181û8) probably used DGDmean=0.8ps, it should be 2.24ps refer to 802.3df DR series.

SuggestedRemedy

Recommend change to 2.24ps

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement proposed remedy with editorial license.

Cl **181** *SC* **181.7.1** *P* **383** *L* **26** # 336

Ferretti, Vince Corning

Comment Type **TR** *Comment Status* **A** *optical channel specs*

ITU-T G.652.B cabled fiber attenuation is only specified for 1310 nm and 1550 nm wavelengths. It is not specified for wavelengths between 1260 nm and 1310 nm and not meant to be used in xWDM applications

SuggestedRemedy

Remove ITU-T G.652.B (dispersion unshifted) as a fiber option.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement suggested remedy.

Implement the same change in clause 183.7.1.

With editorial license

Cl **181** *SC* **181.7.3** *P* **384** *L* **43** # 343

Lambert, Angie Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #339.

Cl **181** *SC* **181.8.5** *P* **386** *L* **41** # 18

LeCheminant, Greg Keysight Technologies

Comment Type **T** *Comment Status* **A** *TDECQ*

The current method for optimizing the tap weighs of equalizer in the TDECQ reference receiver is described in clause 121.8.5. The equalizer tap coefficients are iteratively adjusted to effectively minimize the TDECQ penalty. Although not explicitly stated, one way to view this is that ANY combination of tap weights is valid and that ALL combinations should be tried to ensure the optimum tap weight combination is used when calculating TDECQ. As the equalizer length has been increased from 5 taps to 15 taps, the time required to verify all possible tap weights is likely problematic. This issue was managed in the 802.3 db project, where a 9 tap virtual equalizer is used for TDECQ. The following text was added to clause the definition of the TDECQ method: ôThe lowest measured TDECQ values are achieved with the equalizer optimization method described in 121.8.5. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time, and are expected to report equal or higher values of TDECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibrationö. Note that the MMSE optimization method is used in almost all TDECQ measurements performed today

SuggestedRemedy

Add the following text at line 53 (end of exceptions list): The lowest measured TDECQ values are achieved with the equalizer optimization method described in 121.8.5. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time, and are expected to report equal or higher values of TDECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibration

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #17

Cl **181** *SC* **181.8.5** *P* **386** *L* **41** # 2

Johnson, John Broadcom

Comment Type **T** *Comment Status* **A** *Reference (bucket)*

The TDECQ methods reference channel requirements in 121.8.5.2 instead of the channel requirements in local clause 181.8.5.1.

SuggestedRemedy

Replace the reference to 121.8.5.2 with reference to 181.8.5.1.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **181** *SC* **181.8.5** *P* **387** *L* **3** # 325

Welch, Brian Cisco

Comment Type **TR** *Comment Status* **A** *TDECQ*

Current baseline proposal is lacking tap weight restrictions, which were indicated as TBD when adopted.

SuggestedRemedy

Propose adopting the TDECQ tap weight restrictions as presented in welch_3dj_01_0524.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolve using the response to comment #324.

Cl **181** *SC* **181.8.5.1** *P* **387** *L* **19** # 207

Parsons, Earl CommScope

Comment Type **T** *Comment Status* **A** *optical channel specs*

The maximum and minimum dispersion values in this table should be replaced by equations similar to ones found in previous clauses (i.e. Table 151-12). This method is sometimes called "CM1".

SuggestedRemedy

In the minimum column replace "-2.94" with "0.0115 x ? x [1-(1324/?)^4]". In the maximum column replace "1.66" with "0.0115 x ? x [1-(1300/?)^4]". These are the same values as in Table 151-12 with the coefficient divided by 4.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement suggested remedy with editorial license.

Note that "?" in the suggested remedy is the lambda symbol.

Cl **181** *SC* **181.8.11** *P* **388** *L* **52** # 14

LeCheminant, Greg Keysight Technologies

Comment Type **T** *Comment Status* **A** *RIN-OMA*

The required -3dB BW for the measurement system is not achievable with existing technology. (State of the art power meters with a maximum 120 GHz bandwidth, would require the bandwidth of the photodetetor to be substaitially higher than 120 GHz to achieve the current system bandiwdth required for the test system, as defined in clause 52)

SuggestedRemedy

The bandiwdth of the RIN-OMA test system should be based on the expected bandwidth of the system receivers and consider the expected noise spectrum of transmitters. Spec limits for RIN OMA may need adjustment to adapt to any changes in the test method

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #518

Cl **182** *SC* **182.1** *P* **392** *L* **44** # 301

Maki, Jeffery Juniper Networks

Comment Type **TR** *Comment Status* **A** *IMDD acronym (bucket)*

Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of "Coherent" to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.

SuggestedRemedy

Delete the acronym IMDD.

Response *Response Status* **C**

ACCEPT.

Cl **182** *SC* **182.1** *P* **393** *L* **29** # 302

Maki, Jeffery Juniper Networks

Comment Type **TR** *Comment Status* **A** *IMDD acronym (bucket)*

Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of "Coherent" to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.

SuggestedRemedy

Delete the acronym IMDD.

Response *Response Status* **C**

ACCEPT.

Cl **182** *SC* **182.1** *P* **394** *L* **23** # 303

Maki, Jeffery — Juniper Networks

Comment Type **TR** *Comment Status* **A** *IMDD acronym (bucket)*

Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of "Coherent" to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.

SuggestedRemedy

Delete the acronym IMDD.

Response *Response Status* **C**

ACCEPT.

Cl **182** *SC* **182.1** *P* **394** *L* **50** # 304

Maki, Jeffery — Juniper Networks

Comment Type **TR** *Comment Status* **A** *IMDD acronym (bucket)*

Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of "Coherent" to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.

SuggestedRemedy

Delete the acronym IMDD.

Response *Response Status* **C**

ACCEPT.

Cl **182** *SC* **182.1** *P* **395** *L* **21** # 5

Johnson, John — Broadcom

Comment Type **T** *Comment Status* **A** *Editorial (bucket)*

The PHY bracket in Figure 182-1 does not encompass the PMD layer, which isn't consistent with previous PMDs.

SuggestedRemedy

Lengthen the PHY bracket to include the PMD layer.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **182** *SC* **182.4** *P* **397** *L* **20** # 147

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *Precoding*

Prior to 182.4 add section for PMA function to support precoder to mitigate burst errors

SuggestedRemedy

The transmitter need to supports 1/(1+D) mod 4 precoding, as specified in 135.5.7.2, 120.5.7.2, and 173.5.7.2, 6 and 176.9.1.2, that may be enabled or disabled as needed with OLT, without OLT the optical transmitter should enable 1/(1+D) mod 4 precoding to mitigate burst error.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using response to comment #547.

Cl **182** *SC* **182.6.1** *P* **401** *L* **21** # 328

Welch, Brian — Cisco

Comment Type **TR** *Comment Status* **A** *TX specs*

In later 100GPL specs (ie, 100GBASE-FR1) the difference between OMA(min) and Pave(min) was 3dB, to reflect the case of infinite extinction ratio. In the adopted baselines this narrowed to 2.5 dB as it was not updated to reflect the changes to effective TDECQ(min).

SuggestedRemedy

Propose changing "Average launch power, each lane (min)" in Table 182-7 from -2.1 dBm to -2.6 dBm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change "Average launch power, each lane (min)" in Table 182-7 from -2.1 dBm to -2.6 dBm.

In Table 182-7, add a footnote to the value "-2.6" on the row for "Average launch power, each lane (min)" with the following text:
"Average launch power of -2.6 dBm corresponds to an OMA of 0.4 dBm with an infinite extinction ratio."

Implement with editorial license.

Cl **182** *SC* **182.6.3** *P* **404** *L* **3** # 171

Yu, Rang-chen InnoLight

Comment Type **T** *Comment Status* **A** *power budget*

Although TDECQmax is still TBD. However, the footnote b should also indicate the allocation for penalties, just leave dispersion section as TBD for future update.

SuggestedRemedy

Recommend to add "Allocations to penalties for DRx-2 series including penalties due to dipersion TBDdB, DGD and MPI 0.4dB" to footnote b.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Resolve using the response to comment #128 with the exception that the value is 0.4dB and not 0.5dB.
Implement with editorial license.

Cl **182** *SC* **182.7.1** *P* **405** *L* **31** # 337

Ferretti, Vince Corning

Comment Type **TR** *Comment Status* **R** *optical channel specs*

ITU-T G.652.B cabled fiber attenuation is only specified for 1310 nm and 1550 nm wavelengths. It is not specified for wavelengths between 1260 nm and 1310 nm and not meant to be used in xWDM applications

SuggestedRemedy

Remove ITU-T G.652.B (dispersion unshifted) as a fiber option.

Response *Response Status* **C**

REJECT.

There is no xWDM in this PMD clause.

Cl **182** *SC* **182.7.3** *P* **406** *L* **45** # 344

Lambert, Angie Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-1-1 has been superseded by IEC 61753-1.

SuggestedRemedy

Change "IEC 61753-1-1" to "IEC 61753-1"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #338.

Cl **182** *SC* **182.7.3** *P* **406** *L* **45** # 345

Lambert, Angie Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #339.

Cl **182** *SC* **182.7.3.1.1** *P* **407** *L* **11** # 587

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *Connector labeling*

To support breakout, loopback, and OAN/OLT connectro should be labled

SuggestedRemedy

DR2-2 connector should be labled as Tx1Tx2 ------ Rx2Rx1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #590.

Cl **182** *SC* **182.7.3.1.2** *P* **407** *L* **27** # 588

Ghiasi, Ali Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *Connector labeling*

To support breakout, loopback, and OAN/OLT connectro should be labled

SuggestedRemedy

DR2-4 connector should be labled as Tx1Tx2Tx3Tx4 ------ Rx4Rx3Rx2Rx1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #590.

Cl **182** *SC* **182.7.3.1.3** *P* **408** *L* **15** # 589

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *Connector labeling*

To support breakout, loopback, and OAN/OLT connectro should be labled

SuggestedRemedy

DR2-8 connector should be labled as Tx1Tx2Tx3Tx4Tx5Tx6Tx7Tx8
Rx8Rx7Rx6Rx5Rx4Rx3Rx2Rx1

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #590.

Cl **182** *SC* **182.7.3.2** *P* **408** *L* **22** # 347

Lambert, Angie — Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #339.

Cl **182** *SC* **182.7.3.2** *P* **408** *L* **22** # 346

Lambert, Angie — Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-1-1 has been superseded by IEC 61753-1.

SuggestedRemedy

Change "IEC 61753-1-1" to "IEC 61753-1"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #338.

Cl **182** *SC* **182.7.3.3** *P* **409** *L* **1** # 348

Lambert, Angie — Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #339.

Cl **182** *SC* **182.7.3.4** *P* **409** *L* **8** # 349

Lambert, Angie — Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #339.

Cl **182** *SC* **182.8.5** *P* **411** *L* **30** # 19

LeCheminant, Greg — Keysight Technologies

Comment Type **T** *Comment Status* **A** *TDECQ*

The current method for optimizing the tap weighs of equalizer in the TDECQ reference receiver is described in clause 121.8.5. The equalizer tap coefficients are iteratively adjusted to effectively minimize the TDECQ penalty. Although not explicitly stated, one way to view this is that ANY combination of tap weights is valid and that ALL combinations should be tried to ensure the optimum tap weight combination is used when calculating TDECQ. As the equalizer length has been increased from 5 taps to 15 taps, the time required to verify all possible tap weights is likely problematic. This issue was managed in the 802.3 db project, where a 9 tap virtual equalizer is used for TDECQ. The following text was added to clause the definition of the TDECQ method: ôThe lowest measured TDECQ values are achieved with the equalizer optimization method described in 121.8.5. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time, and are expected to report equal or higher values of TDECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibrationö. Note that the MMSE optimization method is used in almost all TDECQ measurements performed today

SuggestedRemedy

Add the following text at line 44 (end of exceptions list): The lowest measured TDECQ values are achieved with the equalizer optimization method described in 121.8.5. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time, and are expected to report equal or higher values of TDECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibration

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #17

Cl **182** *SC* **182.8.5** *P* **411** *L* **30** # 3

Johnson, John — Broadcom

Comment Type **T** *Comment Status* **A** *TDECQ*

121.8.5.2 Table 121-11 specifies ORL of 21.4dB be applied for TX testing. For 200GBASE-FR1, this needs to be 17.1dB.

SuggestedRemedy

Add a new exception to the list in 182.8.5:
"- The optical return loss is as given in Table 182-7."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement the suggested remedy with editorial license.

Cl **182** *SC* **182.8.5** *P* **411** *L* **30** # 113

Stassar, Peter — Huawei Technologies

Comment Type **T** *Comment Status* **A** *TDECQ*

Currently reference is made to compliance channel in 121.8.5.2, which is for 500m instead of 2km

SuggestedRemedy

Create new subclause 182.8.5.1 and refer to it instead of 121.8.5.2. Create 182.5.2.1 with contents along the lines of 124.8.5.1 from 802.3df with the same compliance channel. Develop with editorial license

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **182** *SC* **182.8.11** *P* **413** *L* **10** # 15

LeCheminant, Greg — Keysight Technologies

Comment Type **T** *Comment Status* **A** *RIN-OMA*

The required -3dB BW for the measurement system is not achievable with existing technology. (State of the art power meters with a maximum 120 GHz bandwidth, would require the bandwidth of the photodetetor to be substaitially higher than 120 GHz to achieve the current system bandiwdth required for the test system, as defined in clause 52)

SuggestedRemedy

The bandiwdth of the RIN-OMA test system should be based on the expected bandwidth of the system receivers and consider the expected noise spectrum of transmitters. Spec limits for RIN OMA may need adjustment to adapt to any changes in the test method

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #518

Cl **182** *SC* **182.9.1** *P* **413** *L* **43** # 350

Lambert, Angie — Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 60950-1 has been superseded by IEC 62368-1.

SuggestedRemedy

Change "IEC 60950-1" to "IEC 63268-1".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #342.

Cl **183** *SC* **183.1** *P* **418** *L* **39** # 305

Maki, Jeffery — Juniper Networks

Comment Type **TR** *Comment Status* **A** *IMDD acronym (bucket)*

Associated clause description is malformed. The acronym IMDD is used, which does not appear in the actual Clause 177 title. Why preclude that at some future point in time that Clause 177 is used for something other than IMDD? Also, there is no use of "Coherent" to describe Inner FECs used for coherent PMDs to setup the appropriate parallelism of terminology.

SuggestedRemedy

Delete the acronym IMDD.

Response *Response Status* **C**

ACCEPT.

Cl **183** *SC* **183.4** *P* **420** *L* **37** # 148

Ghiasi, Ali — Ghiasi Quantum/Marvell

Comment Type **T** *Comment Status* **A** *Precoding*

Prior to 183.4 add section for PMA function to support precoder to mitigate burst errors

SuggestedRemedy

The transmitter need to supports 1/(1+D) mod 4 precoding, as specified in 135.5.7.2, 120.5.7.2, and 173.5.7.2, 6 and 176.9.1.2, that may be enabled or disabled as needed with OLT, without OLT the optical transmitter should enable 1/(1+D) mod 4 precoding to mitigate burst error.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using response to comment #547.

Cl **183** *SC* **183.6.1** *P* **425** *L* **16** # 7

Johnson, John — Broadcom

Comment Type **T** *Comment Status* **A** *TX specs*

Total average launch power (max) in Table 183-6 is TBD for 800GBASE-FR4.

SuggestedRemedy

Replace TBD with a value equal to the Average launch power, each lane (max) + 6 dB, which is 4.9 + 6 = 10.9 dB. This methodology is consistent with previous FR4 PMDs (clauses 122, 151) and 800GBASE-LR4 in this Table.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **183** *SC* **183.6.1** *P* **425** *L* **19** # 166

Yu, Rang-chen — InnoLight

Comment Type **TR** *Comment Status* **A** *TX specs*

Recommended relationship between 'Tx_OMAout (min)' and 'Tx_Pavg (min)' for 800G LR4 (in Table 183û6) should follow 400G LR4-6, with delta equal to 3dB, assuming max . OER infinite.

SuggestedRemedy

With 'OMAout (min)'=1.9dBm, then 'Average launch power, each lane' for 800G LR4 in Table 183û6 should be changed to -1.1dBm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

In Table 183-6 for LR4 change "Average launch power, each lane (min)" from -0.9 to -1.1

In Table 183-6, add a footnote to the value "-1.1" on the row for "Average launch power, each lane (min)" with the following text:
"Average launch power of -1.1 dBm corresponds to an OMA of 1.9 dBm with an infinite extinction ratio."

With editorial license.

Cl **183** *SC* **183.6.1** *P* **425** *L* **19** # 164

Yu, Rang-chen — InnoLight

Comment Type **TR** *Comment Status* **A** *TX specs*

recommend relationship between 'Tx_OMAout (min)' and 'Tx_Pavg (min)' (in Table 183û6) follow 400G FR4, with delta=3dB, assuming max. OER infinite.

SuggestedRemedy

With 'OMAout (min)'=0.8dBm, then 'Average launch power, each lane (min) ' in Table 183û6 should be changed to -2.2dBm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In Table 183-6 for FR4 change "Average launch power, each lane (min)" from -1.8 to -2.2

In Table 183-6, add a footnote to the value "-2.2" on the row for "Average launch power, each lane (min)" with the following text:
"Average launch power of -2.2 dBm corresponds to an OMA of 0.8 dBm with an infinite extinction ratio."

With editorial license.

Cl **183** *SC* **183.6.1** *P* **425** *L* **19** # 329

Welch, Brian Cisco

Comment Type **TR** *Comment Status* **A** *TX specs*

In later 100GPL specs (ie, 400GBASE-FR4) the difference between OMA(min) and Pave(min) was 3dB, to reflect the case of infinite extinction ratio. In the adopted baselines this narrowed to 2.6 dB as it was not updated to reflect the changes to effective TDECQ(min).

SuggestedRemedy

Propose changing "Average launch power, each lane (min)" in Table 183-6 from -1.8 dBm to -2.2 dBm.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #164.

Cl **183** *SC* **183.6.1** *P* **425** *L* **24** # 12

Johnson, John Broadcom

Comment Type **T** *Comment Status* **A** *TX specs*

The TX must be compliant over the full range of fiber length (dispersion), so the use of TDECQ alone is insufficient to determine Outer Optical Modulation Amplitude (OMAouter), each lane
(min) in Table 183-6 for 800GBASE-FR4/LR4.

SuggestedRemedy

Replace TDECQ with max(TECQ, TDECQ) for both PMDs, as has been done in all other PMDs in Clauses 180-182. Note that max(TECQ, TDECQ) is already in Equation 183-1. For consistency, replace "Equation 183-1" with "-0.1 + max(TECQ, TDECQ)" in Table 183-6, and delete Equation 183-1 on page 435, line 20. Also update Figures 183-3, 183-5, 183-6 and surrounding text with max(TECQ, TDECQ).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggest remedy with editorial license.

Cl **183** *SC* **183.6.1** *P* **425** *L* **27** # 503

Rodes, Roberto Coherent

Comment Type **T** *Comment Status* **A** *TX specs*

Change spec format consistent with FR4

SuggestedRemedy

Replace 0.5+TDECQ by 0.5+Max(TECQ,TDECQ)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #12

Cl **183** *SC* **183.6.1** *P* **425** *L* **28** # 9

Johnson, John Broadcom

Comment Type **T** *Comment Status* **A** *TX specs*

Difference in launch power between any two lanes (OMAouter) (max) in Table 183-6 is TBD for 800GBASE-FR4.

SuggestedRemedy

Replace TBD with a value of OMAouter(max) minus OMAouter(min) or 4 dB, whicher is smaller, consistent with other FRn/LRn clauses (122, 151).

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **183** *SC* **183.6.2** *P* **427** *L* **18** # 167

Yu, Rang-chen InnoLight

Comment Type **TR** *Comment Status* **A** *RX specs*

The delta between 'Tx_Pavg(min)' and 'Rx_Pavg(min)' for 800G LR4 should equal to 'Channel insertion loss' (6.3dB for LR4)

SuggestedRemedy

Rx_Pavg (min)' for 800G LR4 in Table 183û7 should be -1.1dBm-6.3dB=-7.4dBm

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

For Table 183-7, in the 800GBASE-LR4 column, change the value for "Average receive power, each lane (min)" to -7.4.

Cl **183** *SC* **183.6.2** *P* **427** *L* **18** # 165

Yu, Rang-chen InnoLight

Comment Type **TR** *Comment Status* **A** *RX specs*

The delta between 'Tx_Pavg(min)' and 'Rx_Pavg(min)' should equal to 'Channel insertion loss' (4.0dB for FR4)

SuggestedRemedy

Rx_Pavg (min)' in Table 183û7 should be -2.2dBm-4.0dB=-6.2dBm

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

For Table 183-7, in the 800GBASE-FR4 column, change the value for "Average receive power, each lane (min)" to -6.2.

Cl **183** *SC* **183.6.2** *P* **427** *L* **21** # 11

Johnson, John Broadcom

Comment Type **T** *Comment Status* **A** *RX specs*

Difference in receive power between any two lanes (OMAouter) (max) in Table 183-7 is TBD for 800GBASE-FR4.

SuggestedRemedy

Replace TBD with a value of 4.1 dB, consistent with other FR4 PMDs (Cl. 122, 151)

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **183** *SC* **183.6.3** *P* **428** *L* **51** # 502

Rodes, Roberto Coherent

Comment Type **T** *Comment Status* **A** *power budget*

Adding explanation on allocation for penalties calculation.

SuggestedRemedy

Use same approach than for the inserion loss adding a note in the LR4 value with the text:"Allocation for penalties is calculated using an additional penalty of 0.7dB from DGD, and 0.4dB from MPI"

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement suggested remedy with editorial license.

Cl **183** *SC* **183.6.3** *P* **429** *L* **6** # 172

Yu, Rang-chen InnoLight

Comment Type **T** *Comment Status* **A** *power budget*

Although TDECQmax is still TBD. However, the footnote b should also indicate the allocation for penalties, just leave dispersion section as TBD for future update.

SuggestedRemedy

Recommend to add "Allocations to penalties for 800G-FR4 including penalties due to dipersion TBDdB, DGD and MPI 0.5dB" to footnote e.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #171.

Cl **183** *SC* **183.6.3** *P* **429** *L* **6** # 168

Yu, Rang-chen InnoLight

Comment Type **T** *Comment Status* **A** *power budget*

Footnote e did not clarify what's the compisiton of total 5dB allocation for penalties.

SuggestedRemedy

Recommend to add "Allocations to penalties for 800G-LR4 including penalties due to dipersion 3.9dB, DGD 0.7dB and MPI 0.4dB" to footnote e.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #502.

Cl **183** *SC* **183.7** *P* **431** *L* **12** # 208

Parsons, Earl CommScope

Comment Type **T** *Comment Status* **R** *optical channel specs*

The positive and negative dispersion values in this table should come from a channel model that uses a statistical approach. A contribution on fiber disperison statistics will be submitted.

SuggestedRemedy

Replace TBDs with values agreed upon by the Task Force.

Response *Response Status* **C**

REJECT.
The following presentation was reviewed by the 802.3dj task force at the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/parsons_3dj_01a_2405.pdf
The presentation provided an overview of the latest fiber data set that could be used to determine dispersion parameters but no specific values were provided or directions on how to modify the draft.

Cl **183** *SC* **183.7.1** *P* **431** *L* **31** # 125

Johnson, John Broadcom

Comment Type **T** *Comment Status* **A** *optical channel specs*

Clause 183.7.1 is TBD.

SuggestedRemedy

Use the same text and table as given in 182.7.1. Since this sub-clause only reiterates fiber cable specs from external standards, not 802.3 specific specs, this should not be controversial.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **183** *SC* **183.7.2** *P* **431** *L* **41** # 126

Johnson, John Broadcom

Comment Type **T** *Comment Status* **A** *optical channel specs*

Clause 183.7.2 is TBD.

SuggestedRemedy

Use the same text as given in 182.7.2: "An optical fiber connection, as shown in Figure 183û7, consists of a mated pair of optical connectors." Since this is a basic definition of terms, it should not be controversial.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **183** *SC* **183.7.3** *P* **432** *L* **40** # 351

Lambert, Angie Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #339.

Cl **183** *SC* **183.8.5** *P* **435** *L* **25** # 20

LeCheminant, Greg Keysight Technologies

Comment Type **T** *Comment Status* **A** *TDECQ*

The current method for optimizing the tap weighs of equalizer in the TDECQ reference receiver is described in clause 121.8.5. The equalizer tap coefficients are iteratively adjusted to effectively minimize the TDECQ penalty. Although not explicitly stated, one way to view this is that ANY combination of tap weights is valid and that ALL combinations should be tried to ensure the optimum tap weight combination is used when calculating TDECQ. As the equalizer length has been increased from 5 taps to 15 taps, the time required to verify all possible tap weights is likely problematic. This issue was managed in the 802.3 db project, where a 9 tap virtual equalizer is used for TDECQ. The following text was added to clause the definition of the TDECQ method: ôThe lowest measured TDECQ values are achieved with the equalizer optimization method described in 121.8.5. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time, and are expected to report equal or higher values of TDECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibrationö. Note that the MMSE optimization method is used in almost all TDECQ measurements performed today

SuggestedRemedy

Add the following text at line 40 (end of exceptions list): The lowest measured TDECQ values are achieved with the equalizer optimization method described in 121.8.5. Alternative optimization methods such as minimum mean squared error (MMSE) may be used to determine equalizer tap weights to reduce test time, and are expected to report equal or higher values of TDECQ. These alternative methods should not be used for receiver sensitivity and stressed receiver sensitivity calibration

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #17

Cl **183** *SC* **183.8.11** *P* **437** *L* **41** # 16

LeCheminant, Greg Keysight Technologies

Comment Type **T** *Comment Status* **A** *RIN-OMA*

The required -3dB BW for the measurement system is not achievable with existing technology. (State of the art power meters with a maximum 120 GHz bandwidth, would require the bandwidth of the photodetetor to be substaitially higher than 120 GHz to achieve the current system bandiwdth required for the test system, as defined in clause 52)

SuggestedRemedy

The bandiwdth of the RIN-OMA test system should be based on the expected bandwidth of the system receivers and consider the expected noise spectrum of transmitters. Spec limits for RIN OMA may need adjustment to adapt to any changes in the test method

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #518

Cl **184** *SC* **184.1.1** *P* **441** *L* **8** # 308

Bruckman, Leon Huawei

Comment Type **TR** *Comment Status* **A** *General (Bucket)*

The Inner FEC as defined, includes the PMA. Shall make this clear to the reader

SuggestedRemedy

Either add sentence: "This Inner FEC subllayer includes functionality often associated with the PMA sublayer", or split the PMA function

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Add sentence: "This Inner FEC sublayer includes functionality often associated with the PMA sublayer at the PMD service interface".
Add similar text to the appropiate sub clause in clause 177
[Editor's note: CC 184, 177]

Cl **184** *SC* **184.2** *P* **443** *L* **7** # 87

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **R** *General (Bucket)*

Other diagrams of this type do not have dashed boxes areound the transmit and received processes.

SuggestedRemedy

For consisetncy with the rest of the document, remove the dashed boxes

Response *Response Status* **C**

REJECT.

The dashed boxes clearly denote the transmit and receive functions. Removing the dashed boxes does not improve clarity of the draft.

Cl **184** *SC* **184.2** *P* **444** *L* **5** # 88

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *Functional (Bucket)*

The second sentence of the paragraph (dsicussing the distribution to 32 lanes by the permutation function) sems to imply that the 32 lanes were interleaved into a serial stream after they were reordered and deskewed, but the text doesn't actually say that is done.

SuggestedRemedy

If the intent is that the 32 lanes are re-interleaved, and then the permutation function distributes the symbols back to 32 lanes (in something other than a round-robin manner), change the end of the first sentence to say "àreordered, deskewed, and serialized". If the intent is that the permutation process just moves symbols around among the 32 lanes, change the second sentence to say "The RS-FEC symbols are then rearranged across the 32 lanes by a permutation function.".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Change "The RS-FEC symbols are then distributed over the 32 lanes by a permutation function. " to "The RS-FEC symbols are then rearranged across the 32 lanes by a permutation function."

Cl **184** *SC* **184.4** *P* **445** *L* **22** # 184

Brown, Matt Alphawave Semi

Comment Type **T** *Comment Status* **A** *Reorder (Bucket)*

The Inner FEC transmit (184.4) and receive (184.5) functions provide a BCH encoder/decoder and other functions to be performed on each PCS lane. Although there is one per PCS lane, these should be called "flows" rather than "lanes" to be consistent with other FEC clauses and to differentiate between "lanes" that go between sublayers.

SuggestedRemedy

When describing the process applied to each PCS lane in each direction, use the word "flow" rather than "lane".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the suggested remedy with editorial license.

Cl **184** *SC* **184.4.1** *P* **445** *L* **3** # 299

Loewenthal, Arnon alphawave semi

Comment Type **T** *Comment Status* **A** *Functional (bucket)*

Need to further define the deskew requirement. For now it is defined as optional. In practice full deskew is optional, but doing 10b alignment of RS symbols is mandatory.

SuggestedRemedy

Replace lines 8-18 with the requirement of partial deskew, which means 10b RS symbols resolution deskew.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
In the first paragraph of clause 184.4.1 delete ", when implemented,"
and delete the second paragraph

Cl **184** *SC* **184.4.1** *P* **445** *L* **5** # 89

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *Functional (bucket1p)*

There are always many implementation options, but we don't have to describe them in the document, we just have to describe the behavior that is required.

SuggestedRemedy

Delete "when implemented" from the first sentence, and delete the second paragraph.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In the first paragraph of clause 184.4.1 delete ", when implemented,"
and delete the second paragraph with editorial license.

Cl **184** *SC* **184.4.1** *P* **445** *L* **12** # 90

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *Functional (Bucket)*

What is the purpose of this mapping? There are 32 lanes being received; this process is simply aligning them based on the RS FEC frame, so it doesn't seem like a.mapping is needed.

SuggestedRemedy

Either explain why this mapping process is needed, or delete it.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Add text to explain the purpose of this mapping.
Implement with editorial license.

Cl **184** *SC* **184.4.1** *P* **445** *L* **12** # 178

Brown, Matt Alphawave Semi

Comment Type **T** *Comment Status* **A** *Functional (bucket1p)*

The process provided in 184.4.1 "Alignment lock and deskew" merely maps bits on the FEC service interface to vectors; it does not include and RS-FEC symbol alignment. The process in 184.4.2 remaps the vectors such that there is alignment to the RS-FEC symbols and the lanes are properly ordered.

SuggestedRemedy

Either combine the two subclauses and process into one subclause or move the RS-FEC symbol alignment process in 184.4.2 to 184.4.1.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Move the RS-FEC symbol alignment process in 184.4.2 to 184.4.1.

Cl **184** *SC* **184.4.2** *P* **445** *L* **19** # 300

Loewenthal, Arnon alphawave semi

Comment Type **T** *Comment Status* **A** *Reorder. (Bucket)*

Need to further define the lanes reorder requirement. For now it is defined as optional. In practice full lanes reorder is optional, but partial reorder, meaning having flow-0 on lanes 0-15 and flow-1 on lanes 16-31 is required. Not doing that would impact end to end FEC performance and margins.

SuggestedRemedy

Two options:
1. remove the word 'optional' from line 22.
2. Define the restriction of having flow-0 on lanes 0-15 and flow-1 on lanes 16-31.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Change: "If that is the case, the optional lane reorder function shall order the PCS lanes according to the PCS lane number." to: "The lane reorder function shall order the PCS lanes according to the PCS lane number."

Cl **184** *SC* **184.4.2** *P* **445** *L* **22** # 179

Brown, Matt — Alphawave Semi

Comment Type **T** *Comment Status* **A** *Reorder (Bucket)*

The lane reorder process is stated as being optional, however, that is not the case. It is not required (or optional) if the lanes are already in order (e.g., connected to a PCS above) and mandatory if the lanes may not be in order (e.g., connected to an 8:32 PMA above), thus it is conditional, rather than optional.

SuggestedRemedy

Change the first 2 sentences in 184.4.2 to "If the sublayer above the Inner FEC does not provide the PCS lanes in order at the service interface, the lane reorder function shall reorder the PCS lanes according to the PCS lane number.".

Response *Response Status* **C**

ACCEPT.

Cl **184** *SC* **184.4.2** *P* **445** *L* **22** # 91

Huber, Thomas — Nokia

Comment Type **T** *Comment Status* **A** *Reorder (Bucket)*

Lane reordering is not optional; the lanes have to be put in the correct order. If they happen to arrive in the correct order, it's a simple process.

SuggestedRemedy

Change the second sentence to say "The lane reorder process shall order the PCS lanes according to the PCS lane number."

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #300

Cl **184** *SC* **184.4.2** *P* **445** *L* **26** # 92

Huber, Thomas — Nokia

Comment Type **T** *Comment Status* **A** *Reorder (bucket1p)*

It is not clear why this description is needed. Other clauses about reordering don't have this.

SuggestedRemedy

Delete the last paragraph

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #178

Cl **184** *SC* **184.4.3** *P* **446** *L* **1** # 93

Huber, Thomas — Nokia

Comment Type **T** *Comment Status* **A** *Reorder (bucket1p)*

This figure is not clear, nor is the relatoinship of the figure to the pseudocode beneath it. I think the columns 0-3 are just numbers that relate to the post-FEC distribution process. I have no idea why there are 32 sets of 4 symbols, as the algorithm doesn't do anything on a four-symbol basis. The function is simply reversing flow1 and flow0 every two columns, so that each lane has interleaved symbols from all four codewords. This could be described more simply by using blocks of 16 symbols in the figure (i.e.., block 0 would be lanes 0-15 in column 0, block 1 would be lanes 16-31 in column 0, etc.).

SuggestedRemedy

Revise the figure as suggested. The input side would look like this (where each row here is corresponding to 16 PCS lanes i nthe figure):
0 2 4 6
1 3 5 7
and the output would be
0 2 5 7
1 3 4 6

This will remove any confusion about whether the 32 blocks are supposed to be somehow related to the 32 PCS lanes, and it will be it easier to see what is changing between the figures.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Change:
"The lane permutation function distributes RS-FEC symbols from the four RS(544,514) codewords present in
the 32 PCS lanes as shown in Figure 184-3."
to:
"The lane permutation function distributes RS-FEC symbols from the four RS(544,514) codewords present in
the 32 PCS lanes as defined by the following pseudocode and illustrated in Figure 184-3."

Move the pseudo-code before Figure 184-3.

Update Figure 184-3 to make it more clear per the suggested remedy and remain consistent with the pseudocode.

Implement with editorial license.

Cl **184** *SC* **184.4.3** *P* **446** *L* **45** # 94

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **R** *Algorithm (bucket1p)*

The algorithm is unnecessarily complex. There is no need for bit-level detail since the operation is performed on 10-bit symbols - though really it seems to be performed on 160-bit entities. Per figure 184-3, it's essentially receiving as input alternating sets of 160 bits from flow0 and flow1, and changing the order from 0, 1, 0, 1, 0, 1, 0, 1 to 0, 1, 0, 1, 1, 0, 1, 0.

SuggestedRemedy

A minimal change would be to state that the algorithm operates on 10-bit symbols, delete the for jà loop and its terminator, and replace "10i+j" with "I" in the statement that describes the permutation..

Another option would be to rewrite the description around the 160-bit entities as described, and perhaps also change the figure to show those instead of 40-bit entities (which as noted in a previous comment seem to have no relevance to this process, or to the convolutional interleaver process that follows it).

Response *Response Status* **C**

REJECT.
The algorithm is correct and unambiguous as written, and reflects the adopted baseline. This bit-wise mapping shows explicitly how the bits are mapped into the larger vector.

There is sympathy for the direction of the suggested remedy; however, a more complete consensus proposal would be needed to change the current description.

Cl **184** *SC* **184.4.4** *P* **447** *L* **22** # 95

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *Algorithm (Bucket)*

The description of the convolutional interleaver process could be improved. The variable i is used in the first part of the subclause as an index for the delay lines and as an indication of time within a sequence. Then at the bottom of page 447 it's used a symbol index.

SuggestedRemedy

Revise the list above the figure to read as follows, eliminating the overleading of the index i and improcing the clarity a bit (and change the figure to label the lines as b=0, b=1, b-2)::
a) The input and output switches are always aligned to the same row b, where b = 0 to 2
b) a block of 40 bits is read from row b
c) The concents of row b are shifted to the right by 40 bits
d) A block of 40 bits is written to row b
e) The switch position is updated to (b+1) mod 3

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.

Cl **184** *SC* **184.4.4** *P* **447** *L* **48** # 96

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **R** *Algorithm (bucket1p)*

Since the convolutional interleaver operates separately on each PCS lane, there's no value in having an algorithm that includes the PCS lanes. Since it operates on 40-bit units, there's also no need to include bit-level description.

SuggestedRemedy

State that the algorithm describes the operation on the 40 bit entities and is run on each PCS lane independently. This allows elimination of the p and j variables.

Response *Response Status* **C**

REJECT.

The algorithm is correct and unambiguous as written, and reflects the adopted baseline.

Cl **184** *SC* **184.4.4** *P* **448** *L* **3** # 97

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *Algorithm*

The algorithm relating the convolutional interleaver output to its input doesn't work when i<36 - it refers to negative block numbers for the input (permo) whlie the delay lines are filling, and those negative numbers need to be ignored as the process starts up. In other words, given the input sequence of 40-bit blocks 0, 1, 2, 3, à, the convolutional interleaver is supposed to produce the output sequence 0, 3, 6, 9, 12, 15, 18, 1, 21, 4, 24, 7, 27, 10, 30, 13, 33, 16, then 36, 19, 2, and then each successive set of 3 is 3 more than the previous (so it continues 39, 22, 5, 42, 25, 8, ...). The algorithm says that output 0 is input 0-18 x (0 mod 3), so that produces 0 as expected, but output 1 is then supposed to be input 1-18 x (1 mod 3), which is -17, not 3.

SuggestedRemedy

The text above figure 184-4 already provides an algorithmix description of how the interleaver works. Rather than a second algorithmic description, it might be better to show the worked example as noted in the comment - i.e., show a table of input blocks from 0 to 42, and the corresponding output blocks.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #613

Cl **184** *SC* **184.4.4** *P* **448** *L* **5** # 613

Huang, Kechao — Huawei Technologies Co., Ltd.

Comment Type **T** *Comment Status* **A** *Algorithm*

For permo[p, 40x(i-18x i mod 3)+j], the column index 40x(i-18x i mod 3)+j may be a negative value

SuggestedRemedy

Suggest to add one sentence after Line 9: When 40x(i-18x i mod 3)+j is negative, permo[p, 40x(i-18x i mod 3)+j] will be undetermined value from initial buffer of the convolutional interleaver.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license.
Add the following sentence after Line 9: "When 40x(i-18x i mod 3)+j is negative, permo is undefined."

Cl **184** *SC* **184.4.5** *P* **448** *L* **12** # 98

Huber, Thomas — Nokia

Comment Type **T** *Comment Status* **A** *Algorithm (Bucket)*

The first statement should not be a 'shall' (which indicates a PICS item of conformance). The second sentence is correct, in that there are 32 encoders, but what's actually required is that each lane has an encoder.

SuggestedRemedy

Revise the paragraph to read: The BCH encoder works in conjunction with the RS(544,514) FEC to increase the FEC coding gain. There is a BCH encoder process for each PCS lane.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement the following with editorial license .
Change: "The BCH encoder shall work in conjunction with the outer RS(544,514) FEC to provide a high-performance FEC for 800GBASE-LR1. There are 32 BCH encoder functions." to: "The BCH encoder works in conjunction with the outer RS(544,514) FEC to provide a high-performance FEC for 800GBASE-LR1. The Inner FEC shall implement 32 BCH encoder functions."

Cl **184** *SC* **184.4.5** *P* **448** *L* **40** # 99

Huber, Thomas — Nokia

Comment Type **T** *Comment Status* **A** *Algorithm (bucket1p)*

The variable p is being overloaded - it is used at line 35 as a lane index, and at line 40 as the parity polynomial. Since the BCH encoding is done per lane, there is really no need to have a variable related to the lane number. The text can simply state that the algorithm is applied to each lane individually.

SuggestedRemedy

Change the line above the dashed list to say "The BCH encoding is done separately on each lane. The encoding of of each BCH codeword u is deined as follows:

At the top of page 449, remove the 'for pà' loop from the pseudocode.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The algorithm is correct as written, and reflects the adopted baseline. However, "p" is used for another purpose in the previous subclause.

Change the flow index from p to q and implement with editorial license.

Cl **184** *SC* **184.4.6** *P* **449** *L* **16** # 100

Huber, Thomas — Nokia

Comment Type **T** *Comment Status* **R** *Algorithm (bucket1p)*

Clarify that the circular shift is applied per lane.

SuggestedRemedy

Make similar changes to what was suggested in previous sections - remove the unnecessary variable p and associated for loop in the pseudocode, and add a sentence stating that the circular shift process is performed on each lane individually.

Response *Response Status* **C**

REJECT.
The algorithm is correct and unambiguous as written, and reflects the adopted baseline.

Cl **184** *SC* **184.4.7.1** *P* **450** *L* **12** # 101

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *Order (Bucket)*

The DSP frame should probably be a level 3 clause of its own, rather than a sub-clause under BCH interleaver.

SuggestedRemedy

Change to a level 3 heading

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The "BCH interleaver" function includes the pilot insertion. Change clause 184.4.7 title to: BCH interleaver and pilot insertion"
Implement with editorial license.

Cl **184** *SC* **184.4.7.1** *P* **450** *L* **14** # 371

He, Xiang Huawei

Comment Type **TR** *Comment Status* **A** *DSP (Bucket)*

It is said " 4-bit pilot symbols (PS) are inserted every 64 4-bit blocks (one 4-bit PS, 63 4-bit message blocks)."
But in Figure 184-5, message blocks m<0:63>, m<64-127>, àbetween pilot symbols has 64 4-bit blocks.

SuggestedRemedy

Change Figure to match the text, i.e., change m<0:63> to m<0:62>, change m<64:127> to m<63:125>, etc.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.

Cl **184** *SC* **184.4.7.1** *P* **450** *L* **18** # 102

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *DSP (Bucket)*

The first sentence of the second paragraph could be written more clearly.

SuggestedRemedy

Replace with "Two streams of DSP frames, one for each polarization, are generated by the inner FEC."

Response *Response Status* **C**

ACCEPT.

Cl **184** *SC* **184.4.7.2** *P* **450** *L* **45** # 103

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *DSP (Bucket)*

It is not clear what "192 bits that are complemented with zeros" is intended to mean. Based on what is in Table 184-2, I think the intent is that a zero is inserted after each bit of the PRBS9 ouput to form the bit-pairs that become the PS symbols. Also, the text talks about 4-bit PS symbols, but Table 184-2 is showing bit-pairs for each component rather than 4-bit symbols without explaining that outputs 0 and 1 are for the X polarization (so the X PRBS is spread across outputs 0 and 1) and outputs 2 and 3 are for the Y polarization.

SuggestedRemedy

Revise the two pargraphs above table 184-1 to read as follows:
For both DSP frame_0 and DSP frame_1, the generator is initialized using the seed at the start of every DSP frame. The generator produces a sequence of 192 bits. A zero bit inserted after each bit to generate the bit-pairs that form the pilot symbos, which use the outer points of the 16QAM constellation.

The generator polynomial and seed values are shown in Figure 184-6 and listed in Table 184-1. The complete pilot sequence is shown in Table 184-2. The bit-pairs for the X polarization are distributed in a round-robin manner to outputs 0 and 1. The bit-pairs for the Y polarization are distributed in a round-robin manner to outputs 2 and 3.

Response *Response Status* **C**

ACCEPT.

Cl **184** *SC* **184.4.9** *P* **452** *L* **50** # 104

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *Interface (Bucket)*

The editor's note suggesting that the mapping to analog signals probably belongs in the PMD clause seems to make sense, in which case this clause is really not "DP-16QAM mapping", it's really just mapping to 4-level signals, which the PMD will then turn into DP-16QAM.

SuggestedRemedy

Change the title to "4-level signal mapper", and make the corresponding change in 184.5.3.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
After the first sentence of subclause 184.4.9 add: "This four-level signals are used by the 800GBASE-LR1 PMD to generate a single optical DP-16QAM signal with orthogonal polarizations (see 185.4.2)."
Implement with editorial license.

Cl **184** *SC* **184.4.9** *P* **452** *L* **50** # 105

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **R** *Order (Bucket)*

The overall flow would be improved if it went BCH interleaver, 4-level signal mapping, DSP frame, with all the pilot symbol details then in the DSP frame clause.

SuggestedRemedy

Revise so the flow is like this:
184.4.7 BCH interleaver
184.4.8 Four-level signal mapping (current 184.4.9, without subclauses)
184.4.9 DSP frame generation (current 184.4.7.1)
184.4.9.1 Pilot sequence (current 184.4.7.2 and 184.4.9.1)

Response *Response Status* **C**

REJECT.
The text is correct as written.
The actual order is the right one. It describes the bit blocks generation and handling, then the mapping to four levels.

Cl **184** *SC* **184.5.1** *P* **455** *L* **42** # 106

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **R** *Interface (bucket1p)*

The paragraph that begins with "the signals Rx_Xi, Rx_XQ, à" doesn't seem to make sense. The Tx and Rx signals are not guaranteed to be the same (i.e., Tx_XI can be received as any of the four components), but the contents of Tx_XI aren't distibuted to all the Rx signals.

SuggestedRemedy

Revise to say: The signals Rx_XI, Rx_XQ, Rx_YI, and Rx_YQ each represent one of the corresponding Tx_XI, Tx_XQ, Tx_YI, Tx_YQ signals from the transmitting PMD. The association between Tx and Rx components is arbitary (e.g., Rx_XI can be any of the 4 Tx components).

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **184** *SC* **184.5.8** *P* **457** *L* **45** # 107

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *Algorithm (Bucket)*

Similar changes should be made in the convolutional de-interleaver as were requested for the convolutional interleaver in earlier comments

SuggestedRemedy

Revise the items in the lettered list and the algoritm to align with whatever changes are agreed for the convolutional interleaver.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.

Cl **184** *SC* **184.6.5** *P* **462** *L* **1** # 372

He, Xiang Huawei

Comment Type **TR** *Comment Status* **A** *Diagrams*

It is possible that one polarization is locked but the other polarization can not get locked. With the current variable list and state diagrams this can not be identified or reported. (This is a little different from AM lock process across PCS lanes, where it is way up in the sublayers higher than the pilot sequence lock, and it may not be a problem.)

SuggestedRemedy

Recommend to add a timer (value TBD) to indicate that it has waited long enough after one polarization is locked but the other is still not locked.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The DSP lock state diagram is implemented per polarization, so there is an indication of sync per polarization. There are no timers defined for alarm indications in the standard.
Add a status variable with mapping to MDIO address, to allow the user reading the status of the synchronization process per polarization.
[Editor's note: CC 184 45]

Cl **184** *SC* **184.6.5** *P* **462** *L* **3** # 307

Bruckman, Leon Huawei

Comment Type **TR** *Comment Status* **A** *Diagrams (bucket1p)*

Set TBD values of N and M

SuggestedRemedy

Set N=12, M=8. See contribution bruckman_3dj_01_241205

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The following presentation (referenced in the suggested remedy) was reviewed by the 802.3dj task force at the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/bruckman_3dj_01a_2405.pdf
Implement the suggested remedy with editorial license.

Cl **184** *SC* **184.6.5** *P* **462** *L* **9** # 559

Law, David HPE

Comment Type **T** *Comment Status* **A** *Diagrams (Bucket)*

The LOCK_INIT state in Figure 184û9 'DSP lock state diagram' includes the action 'test_sym <= false', however the test_sym variable isn't defined in subclause 184.6.2 'Variables' and isn't used anywhere else in Figure 184û9.
á
It seems that this should have been 'test_ps <= false' as the test_ps variable isn't initialised during reset in the LOCK_INIT state but used to control the GET_SYMBOL to FIND_1ST transition below.

SuggestedRemedy

Change 'test_sym <= false' to read 'test_ps <= false'.

Response *Response Status* **C**

ACCEPT.

Cl **184** *SC* **184.6.5** *P* **462** *L* **22** # 560

Law, David HPE

Comment Type **T** *Comment Status* **A** *Diagrams*

N (the number of consecutive PS symbols matching the expected value for a given polarization stream required to enter frame lock), and M (the number of consecutive PS symbols that don't match the expected value for a given polarization stream required to exit frame lock) used in Figure 184û9 'DSP lock state diagram' aren't defined in subclause 184.6 'Inner FEC state diagrams' or its subclauses.
á
Suggest that these values should be defined in one place (I assume in subclause 184.5.4 'DSP frame synchronization and pilot removal' which includes the text 'The values of N and M are TBD.), with a pointer to this subclause elsewhere.

SuggestedRemedy

[1] Insert a new subclause 184.6.5 'Constants' as follows, renumbering the following subclause.
á
184.6.5 Constants
M
The number of consecutive PS symbols that fail to match the expected value for a given polarization stream required to exit frame lock (see 184.5.4).
N
The number of consecutive PS symbols matching the expected value for a given polarization stream required to enter frame lock (see 184.5.4).
á
{2] In subclause 184.6.2 'Variables', change the text 'It is set to true when TBD PS symbols ...' to read 'It is set to true when M PS symbols ...' in the variable 'restart_lock' description.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

In the first paragraph of clause 184.5.4 remove: "The values of N and M are TBD."

Insert new subclause 184.6.5 "Constants" after subclause 184.6.4 as follows, renumbering the subsequent subclause:
****
184.6.5 Constants

M
The number of consecutive PS symbols that fail to match the expected value for a given polarization stream required to exit frame lock (see 184.5.4). M = 8.

N
The number of consecutive PS symbols matching the expected value for a given polarization stream required to enter frame lock (see 184.5.4). N=12.
****

In subclause 184.6.2 'Variables', change the text for "restart_lock" from:

"It is set to true when TBD PS symbols ..." to: "It is set to true when M PS symbols ..."

Implement with editorial license.

Cl **184** *SC* **184.6.5** *P* **463** *L* **6** # 558

Law, David HPE

Comment Type **E** *Comment Status* **A** *(editorial)*

The variable 'alignnment_status' used in the LOSS_OF_ALIGNMENT and ALIGNMENT_ACQUIRED states is misspelt.

SuggestedRemedy

Suggest that 'alignnment_status' should read 'alignment_status'.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement with editorial license and discretion.

Cl **184** *SC* **184.8** *P* **464** *L* **10** # 373

He, Xiang Huawei

Comment Type **TR** *Comment Status* **A** *Diagrams*

Only "alignment_valid" is reported, not individual "dsp_lock<x>" variables.

SuggestedRemedy

It is recommend to report both "dsp_lock<x>" in table 184-7, as we did for PCS lane lock where we reported "Lane x aligned" for all PCS lanes.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #372.

Cl **185** *SC* **185.1** *P* **468** *L* **19** # 323

D'Ambrosia, John Futurewei, U.S. Subsidiary of Huawei

Comment Type **TR** *Comment Status* **A** *Conditional PMA (bucket)*

Table 185-1, Figure 185-1, Figure 185-2 does not reflect the PHY type and clause correlation in Table 169-3a. There is no mention of 800GBASE-R BM-PMA, 800GAU-I8 2C2, 800GAUI-8 C2M, 800GBASE SM-PMA, 800GAUI-4 C2C, and 800GAUI-4 C2M.

Baseline Proposal in https://www.ieee802.org/3/dj/public/23_07/kota_3dj_01a_2307.pdf shows support for 800GAUI's.

SuggestedRemedy

Clause 185 needs to be updated to reflect these layers.
Table185-1needs the following entries -
800GBASE-R BM-PMA - conditional
800GAU-I8 2C2 - optional
800GAUI-8 C2M - optional
800GBASE SM-PMA - conditional
800GAUI-4 C2C - optional
800GAUI-4 C2M - optional
Add note "C= Conditional, 800GBASE-R BM-PMA is conditional, pending implementation of 800GAUI-8 C2C/C2M
800GBASE-R SM PMA is conditional, pending implementation of 800GAUI-4 C2C/C2M"

Figure 185-1 should include a PMA sublayer in the diagram and be added to legend below
FIgure 185-2 needs to be updated to show the 800GBASE-R PMA Sublayer and service interface between the PCS and Inner FEC

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Some optional and conditional sublayers are missing from Table 185-1 and the conditions for include the SM-PMA and BM-PMA should be included in this table.
Regarding Figure 185-1 and Figure 185-2, no PMA is shown because the 800GBASE-LR1 Inner FEC sublayer connects directly with the PCS; a PMA is not required between the PCS and the 800GBASE-LR1 Inner FEC. Note that the 800GBASE-LR1 Inner FEC subsumes some functions/services normally provided by a PMA for the PMD.
Add the following rows in Table 185-1:
800GBASE-R BM-PMA - conditional
800GAUI-8 C2C - optional
800GAUI-8 C2M - optional
800GBASE SM-PMA - conditional
800GAUI-4 C2C - optional
800GAUI-4 C2M - optional
Resolve the concern about conditional SM-PMA and BM-PMA related to Table 185-1 using the response to comment #317.
Implement with editorial license.

Cl **185** *SC* **185.3** *P* **473** *L* **31** # 114

Stassar, Peter Huawei Technologies

Comment Type **T** *Comment Status* **A** *Delay*

The TBDs need to be replaced by values. Follow the same methodology as in 154 and latest draft D3.0 of P802.3cw

SuggestedRemedy

Replace contents by The sum of the transmit and receive delays at one end of the link contributed by the 800GBASE-LR1 PMD including 2 m of fiber in one direction shall be no more than 16 384 bit times (32 pause_quanta or 20.48 ns).
A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 169.4 and its references.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement the suggested remedy and update Table 169-4 with editorial license.

Cl **185** *SC* **185.5.1** *P* **477** *L* **8** # 381

Maniloff, Eric Ciena

Comment Type **T** *Comment Status* **A** *TX specs*

The specification should have a Tx clock noise defined.

SuggestedRemedy

Add an entry for Tx clock phase noise (PN): Maximum PN mask

Add an entry for: Tx clock phase noise (PN); Maximum total integrated random jitter

Add an entry for: Tx clock phase noise (PN); Maximum total periodic jitter

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggest remedy with editorial license.

Cl **185** *SC* **185.5.1** *P* **477** *L* **8** # 380

Maniloff, Eric Ciena

Comment Type **T** *Comment Status* **A** *TX specs*

800GBASE-LR1 is being defined to allow unlocked lasers with frequency errors larger than the DSP digital acquisition range. Additional parameters are required for the Tx laser to accommodate this. Values will be provided after further study, but the new paramaters can be added to Table 185-4. A supporting contribution will be provided.

SuggestedRemedy

Add the following parameters to Table 185-4:

Maximum Tx laser frequency slew rate: Preacquisition [Units GHz/s]

Maximum Tx laser frequency slew rate: Post acquisition [Units GHz/ms]

Laser Relative Frequency tracking accuracy [Units GHz]

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
The following presentation was reviewed by the 802.3dj task force at the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/maniloff_3dj_01_2405.pdf
Implement suggest remedy with editorial license.

Cl **185** *SC* **185.5.1** *P* **477** *L* **8** # 384

Maniloff, Eric Ciena

Comment Type **T** *Comment Status* **R** *TQM*

TQM is currently undefined. Recommend adopting RSNR Penalty as a TQM. Supporting Contribution to be provided.

SuggestedRemedy

Replace TQM with RSNR Penalty

Response *Response Status* **C**

REJECT.
The following presentation was reviewed by the 802.3dj task force at the May Interim meeting:
https://www.ieee802.org/3/dj/public/24_05/maniloff_3dj_02_2405.pdf

No agreement yet on an appropriate quality metric therefore no consensus to make a change.

Cl **185** *SC* **185.5.1** *P* **477** *L* **12** # 578

Kota, Kishore — Marvell Semiconductor

Comment Type **TR** *Comment Status* **R** *(withdrawn)*

Minimum transmit power specification has a big impact on coherent module designs. This has been defined in the initial proposals as a specification on the average power following other coherent physical layer specifications defined for DWDM systems. However, there is opportunity for a 800GBASE-LR1 PMD to change this in a way which can relax module transmit specifications

SuggestedRemedy

Define the minimum transmit power specification to be defined per lane instead of average. See https://grouper.ieee.org/groups/802/3/dj/public/23_11/kota_3dj_01a_2311.pdf for an initial proposal based on this concept. Defining the power per lane provides an opportunity to relax lane mismatch specs.

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **185** *SC* **185.5.1** *P* **477** *L* **15** # 579

Kota, Kishore — Marvell Semiconductor

Comment Type **TR** *Comment Status* **R** *(withdrawn)*

The draft contains separate specifications of X-Y power imbalances and I-Q imbalance. However, there is an opportunity for a 800GBASE-LR1 PMD to change this in a way which can relax module transmit specifications

SuggestedRemedy

Having a separate X-Y and I-Q imbalance specification splits the imbalance power budget and results in a tighter specification than necessary. These specifications should be combined into a single lane-to-lane imbalance specification. See https://grouper.ieee.org/groups/802/3/dj/public/23_11/kota_3dj_01a_2311.pdf for an initial specification methodology proposal.

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **185** *SC* **185.5.2** *P* **478** *L* **15** # 580

Kota, Kishore — Marvell Semiconductor

Comment Type **TR** *Comment Status* **R** *(withdrawn)*

Average receiver power (min) and the per-lane transmit power (min) specifications should be tied to an appropriate transmit quality metric similar to the TDECQ specifications in other IMDD clauses

SuggestedRemedy

See https://grouper.ieee.org/groups/802/3/dj/public/24_01/kota_3dj_01a_2401.pdf and https://grouper.ieee.org/groups/802/3/dj/public/23_11/kota_3dj_01a_2311.pdf for initial proposals on how to tie the RX sensitivity and TX power specifications with a transmit quality metric. This provides flexibility to allow module designers to explore design tradeoffs to simplify designs in ways which can benefit end users.

Response *Response Status* **Z**

REJECT.

This comment was WITHDRAWN by the commenter.

Cl **185** *SC* **185.5.3** *P* **478** *L* **43** # 382

Maniloff, Eric — Ciena

Comment Type **T** *Comment Status* **A** *optical channel specs*

A value of -27dB is appropriate for Maximum discrete reflectance

SuggestedRemedy

Replace TBD for Maximum discrete reflectance with -27

Response *Response Status* **C**

ACCEPT.

Cl **185** *SC* **185.6** *P* **479** *L* **51** # 383

Maniloff, Eric — Ciena

Comment Type **T** *Comment Status* **A** *optical channel specs*

A value of 24dB is appropriate for Optical Return Loss

SuggestedRemedy

Replace TBD in Table 185-7 with 24

Response *Response Status* **C**

ACCEPT.

Cl **185** *SC* **185.6.3** *P* **480** *L* **52** # 352

Lambert, Angie — Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #339.

Cl **185** *SC* **185.7.1** *P* **481** *L* **21** # 374

He, Xiang — Huawei

Comment Type **TR** *Comment Status* **A** *test pattern (common)*

The 800GBASE-LR1 Inner FEC would not see or use scrambled idles as its input. The input to the 800GBASE-LR1 Inner FEC should be "scrambled idle processed by 800GBASE-R PCS".

SuggestedRemedy

Change "pattern description" column in Table 185-9 to "Scrambled idle procedd by 800GBASE-R PCS and then encoded by the 800GBASE-LR1 Inner FEC".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

The referenced text in Table 185-9 is as follows: "Scrambled idle encoded by the 800GBASE-LR1 Inner FEC"

The references provide are: 175.2.4.11 and 184.4. 175.2.4.11 is the incorrect reference as Clause 175 defines the 1.6TBASE-R PCS. The correct reference is 172.2.4.11; however, comment #375 addresses this error.

172.2.4.11 defines the scrambled idle test pattern as follows: "The scrambled idle test pattern is the output of the PCS when the input to the PCS at the 800GMII is composed only of idle control characters."

The description in Table 185-9 is correct, but could be reworded for clarification.

Change the description in Table 185-9 to: "Scrambled idle test pattern encoded by the 800GBASE-LR1 Inner FEC"

Cl **185** *SC* **185.7.1** *P* **481** *L* **21** # 375

He, Xiang — Huawei

Comment Type **TR** *Comment Status* **A** *test pattern (bucket)*

The scrambled idle test pattern for 800GBASE-R PCS is defined in 172.2.4.11, not 175.2.4.11.

SuggestedRemedy

Change "175.2.4.11" to "172.2.4.11" and format as external reference.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggested remedy with editorial license.

Cl **185** *SC* **185.11.4.6** *P* **490** *L* **27** # 353

Lambert, Angie — Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #339.

Cl **186** *SC* **186** *P* **491** *L* **1** # 334

de Koos, Andras — Microchip Technology

Comment Type **T** *Comment Status* **R** *(bucket)*

ER1 PCS: Planting the seed for when the PCS is ready to be properly reviewed.
How to calculate the path data delay across the ER1 PCS/PMA? Clause 90 and Annex 90A give general rules, like how to calculate the rx/tx path data delay when there are functions within the PHY that introduce cyclical delay.
But the path data delay in the ER1 PCS is very different from anything that has been imagined in Clause 90 - an Ethernet stream that floats within a GMP frame will present unique challenges; it is not immediately clear how to determine the min/max latency across such a PCS.
This might be worse than the Alignment marker issue!

SuggestedRemedy

Response *Response Status* **C**

REJECT.
The suggested remedy does not provide sufficient detail to implement.

Cl **186** *SC* **186** *P* **491** *L* **1** # 108

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *(bucket)*

The baseline for the 800GBASE-ER1[-20] PCS has issues with PTP accuracy when an extender sublayer is used.

SuggestedRemedy

Update the baseline per presentations in the May meeting proposing a mechanism to reduce the PTP inaccuracy.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the proposal in https://www.ieee802.org/3/dj/public/24_05/sluyski_3dj_01a_2405.pdf, which was presented in the May interim meeting. Impelemnt the suggested remedy in sluyski_3dj_01a_2405 with editorial license.

Cl **187** *SC* **187.3** *P* **497** *L* **31** # 115

Stassar, Peter Huawei Technologies

Comment Type **T** *Comment Status* **A** *Delay*

The TBDs need to be replaced by values. Follow the same methodology as in 154 and latest draft D3.0 of P802.3cw

SuggestedRemedy

Replace contents by The sum of the transmit and receive delays at one end of the link contributed by the 800GBASE-LR1 PMD including 2 m of fiber in one direction shall be no more than 16 384 bit times (32 pause_quanta or 20.48 ns).
A description of overall system delay constraints and the definitions for bit times and pause_quanta can be found in 169.4 and its references.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.

Implement the suggested remedy and update Table 169-4 with editorial license.

Cl **187** *SC* **187.5** *P* **502** *L* **17** # 117

Stassar, Peter Huawei Technologies

Comment Type **T** *Comment Status* **A** *RX specs*

Previously for Clause 154 and draft Clause 156 in D3.0 for P802.3cw 20 dB maximum receiver reflectance has been used, which is a common value in the industry and in draft Clause 155.5.2

SuggestedRemedy

For Receiver reflectance (max) replace TBD by 20 dB for both ER1-20 and ER1

Response *Response Status* **C**

ACCEPT.

Cl **187** *SC* **187.5.1** *P* **501** *L* **8** # 109

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *TX specs*

The ppm value for this PMD should be 20 ppm

SuggestedRemedy

Repalce TBD with 20

Response *Response Status* **C**

ACCEPT IN PRINCIPLE. Implement suggest remedy with editorial license.

Cl **187** *SC* **187.5.2** *P* **501** *L* **8** # 110

Huber, Thomas Nokia

Comment Type **T** *Comment Status* **A** *TX specs*

The ppm value for this PMD should be 20 ppm

SuggestedRemedy

Repalce TBD with 20

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggest remedy with editorial license.

Cl **187** *SC* **187.6** *P* **503** *L* **44** # 116

Stassar, Peter Huawei Technologies

Comment Type **T** *Comment Status* **A** *optical channel specs*

Negative dispersion does not occur around 1550 nm. 0 ps/nm is the minimum. Only need min and max dispersion as in draft D3.0 of P802.3cw. A safe upper limit of 20 ps/nm.km can be used for a wavelength close to 1550 nm

SuggestedRemedy

Replace "Positive dispersion (max)" by "Chromatic dispersion (max)" with value 400 ps/nm for ER1-20 and 800 ps/nm for ER1. Replace "Negative dispersion (min)" by "Chromatic dispersion (min)" with value 0 ps/nm for both ER1-20 and for ER1.

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Implement suggest remedy with editorial license.

Cl **187** *SC* **187.6.3** *P* **504** *L* **48** # 354

Lambert, Angie Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #339.

Cl **187** *SC* **187.11.4.6** *P* **514** *L* **25** # 355

Lambert, Angie Corning

Comment Type **T** *Comment Status* **A** *IEC revision*

IEC 61753-021-2 has been superseded by IEC 61753-021-02.

SuggestedRemedy

Change "IEC 61753-021-2" to "IEC 61753-021-02".

Response *Response Status* **C**

ACCEPT IN PRINCIPLE.
Resolve using the response to comment #339.