

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 00 SC 0 P565 L47 # 203

Brown, Matt Alphawave Semi

Comment Type T Comment Status X

Now that the receive signal names are sufficiently unique compared to the transmit signal names AND it is already explained in 187.5.3, the note at the bottom of Figure 186-11 is no longer required.

SuggestedRemedy

Delete the note at the bottom of Figure 186-11.

Proposed Response Response Status O

Cl 1 SC 1.3 P50 L41 # 398

Dawe, Piers Nvidia

Comment Type T Comment Status X

The OSFP specification has been updated. Notice that 1.3 says "Standards may be subject to revision, and parties subject to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards indicated below"

SuggestedRemedy

Update OSFP from Rev 5.0, October 2, 2022 to Rev 5.1, September 12th, 2024, or remove the date and revision number from the reference.
Update any other references as appropriate if new revisions are published.

Proposed Response Response Status O

Cl 45 SC 45.2.1.213b P90 L51 # 164

He, Xiang Huawei

Comment Type TR Comment Status X

Add MDIO register for newly added "align_status" variable, see 177.4.1 and 177.11. It might be confusing to put it in 45.2.1.213b since the registers now in the table are for Inner FEC receive direction. We could

SuggestedRemedy

In 45.2.1.213b, add a new row above "Inner FEC lock 7" for the "align_status" in 177.4.1 and 177.11:
Bit(s) / Name / Description / R/W
1.2401.8 / align_status / alignment marker lock status for Inner FEC transmit direction / RO
And change "1.2401.15:8" to "1.2401.15:9" in the first row.

Proposed Response Response Status O

Cl 45 SC 45.2.1.213c P91 L31 # 122

Brown, Matt Alphawave Semi

Comment Type E Comment Status X

Use of possessive, e.g., lane 0's Inner FEC total bits register, is not necessary or appropriate for a technical document. It is sufficient and appropriate to use "lane 0 Inner FEC total bits registers".

SuggestedRemedy

Replace "lane 0's" with "lane 0" here and 4 other places in Clause 45.

Proposed Response Response Status O

Cl 45 SC 45.2.1.213g P93 L44 # 4

Bruckman, Leon Nvidia

Comment Type TR Comment Status X

In Table 45-177g bins 2 and 3 shall also be described

SuggestedRemedy

In Table 45-177g show registers 1.2416, 1.2417, 1.2418 and 1.2419 for lane 0 error bins 2 and 3 (same structure as for error bin 1)

Proposed Response Response Status O

Cl 45 SC 45.2.3.1 P94 L17 # 35

KABRA, LOKESH SYNOPSYS

Comment Type TR Comment Status X

Include update to 3.0.5:2 "Speed Selection" values corresponding to 800 Gb/s and 1.6 Tb/s in Table 45-211-- PCS control 1 register bit definitions

SuggestedRemedy

Modify 3.0.5:2 bit field "Speed selection" description

Existing
1 1 x x = Reserved

Proposed
1 1 1 x = Reserved
1 1 0 1 = 1.6 Tb/s
1 1 0 0 = 800 Gb/s

Similar changes to be done in 4.0.5:2 and 5.0.5:2 bit field descriptions.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 45 SC 45.2.3.1 P94 L18 # 1 [REDACTED]
 Marris, Arthur Cadence Design Systems
 Comment Type T Comment Status X
 PCS control 1 register speed selection bits need to be updated for 1.6 Tb/s. Similar issue for PHY and DTE XS control 1 registers
 SuggestedRemedy
 Bring Tables 45-234, 45-315, and 45-340 and update as necessary. Also after maintenance request https://www.ieee802.org/3/maint/requests/maint_1437.pdf is considered include 800 Gb/s selection also.
 Proposed Response Response Status O

CI 45 SC 45.2.3.2.7 P94 L17 # 36 [REDACTED]
 KABRA, LOKESH SYNOPSISYS
 Comment Type T Comment Status X
 Update "PCS receive link status (3.1.2)" description
 SuggestedRemedy
 Existing
 When a 10/25/40/50/100/200/400GBASE-R,
 Proposed
 When a 10/25/40/50/100/200/400/800GBASE-R, 1.6TBASE-R,
 Second change :
 Two instances of "(3.7.3:0)" to be corrected to "(3.7.4:0)".
 Proposed Response Response Status O

CI 45 SC 45.2.3.6.1 P94 L44 # 37 [REDACTED]
 KABRA, LOKESH SYNOPSISYS
 Comment Type T Comment Status X
 Include update to "PCS type selection" values corresponding to 800 Gb/s and 1.6 Tb/s in Table 45-214-- PCS control 2 register bit definitions
 SuggestedRemedy
 Modify 3.7.4:0 bit field "PCS type selection" description
 Existing
 1 0 1 x x = Reserved
 Proposed
 1 0 1 1 x = Reserved
 1 0 1 0 1 = Select 1.6TBASE-R PCS type
 1 0 1 0 0 = Select 800GBASE-R PCS type
 Proposed Response Response Status O

CI 45 SC 45.2.3.8 P94 L45 # 38 [REDACTED]
 KABRA, LOKESH SYNOPSISYS
 Comment Type T Comment Status X
 Add capability field for 800GBASE-R & 1.6TBASE-R in this register
 SuggestedRemedy
 In Table 45-216-- PCS Status 3 register bit definitions,
 Existing
 3.9.15:8 Reserved Value always 0
 Proposed
 3.9.15:10 Reserved Value always 0
 3.9.15:9 1.6TBASE-R capable 1 = PCS is able to support 1.6TBASE-R PCS type
 0 = PCS is not able to support 1.6TBASE-R PCS type
 3.9.15:8 800GBASE-R capable 1 = PCS is able to support 800GBASE-R PCS type
 0 = PCS is not able to support 800GBASE-R PCS type
 Proposed Response Response Status O

Cl 45 SC 45.2.3.8.1a P94 L46 # 39
KABRA, LOKESH SYNOPSIS
Comment Type T Comment Status X
Add new subsection
SuggestedRemedy
45.2.3.8.1a 1.6TBASE-R capable (3.9.9)
When read as a one, bit 3.9.9 indicates that the PCS is able to support the 1.6TBASE-R PCS type. When read as a zero, bit 3.9.9 indicates that the PCS is not able to support 1.6TBASE-R PCS type
Proposed Response Response Status O

Cl 45 SC 45.2.3.8.1b P94 L47 # 40
KABRA, LOKESH SYNOPSIS
Comment Type T Comment Status X
Add new subsection
SuggestedRemedy
45.2.3.8.1b 800GBASE-R capable (3.9.8)
When read as a one, bit 3.9.8 indicates that the PCS is able to support the 800GBASE-R PCS type. When read as a zero, bit 3.9.8 indicates that the PCS is not able to support 800GBASE-R PCS type
Proposed Response Response Status O

Cl 45 SC 45.2.3.15.1 P94 L48 # 41
KABRA, LOKESH SYNOPSIS
Comment Type T Comment Status X
Update last line of 45.2.3.15.1
SuggestedRemedy
Existing
"100GBASE-R, and in 119.3 for 200G/400GBASE-R."
Proposed
"100GBASE-R, in 119.3 for 200G/400GBASE-R, in 172.3 for 800GBASE-R, and in 175.8 for 1.6TBASE-R.
Similar update required in 45.2.4.12.1, 45.2.5.12.1
Proposed Response Response Status O

Cl 45 SC 45.2.4 P97 L37 # 3
Marris, Arthur Cadence Design Systems
Comment Type T Comment Status X
A control bit needs to be added for the variable "PHY_XS_enhanced_ptp_accuracy_enable" listed in "Table 171-2—MDIO PHY 800GXS to Clause 172 control variable mapping"
SuggestedRemedy
Create a new "TimeSync PHY XS configuration" register at location 4.1813 with a "PHY XS enhanced PTP accuracy enable" bit. Add an ability bit for for enhanced PTP accuracy in "TimeSync PHY XS capability (Register 4.1800)".
Proposed Response Response Status O

Cl 45 SC 45.2.4.13 P97 L34 # 42
KABRA, LOKESH SYNOPSIS
Comment Type T Comment Status X
Update second line of paragraph
SuggestedRemedy
Existing
"This register is only required when the 200/400GBASE-R capability is supported. The test-pattern methodology is described in 119.2.4.9."
Proposed
"This register is required when the 200/400GBASE-R or 800GBASE-R or 1.6TBASE-R capability is supported. The test-pattern methodology is described in 119.2.4.9 for 200/400GBASE-R, in 172.2.4.11 for 800GBASE-R, and in 175.2.4.11 for 1.6TBASE-R."
Similar update required in 45.2.5.13.
Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 116 SC 116.3.3.3 P134 L51 # 5
 Bruckman, Leon Nvidia
 Comment Type E Comment Status X
 Text can be improved
 SuggestedRemedy
 Change: "and, for physical layer implementations that use the ILT function defined in Annex 178B, to indicate the ILT status."
 to: "and, to indicate the ILT status for physical layer implementations that use the ILT function defined in Annex 178B."
 Proposed Response Response Status O

Cl 116 SC 116.3.3.4 P135 L42 # 6
 Bruckman, Leon Nvidia
 Comment Type E Comment Status X
 Text can be improved
 SuggestedRemedy
 Change: "and, for physical layer implementations that use the ILT function defined in Annex 178B, to indicate the ILT status."
 to: "and, to indicate the ILT status for physical layer implementations that use the ILT function defined in Annex 178B."
 Proposed Response Response Status O

Cl 116 SC 116.3.3.4.1 P136 L11 # 7
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 Typo: "the lower higher sublayer"
 SuggestedRemedy
 Change: "the lower higher sublayer"
 to: "the next lower sublayer"
 Proposed Response Response Status O

Cl 119 SC 119.2.6.2.1 P148 L17 # 136
 Brown, Matt Alphawave Semi
 Comment Type T Comment Status X
 SIGNAL_OK parameter is now defined with four parameters {OK, IN_PROGRESS, READY, FAIL} rather than two {OK, FAIL}. The signal_ok variable value is not defined for the two new values, only for OK and FAIL.
 SuggestedRemedy
 In 119.2.6.2.1 in the definition of the signal_ok variable...
 Replace "It is true if the value was OK and false if the value was FAIL."
 With: "It is true if the value was OK and false otherwise."
 Proposed Response Response Status O

Cl 169 SC 169.3.2 P162 L34 # 59
 Opsasnick, Eugene Broadcom
 Comment Type TR Comment Status X
 In Figure 169-3, the block labeled "800GBASE-R n:32 PMA" immediately above the 800GBASE-R PMD should be a "32:n PMA" (not n:32).
 SuggestedRemedy
 Change "800GBASE-R n:32 PMA" to "800GBASE-R 32:n PMA" on line 34 of page 162.
 Note that the "n" should also be in italics.
 Consider changing it to "800GBASE-R 32:p PMA" and add a definition of p under the figure to be consistent with Figure 174-3 on page 217.
 Proposed Response Response Status O

Cl 170 SC 170.1 P168 L13 # 8
 Bruckman, Leon Nvidia
 Comment Type ER Comment Status X
 Missing "the"
 SuggestedRemedy
 Change: "and 1.6 Tb/s Media Independent"
 to: "and the 1.6 Tb/s Media Independent"
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 171 SC 171.1.1 P177 L9 # 166

Huber, Thomas Nokia
 Comment Type T Comment Status X

The "can be" was changed to "may be" in D1.2, but the corresponding statement for 800G at the bottom of the preceding page is still "can be", making the wording inconsistent between the two rates.

SuggestedRemedy

Other similar extender sublayer clauses also use "can be". Change the "may be" back to "can be".

Proposed Response Response Status O

Cl 171 SC 171.6.1 P183 L48 # 53

Opsasnick, Eugene Broadcom
 Comment Type TR Comment Status X

The cross-reference to the definition of FEC_degraded_SER and rx_local_degraded for DTE 1.6TXS is wrong. It should not be 175.2.6.2.2, rather it should be 175.2.5.3 and 175.2.5.5.

SuggestedRemedy

Change: "... defined in 175.2.6.2.2 for DTE1.6TXS, ..."
 To: "... defined in 175.2.5.3 and 175.2.5.5 for DTE 1.6TXS, ..."
 with updates of the hyperlinks to the correct subclauses.

Proposed Response Response Status O

Cl 171 SC 171.6a P184 L17 # 379

Slavick, Jeff Broadcom
 Comment Type E Comment Status X

Enhanced PTP should likley come after the "normal" TimeSync function of path delay information.

SuggestedRemedy

Flip-flop Enhanced PTP accuracy and Path data delay for time synchronization

Proposed Response Response Status O

Cl 171 SC 171.6a P184 L18 # 381

Slavick, Jeff Broadcom
 Comment Type T Comment Status X

The opening paragraph is not accurately representing the Enhanced PTP accuracy functionality.

SuggestedRemedy

Update the first paragraph to read:
 If the sublayer below the 800GXS is an 800GBASE-ER1 PCS, the enhanced PTP accuracy feature provides the indication of where in the 800GMII stream 800GBASE-R alignment markers once existed. This indicator allows for subsequent insertion of 800GBASE-R alignment markers into the same spot in the data stream.

Proposed Response Response Status O

Cl 171 SC 171.6a P184 L36 # 382

Slavick, Jeff Broadcom
 Comment Type T Comment Status X

The insertion of AMs is defined to occur with RAML, but the PCSs are built upon this occurring as the first N 257b words of a RS-FEC, so the PHY XS needs to align it's RS-FEC formation around the RAML not just stuff the AMs anywhere within a RS-FEC codeword.

SuggestedRemedy

Change: "When enhanced PTP accuracy is enabled, the PHY 800GXS inserts the 800GBASE-R PCS alignment markers based on the RAML signal. If the enhanced PTP feature is disabled, the PHY 800GXS inserts the 800GBASE-R PCS alignment markers as defined in 172.2.4.6."
 To: "When enhanced PTP accuracy is enabled, the PHY 800GXS inserts the 800GBASE-R PCS alignment markers based on the RAML signal and waits for the first RAML after reset removal to begin its encoding process. When the enhanced PTP feature is disabled the alignment marker insertion process operates normally, see 172.2.4.6."

Proposed Response Response Status O

Cl 171 SC 171.6b P184 L47 # 368

Slavick, Jeff Broadcom

Comment Type T Comment Status X

Support of the "optional" path delay information should be presented as the first information of this section not the last.

SuggestedRemedy

Change 171.6b to be:
 171.6b Path data delay (optional)
 171.6b.1 PHY XS path data delay
 Support for the optional path data delay information is indicated by the PHY XS status variables PHY_XS_delay_ns_TX_ability, PHY_XS_delay_subns_TX_ability, PHY_XS_delay_ns_RX_ability, and PHY_XS_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported and the PCS_timesync_multilane_ability variable is true (see 90.7.1), the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) is the start of the set of interleaved RS-FEC codewords, corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
 — PHY_XS_delay_ns_TX_max, PHY_XS_delay_subns_TX_max
 — PHY_XS_delay_ns_TX_min, PHY_XS_delay_subns_TX_min
 — PHY_XS_delay_ns_RX_max, PHY_XS_delay_subns_RX_max
 — PHY_XS_delay_ns_RX_min, PHY_XS_delay_subns_RX_min

171.6b.2 DTE XS path data delay
 Support for the optional path data delay information is indicated by the DTE XS status variables DTE_XS_delay_ns_TX_ability, DTE_XS_delay_subns_TX_ability, DTE_XS_delay_ns_RX_ability, and DTE_XS_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported and the PCS_timesync_multilane_ability variable is true (see 90.7.1), the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) is the start of the set of interleaved RS-FEC codewords, corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
 — DTE_XS_delay_ns_TX_max, DTE_XS_delay_subns_TX_max
 — DTE_XS_delay_ns_TX_min, DTE_XS_delay_subns_TX_min
 — DTE_XS_delay_ns_RX_max, DTE_XS_delay_subns_RX_max
 — DTE_XS_delay_ns_RX_min, DTE_XS_delay_subns_RX_min

Proposed Response Response Status O

Cl 171 SC 171.8 P187 L17 # 167

Huber, Thomas Nokia

Comment Type T Comment Status X

The additional row for the enhanced_ptp_accuracy_enable does is out of place, since that function is not part of clause 172, but instead is part of 186.

SuggestedRemedy

Either insert a new table for PHY 800GXS to Clause 186 control variable mapping with the enhanced_ptp_accuracy_enable information, or, if a separate table with a single row is not desirable, change the title of Table 171-2 to refer to add "and Clause 196", change the last column in the same way, and include in each row the clause number along with the variable name.

Proposed Response Response Status O

Cl 171 SC 171.9 P195 L0 # 380

Slavick, Jeff Broadcom

Comment Type T Comment Status X

No PICS for TimeSync functions

SuggestedRemedy

Add PICS similar to Table 175-4 to Clause 171 but also add in the Enhanced PTP accuracy

Proposed Response Response Status O

Cl 171 SC 171.9 P195 L1 # 322

Nicholl, Gary Cisco Systems

Comment Type TR Comment Status X

Need to add a PICS item to address optional support for Enhanced PTP accuracy (see 171.6a).

SuggestedRemedy

Update PICS to add an item for optional support of Enhanced PTP accuracy (referencing 171.6a)

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 171 SC 171.9 P195 L1 # 321

Nicholl, Gary Cisco Systems

Comment Type TR Comment Status X

Need to update PICS to include path data delay for time synchronization (see 171.6b) . See 175.9.4.7 as an example for what was done for the 1.6TBASE-R PCS in Clause 175.

SuggestedRemedy

Updated PICS to include path data delay for time synchronization. See 175.9.4.7 as an example.

Proposed Response Response Status O

Cl 171 SC 171.9.4.1 P196 L50 # 168

Huber, Thomas Nokia

Comment Type T Comment Status X

The PTP accuracy feature should be a PICS item that is conditional on being connected to an 800GBASE-ER1 PCS (i.e., we want all implementations to have the feature available; the MDIO variable can turn it on or off if users prefer to not use it).

SuggestedRemedy

Add a PICS item for 'supports the enhanced PTP accuracy' feature.

Proposed Response Response Status O

Cl 172 SC 172.1.6 P204 L48 # 52

Opsasnick, Eugene Broadcom

Comment Type TR Comment Status X

In Figure 172-2 (the block diagram of the 800G PCS), the lower interface says "PMA", but should be "PCS".

SuggestedRemedy

Change:"Service Interface below the PMA"
To: "Service Interface below the PCS"

Proposed Response Response Status O

Cl 174 SC 174.3.2 P217 L31 # 60

Opsasnick, Eugene Broadcom

Comment Type TR Comment Status X

In Figure 174-3, the signal "PMA:IS_SIGNAL.request" from the 1.6TBASE-R PCS to the 1.6TBASE-R 16:p PMA should be removed. The PCS does not have this output - see Figure 175.2 on page 226. No relevant PCS has this output at the service interface below the PCS - see also Fig. 172-2 (on page 198 of 802.3df-2014) and Fig. 119-2 (on page 4837 of 802.3-2022). See also the similar extender figure 169-3 for 800GMII on page 162.

SuggestedRemedy

Remove "PMA:IS_SIGNAL.request" out of the 1.6TBASE-R PCS in Figure 174-3.

Proposed Response Response Status O

Cl 174 SC 174.3.2 P218 L20 # 61

Opsasnick, Eugene Broadcom

Comment Type E Comment Status X

In Figure 174-4 (1.6T Inter-sublayer interfaces with Inner FEC), there is no AUI. The Inner FEC will (almost) always be in an optical module below an AUI connection to a host. It would be better to show the Inner FEC below an AUI in this figure since the layer stack shown, while logically correct, will never actually be used.

SuggestedRemedy

Add a "1.6T BASE-R 8:8 PMA" between the "1.6T BASE-R 16:8 PMA" on line 14 and the "1.6TBASE-R Inner FEC" on line 20. And then add the necessary inter-layer signals on the AUI connection between the two PMAs.

Proposed Response Response Status O

Cl 174 SC 174.4 P219 L28 # 44

Opsasnick, Eugene Broadcom

Comment Type TR Comment Status X

Table 174-4 has an incorrect cross-reference to the PCS delay constraints

SuggestedRemedy

Change the cross-reference from "175.4" to be "175.5".

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 174A SC 174A.6.1.1 P642 L22 # 77

Ran, Adeo Cisco Systems, Inc.

Comment Type ER Comment Status X

The counter variable names tbcoun and tbtcount are obscure and too similar to each other, making the text difficult to parse. There is no need to use such abbreviated names. The text would be clearer with variable naming similar to the PCS counter names e.g. in 175.2.5.3.

SuggestedRemedy

Rename tbcoun(k) to test_block_error_bin(k) and tbtcount to test_block_counter.

Apply elsewhere as necessary.

Proposed Response Response Status O

CI 174A SC 174A.6.1.4 P643 L31 # 78

Ran, Adeo Cisco Systems, Inc.

Comment Type T Comment Status X

The description of the process can be simplified by initializing the distribution to that of BER_added (step c) and then iterating with i from 0 to p-1 (instead of treating i=0 as initial value). This would remove two steps (a and d) and yield the same result with fewer intermediate variables..

SuggestedRemedy

Rewrite the process as suggested.

Proposed Response Response Status O

CI 174A SC 174A.6.1.5 P644 L1 # 150

Dudek, Mike Marvell

Comment Type TR Comment Status X

This subsection describes a method that only works for the complete PCS to PCS link and should not be included in 174A.6 whose title is "inter-sublayer links" and whose first sentence says "This subclause defines test methods for an ISL (see 178B.2) with 200 Gb/s per lane signaling between a pair of PMAs"

SuggestedRemedy

Separate this procedure into a separate subclause (174A.7 renumbering the other subclauses). Rewrite the section to use FEC symbols and the code-word error counters rather than just 10-bit symbols.

Proposed Response Response Status O

CI 174A SC 174A.6.1.5 P644 L3 # 132

Brown, Matt Alphawave Semi

Comment Type T Comment Status X

The methodology for measuring block error ratio using a PCS is out of date with changes made to the test methodology using a PMA as defined in 174A.6.1.3 and 174A.6.1.4.

SuggestedRemedy

A contribution to address this will be provided.

Proposed Response Response Status O

CI 174A SC 174A.6.1.5 P644 L5 # 210

Healey, Adam Broadcom Inc.

Comment Type T Comment Status X

A method for calculating block error ratio using PCS-based measurements has not been defined.

SuggestedRemedy

A contribution will be provided with a detailed proposal for a calculation procedure.

Proposed Response Response Status O

CI 174A SC 174A.6.1.5 P644 L14 # 79

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The process for block error ratio using the PCS should be similar to the one in 174A.6.1 (analytic calculation rather than injecting real errors) but using the PCS codeword bin counters instead.

The process starts with the current step a, continues like the one of 174A.6.1.1 steps d-e (but using the FEC bin counters and total counter instead of the PMA ones) and step f to calculate the (single) histogram. Then it can continue using either 174A.6.1.3 (mask) or 174A.6.1.4 (convolution of the single histogram with a BER_added calculated histogram).

SuggestedRemedy

Rewrite the process as suggested.

Proposed Response Response Status O

Cl 174A SC 174A.6.1.5 P644 L30 # 151

Dudek, Mike Marvell
 Comment Type TR Comment Status X

The PCS is working on a per interface level rather than a per lane basis therefore applying noise to each of the n lanes one at a time will not result in there being 16 or more errored symbols in the 544 symbols (as three quarter of these 16 symbols will be distributed across lanes that would have no or very few errors).

SuggestedRemedy

If another comment is accepted to use FEC symbols and the code-word error counters replace this note with "Note- for this test method noise must be added to all the lanes for the test." If the other comment is not accepted then better describe what "streams" are i.e "streams of bits on each physical lane" and make the blocks being 544 symbols on each lane. The Block error ratio will then be the average of NE/NT of each of the lanes.

Proposed Response Response Status

Cl 174A SC 174A.8 P645 L38 # 81

Ran, Adeo Cisco Systems, Inc.
 Comment Type TR Comment Status X

As the editor's note indicates, the AUIs within an extender can have much larger BER while still meeting the BERtotal of the extender.

The suggested remedy is to divide the BERtotal between C2C and C2M in a ratio of 1:3, similar to that of a PHY-to-PHY link.

SuggestedRemedy

In Table 174A-3, change "BER per sublayer" values to 5.53e-5 for C2C and 1.66e-4 for C2M.

Add text in annexes 176C and 176D to address the Extender case.

Proposed Response Response Status

Cl 174A SC 174A.8 P645 L9 # 152

Dudek, Mike Marvell
 Comment Type TR Comment Status X

The BER allocated per sublayer in the 200G C2C is 0.08e-4. However the allocation for the 100G or lower C2C AUI that can be part of the Phy is 0.1e-4.

SuggestedRemedy

Either change the allocation for the C2C AUI's to 0.1e-4 reducing the PMD allocation to 2.24e-4 for the optical PHYs and 2.72e-4 for the electrical PHYs and change the BER added in the optical clauses to 6.8e-5 for PMA to PMA and 3.4e-5 for the measurements at the PCS or Add a footnote to the use of clauses 120B and 120D and 120F in Table 180-1 and the equivalent tables in the other PMD clauses (178,179, 181,etc) Stating. "Useable without restriction in extenders. If 120B, 120D or 120F C2C links are used in the main link the DER0 used in the common calculation for the channel is reduced from 1e-5 to 0.67e-5.

Proposed Response Response Status

Cl 175 SC 175.5 P244 L4 # 116

Brown, Matt Alphawave Semi
 Comment Type E Comment Status X

Several instances of acronym "BT" with defining this acronym. Typically, in this draft the it "bit times (BT)".

SuggestedRemedy

change "BT" to "bit times (BT)" also, in 184.7 and 186.5

Proposed Response Response Status

Cl 174A SC 174A.8 P645 L35 # 80

Ran, Adeo Cisco Systems, Inc.
 Comment Type ER Comment Status X

In Table 174A-3 the last column has "in a PHY" but it is about an xMII extender.

SuggestedRemedy

Change to "in an xMII Extender".

Proposed Response Response Status

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 175 SC 175.6 P244 L10 # 369

Slavick, Jeff Broadcom

Comment Type T Comment Status X

Support of the "optional" path delay information should be presented as the first information of this section not the last.

SuggestedRemedy

Change 175.6 to be:

175.6 Path data delay (optional)

Support for the optional path data delay information is indicated by the status variables PCS_delay_ns_TX_ability, PCS_delay_subns_TX_ability, PCS_delay_ns_RX_ability, and PCS_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported and the PCS_timesync_multilane_ability variable is true (see 90.7.1), the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) is at the start of the set of four interleaved RS-FEC codewords, longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:

- PCS_delay_ns_TX_max, PCS_delay_subns_TX_max
- PCS_delay_ns_TX_min, PCS_delay_subns_TX_min
- PCS_delay_ns_RX_max, PCS_delay_subns_RX_max
- PCS_delay_ns_RX_min, PCS_delay_subns_RX_min

Proposed Response Response Status O

Cl 175 SC 175.8 P245 L9 # 43

KABRA, LOKESH SYNOPSIS

Comment Type E Comment Status X

Incorrect Variable reference given in Table 175--3 for "loopback"

SuggestedRemedy

Change 175.3 to 175.4

Proposed Response Response Status O

Cl 176 SC 176.1.3 P253 L34 # 373

Slavick, Jeff Broadcom

Comment Type E Comment Status X

Eleven items is a bit more than what I'd considered to be several.

SuggestedRemedy

Change "Several terms" to "The following terms"

Proposed Response Response Status O

Cl 176 SC 176.1.4 P254 L47 # 45

Opsasnick, Eugene Broadcom

Comment Type TR Comment Status X

To convert from a AUI-2 to a AUI-1, a xBASE-R BM-PMA must be placed next to a xBASE-R SM-PMA.

SuggestedRemedy

Change: "... placed next to a 200GAUI-1 8:1 PMA."

To: "... placed next to a 200GBASE-R 8:1 PMA."

Proposed Response Response Status O

Cl 176 SC 176.1.4 P255 L1 # 372

Slavick, Jeff Broadcom

Comment Type T Comment Status X

Forwarding of the clock is a necessary function for the PMA regardless of ILT. Since the PMA does not do any PPM compensation.

SuggestedRemedy

Remove the last paragraph of 176.1.4 that begins with "In order to support the inter-sublayer link training"

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 176 SC 176.1.4 P255 L1 # 26
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 ILT does not require the clock to be passed through the PMA. The mission data requires it. ILT operates with local clock.
 SuggestedRemedy
 Delete: "In order to support the inter-sublayer link training (ILT) function,"
 Proposed Response Response Status O

Cl 176 SC 176.1.5 P255 L50 # 46
 Opsasnick, Eugene Broadcom
 Comment Type TR Comment Status X
 Footnote (e) to Table 176-2 mentions the PMA to connect to a 800GBASE-LR1 Inner FEC is "For 800GBASE-R 8:16 only". But this looks like the wrong ratio of lanes for the 800GBASE-R PMA.
 SuggestedRemedy
 Change: "For 800GBASE-R 8:16 only"
 To: "For 800GBASE-R 4:32 only."
 Proposed Response Response Status O

Cl 176 SC 176.2 P256 L47 # 374
 Slavick, Jeff Broadcom
 Comment Type E Comment Status X
 The last several paragraphs of 176.2 are dealing with specific types of PMAs and the SIGNAL_OK function. We have 3 different types of PMAs whose functionality we do group into different sub-clauses later on, so making each its own sub-clause of 176.2 I think would organize it better.
 SuggestedRemedy
 Insert this heading "176.2.1 PMA service interface for m:n PMA" before the paragraph that begins with "In the transmit direction, the m:n PMAs"
 Insert this heading "176.2.2 PMA service interface for n:m PMA" before the paragraph that begins with "In the transmit direction, the n:m PMAs"
 Insert this heading "176.2.3 PMA service interface for n:n PMA" before the paragraph that begins with "In the transmit direction, the n:n PMAs"
 Insert this heading "176.2.4 SIGNAL_OK for the PMA service interface" before the paragraph that begins with "The PMA receives signal status"
 Proposed Response Response Status O

Cl 176 SC 176.2 P257 L15 # 375
 Slavick, Jeff Broadcom
 Comment Type T Comment Status X
 Using one variable name "SIGNAL_OK" when we have two copies of it for each Service interface and we have two service interfaces is going to be very confusing. We don't use just symbol for the data, we use tx_symbol and rx_symbol.
 SuggestedRemedy
 Using editorial license.

In Table 176-5 change the headings to be:
 inst.IS_SIGNAL.indication SIGNAL_OK_rx
 PMA.IS_SIGNAL.indication SIGNAL_OK_rx

In Table 176-6 change the headings to be:
 PMA.IS_SIGNAL.request SIGNAL_OK_tx
 inst.IS_SIGNAL.request SIGNAL_OK_tx

In 176.2 in the 2nd paragraph update IS_SIGNAL primitives to be as follows:
 PMA:IS_SIGNAL.request(SIGNAL_OK_tx)
 PMA:IS_SIGNAL.indication(SIGNAL_OK_rx)

In 176.2 in the 2nd to last paragraph (above Table 176-5) change the last two sentences to be: The SIGNAL_OK_rx parameter at the client interface is set according to Table 176-5, for n:n PMAs the parameter is set as if all_locked_demux<y> is true.

In 176.3 in the 2nd paragraph update IS_SIGNAL primitives to be as follows:
 inst:IS_SIGNAL.request(SIGNAL_OK_tx)
 inst:IS_SIGNAL.indication(SIGNAL_OK_rx)

In 176.3 in the 2nd to last paragraph (above Table 176-5) change the last two sentences to be: The SIGNAL_OK_tx parameter at the interface below the PMA is set according to Table 176-6, for n:n PMAs the parameter is set as if align_status_mux is true.

In 176.4.4.2.1 in the signal_ok_mux definition change "SIGNAL_OK" to "SIGNAL_OK_tx/rx"

In 176.4.4.2.1 in the signal_ok_demux definition change "SIGNAL_OK" to "SIGNAL_OK_tx/rx"

Proposed Response Response Status O

Cl 176 SC 176.2 P257 L30 # 47

Opsasnick, Eugene Broadcom

Comment Type T Comment Status X

In Table 176-5, the middle column for the value of align_status_mux or all_locked_demux is listed as "N/A" for three of the rows. "N/A", not-applicable, implies there is no value or the status variable does not exist in this case. But the status variables are always there and in these cases, when the SIGNAL_OK input value is (not OK), they would have the value 'false'. But when the input SIGNAL_OK has a value of (not OK), the output does not really depend on the status variable, and it is a "don't care" for the calculation of the output IS_SIGNAL.indication.

SuggestedRemedy

In Table 176-5, Change the three entries of "N/A" for align_status_mux or all_locked_demux to "don't care" (or "false"). The same change from "N/A" to "don't care" should be applied to Table 176-6 on page 258.

Proposed Response Response Status O

Cl 176 SC 176.2 P257 L39 # 377

Slavick, Jeff Broadcom

Comment Type E Comment Status X

Noting that there is a clock propagation in addition to the actual listed primitives should occur right after we list out those parameters and before we fully define them.

SuggestedRemedy

Move the last paragraph of 176.2 and 176.3 to be after the bullet list of interface primitives.

Proposed Response Response Status O

Cl 176 SC 176.3 P258 L26 # 249

Shrikhande, Kapil Marvell

Comment Type TR Comment Status X

The subclause is about the service interface below the PMA. Therefore, the PMA:IS_SIGNAL.indication primitive should be inst:IS_SIGNAL.indication, and the PMA:IS_SIGNAL.request primitive should be inst:IS_SIGNAL.request.

SuggestedRemedy

Replace PMA with inst as outlined in the comment.

Proposed Response Response Status O

Cl 176 SC 176.3 P258 L34 # 248

Shrikhande, Kapil Marvell

Comment Type TR Comment Status X

In Table 176-6, when the sublayer above the PMA is a PCS, there is no PMA:IS_SIGNAL.request input (no PCS drives this signal). The table does not cover the common case of an m:n PMA with a PCS above.

SuggestedRemedy

Add two additional rows to the table with N/A in the left most column (no input value), and determine the output value of inst:IS_SIGNAL.request SIGNAL_OK signal depending only on the value of the align_status_mux variable. Alternative would be to have the PCS drive a signal to the PMA.

Proposed Response Response Status O

Cl 176 SC 176.3 P258 L34 # 56

Opsasnick, Eugene Broadcom

Comment Type TR Comment Status X

Table 176-6 specifies how to set the output inst:IS_SIGNAL.request(SIGNAL_OK) based on the input PMA:IS_SIGNAL.request(SIGNAL_OK) and the variable align_status_mux or all_locked_demux. However, when the sublayer above the PMA is a PCS, there is no PMA:IS_SIGNAL.request input.

SuggestedRemedy

Suggest adding two rows to Table 176-6 to account for the case where PMA:IS_SIGNAL.request input is not present. Add two rows with N/A for the IS_SIGNAL.request(SIGNAL_OK) input, and the output is based only on the internal variable being true or false. Something like:

```
New row 1: | N/A | true | OK |
           +-----+-----+-----+
New row 2: | N/A | false | READY |
```

Proposed Response Response Status O

Cl 176 SC 176.3 P260 L26 # 57

Opsasnick, Eugene Broadcom

Comment Type TR Comment Status X

In figure 176-2 the signal "all_locked_demux" between the Symbol demultiplexing and Alignment marker lock blocks should be "all_locked_demux<0:(n-1)>" since this variable is defined as an indexed variable later in 176.4.4.2.1 and all of the individual indexed values are needed. However, a better name for this variable might be "lane_locked_demux<0:(n-1)>" (see editorial comments submitted separately via pdf).

SuggestedRemedy

Change "all_locked_demux" to "lane_locked_demux<0:(n-1)>" in Figure 176-2 and redefine all_locked_demux as "true when lane_locked_demux<y> is true for all y."

Proposed Response Response Status O

Cl 176 SC 176.4.1 P260 L4 # 55

Opsasnick, Eugene Broadcom

Comment Type TR Comment Status X

In figure 176-2 near line 4, there is an input called PMA:IS_SIGNAL.request. This input is required if the sublayer above the PMA is another PMA or an AUI. However, when the sublayer above the PMA is a PCS, this input is not present. All possible PCS's, 200G/400G PCS (CL 119), 800G PCS (CL 172), and 1.6T PCS (CL 175) do not have this output at the service interface below the PCS.

SuggestedRemedy

A notation in Figure 176-2 should be added that PMA:IS_SIGNAL.request is not present when the sublayer above the PMA is a PCS or DTE XS.

Proposed Response Response Status O

Cl 176 SC 176.4.2.6 P268 L27 # 58

Opsasnick, Eugene Broadcom

Comment Type T Comment Status X

The PAM4 encode function should specify that PAM4 symbols be aligned to RS-FEC symbol boundaries. When the 2-bit PAM4 symbols are aligned to the 10-bit RS-FEC, there are exactly 5 PAM4 symbols within each RS-FEC symbol. However, if they are not aligned, then each RS-FEC symbol would contain the second bit of one PAM4 symbol, followed by the 8 bits of 4 PAM4 symbols, followed by the first bit of the next PAM4 symbol. The unaligned arrangement makes the RS-FEC error performance analysis more complicated since there is an unequal probability of the first and second bits of a PMA4 symbol being in error (RS-FEC performance for the symbol muxing 200G/lane interfaces has so far only been done for the "aligned case"). The aligned case should already be the norm for most or all implementations. Specifying it this way should just guarantee the FEC performance is as already studied, and receiver implementations may also take advantage of this guarantee.

SuggestedRemedy

In subclause 176.4.2.6 "PAM4 encode" and 176.4.3.6 "PAM4 encode", add a requirement that the PAM4 symbols must align to the RS-FEC symbols such that each RS-FEC symbol contains 10 bits from exactly 5 full PAM4 symbols.

A similar requirement should be also be added to the PAM4 encoding description in 177.4.8. In this case, the PAM4 symbols should align with the start of a block of 8x Inner FEC codewords (see Fig. 177-6) after the circular shift.

Proposed Response Response Status O

Cl 176 SC 176.4.4.2.1 P271 L10 # 48

Opsasnick, Eugene Broadcom

Comment Type TR Comment Status X

The definition of the variable "reset" refers to another variable "PMA_reset", but PMA_reset is not defined anywhere.

SuggestedRemedy

Add the definition of PMA_reset to the list of variables just prior to reset. PMA_reset = "Boolean variable that is true when set by a management entity and is false otherwise."

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 176 SC 176.4.4.2.1 P271 L45 # 376

Slavick, Jeff Broadcom

Comment Type E Comment Status X

The mapping of SIGNAL_OK to signal_ok_*mux is an active mapping of the service interface to status value.

SuggestedRemedy

Change "It is true if the value was OK" to "It is true when the value is OK" in both signal_ok_mux and signal_ok_demux definitions.

Proposed Response Response Status O

Cl 176 SC 176.4.4.2.1 P271 L50 # 247

Shrikhande, Kapil Marvell

Comment Type TR Comment Status X

In the SM-PMA demultiplexer, there is a boolean variable all_locked_demux<y> that is set to true when all PCSs within an input lane are locked. However in addition, there should be a composite variable that is set to true when all input lanes of the PMA have achieved lock.

SuggestedRemedy

Add boolean variable all_locked_demux. This variable is set to true when all_locked_demux<y> is true for all y = 0 to (n-1), and false otherwise, where n is the number of input lanes in the demultiplexing direction.

Proposed Response Response Status O

Cl 176 SC 176.7.1.2 P280 L13 # 49

Opsasnick, Eugene Broadcom

Comment Type T Comment Status X

The third paragraph of 176.7.1.2 describes four independent enables for precoding on four interfaces, TX input/output and RX input/output. The last sentence of this paragraph states "By default, precoding on the Tx output or Rx output is disabled." But the default value for TX input and RX input is not mentioned.

SuggestedRemedy

If the default value is disabled, then change the last sentence to include the default value for all 4 enables. "By default precoding is disabled on the Tx input, Tx output, Rx input and Rx output." or maybe "By default, precoding is disabled on all interfaces."

Proposed Response Response Status O

Cl 176 SC 176.7.2 P280 L33 # 50

Opsasnick, Eugene Broadcom

Comment Type TR Comment Status X

It is stated that "During local loopback, the PMA continues to propagate data in the Tx direction and drives the Tx service interface below the PMA.". It is also stated in 176.7.3 on line 47 on the same page that "During remote loopback, the PMA continues to propagate data in the Rx direction and drives the Rx PMA service interface towards the PMA client." If both remote loopback and local loopback are enabled, then these statements are contradictory. The service interfaces cannot transmit both loopback data and propagated data.

SuggestedRemedy

The output data at each service interface should be defined when both local loopback and remote loopback are enabled (probably loopback data, not propagated data); or it must be stated that local loopback and remote loopback are mutually exclusive.

Proposed Response Response Status O

Cl 176 SC 176.7.4 P281 L8 # 138

Brown, Matt Alphawave Semi

Comment Type T Comment Status X

In 174A.6, a set of test methods are defined to measure the block error ratio for inter-sublayer links (ISLs). These test methods require the PRBS31Q error check to be enhanced to include block error checkers and block error bin counters as defined in 174A.6.1.1 and 174A.6.1.2.

SuggestedRemedy

Define block error counting and related counters. A contribution on this topic will be provided.

Proposed Response Response Status O

Cl 176 SC 176.7.4 P281 L8 # 135
 Brown, Matt Alphawave Semi
 Comment Type T Comment Status X
 176A.5 defines test methodologies for measuring block errors without the use of a PCS. This methodology generates and check a PRBS31Q sequence in the PMA. New counters are required for each lane attached to a PMD or AUI component associated with the PRBS31Q error checker.
 SuggestedRemedy
 Define new counters as summarized in 174A.6.1.1.
 Proposed Response Response Status O

Cl 176 SC 176.10 P281 L60 # 370
 Slavick, Jeff Broadcom
 Comment Type T Comment Status X
 Support of the "optional" path delay information should be presented as the first information of this section not the last.
 SuggestedRemedy
 Change 176.10 to be:
 176.10 Path data delay (optional)
 Support for the optional path data delay information is indicated by the PMA status variables PMA_delay_ns_TX_ability, PMA_delay_subns_TX_ability, PMA_delay_ns_RX_ability, and PMA_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).
 When path delay information is supported, the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on an odd PCS lane, corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.
 Four separate delays are reported in the following eight path data delay status variables:
 — PMA_delay_ns_TX_max, PMA_delay_subns_TX_max
 — PMA_delay_ns_TX_min, PMA_delay_subns_TX_min
 — PMA_delay_ns_RX_max, PMA_delay_subns_RX_max
 — PMA_delay_ns_RX_min, PMA_delay_subns_RX_min
 Proposed Response Response Status O

Cl 176 SC 176.12 P252 L1 # 323
 Nicholl, Gary Cisco Systems
 Comment Type TR Comment Status X
 Need to update PICS to include path data delay for time synchronization (see 176.10) . See 175.9.4.7 as an example for what was done for the 1.6TBASE-R PCS in Clause 175.
 SuggestedRemedy
 Updated PICs to include path data delay for time synchronization. See 175.9.4.7 as an example.
 Proposed Response Response Status O

Cl 176C SC 176C.2 P677 L22 # 113
 Brown, Matt Alphawave Semi
 Comment Type T Comment Status X
 Figure 178-2. The signals SLi and DLi are never defined in Annex 176C.
 SuggestedRemedy
 In Figure 176C-2, add a note similar to the note in Figure 179-2.
 Proposed Response Response Status O

Cl 176C SC 176C.2 P678 L11 # 153
 Dudek, Mike Marvell
 Comment Type TR Comment Status X
 Figure 176D-2 is still confusing. The boxes around what are called components don't include the package, which is part of what is being called a component in the text.
 SuggestedRemedy
 Change from "C2C component transmitter" and "C2C component receiver" to "C2C transmitter" and "C2C receiver" or "C2C transmitter device" and "C2C receiver device" or less preferred "C2C transmit function" and "C2C receive function" (as used in figure 178-2)
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 176C SC 176C.3.1 P679 L27 # 133

Brown, Matt Alphawave Semi

Comment Type E Comment Status X

The "Error ratio allocation" subclause should not be a level 3 heading under service interfaces.

SuggestedRemedy

Change the heading number from "177C.3.1" to "176C.4" and renumber the subsequent level 3 headers.

Proposed Response Response Status O

Cl 176C SC 176C.3.1 P679 L27 # 134

Brown, Matt Alphawave Semi

Comment Type E Comment Status X

To be consistent with the various PMD clauses the error allocation subclause should be a level 2 heading immediately after the overview subclause.

SuggestedRemedy

Move "176C.3.1" to just before 176C.2 and change to a level 2 heading "176C.2". Similarly, move 176D.4 to just before 176C.2.

Proposed Response Response Status O

Cl 176C SC 176C.3.1 P679 L29 # 119

Brown, Matt Alphawave Semi

Comment Type E Comment Status X

For consistency with PMD clauses, the error allocation subclause should be 2nd level heading right after the introduction.

SuggestedRemedy

Move 176C.3.1 to be immediately after 176C.1, with new heading number 176C.2.

Proposed Response Response Status O

Cl 176C SC 176C.4.3 P680 L24 # 361

Sakai, Toshiaki Socionext

Comment Type T Comment Status X

In "Table 176C-1 Transmitter electrical characteristics at TP0v", Difference effective return loss, dERL (min) is still TBD. In "Table 176C-3 Receiver characteristics at TP5v", the dERL value for receiver is "-3dB". In CL178 (KR), the ERL values for transmitter and receiver are the same. (-3dB)

There is no reason not to set the dERL value for transmitter to "-3dB".

SuggestedRemedy

Change C2C transmitter dERL value from "TBD" to "-3dB".

Proposed Response Response Status O

Cl 176C SC 176C.4.3.1 P681 L18 # 154

Dudek, Mike Marvell

Comment Type T Comment Status X

The only references to a PMA management function in 802.3dj are in clause 186 which isn't relevant to this AUI interface. The correct control function to be used for this C2C interface is the same as the one used in Clauses 178 and 179. The reference to the description is blank.

SuggestedRemedy

Delete the sentence. "The transmitter output may be manipulated using the control function or PMA management interface as described in ."

Add a new paragraph "The transmitter output may be manipulated using the Type E1 Inter Sublayer link training function as described in Annex 178B.10

Proposed Response Response Status O

Cl 176C SC 176C.4.4 P685 L45 # 155

Dudek, Mike Marvell

Comment Type T Comment Status X

The insertion loss should include the package as is done for clause 178.

SuggestedRemedy

replace the footnote b to table 176C-4 with footnote b to table 178-19

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl **176C** SC **176C.5.1** P**688** L**9** # **352**
 Simms, William (Bill) NVIDIA
 Comment Type **TR** Comment Status **X**
 Table 176C-7 has Ane set to 0.578V which is consistent with 0.6Vf but should be reduced to 0.482 to match Vf of 0.5V
 SuggestedRemedy
 Reduce Ane to 0.482
 Proposed Response Response Status **O**

Cl **176D** SC **176D.4** P**698** L**42** # **120**
 Brown, Matt Alphawave Semi
 Comment Type **E** Comment Status **X**
 For consistency with PMD clauses, the error allocation subclause should be 2nd level heading right after the introduction.
 SuggestedRemedy
 Move 176D.4 to be immediately after 176D.1, with new heading number 176D.2.
 Proposed Response Response Status **O**

Cl **176D** SC **176D.1** P**696** L**14** # **195**
 Li, Tobey MediaTek
 Comment Type **ER** Comment Status **X**
 Typo in "400 Gb/s two-lane Attachment Unit Interface (200GAUI-2 C2M)"
 SuggestedRemedy
 Change "200GAUI-2 C2M" to "400GAUI-2 C2M".
 Proposed Response Response Status **O**

Cl **176D** SC **176D.4.3** P**700** L**23** # **409**
 Dawe, Piers Nvidia
 Comment Type **TR** Comment Status **X**
 In D1.1, vf min was 0.387 V, from 3ck CR, which was too high for C2M anyway. This draft shows 0.4 which is even worse and not consistent with 0.4 V at the silicon.
 SuggestedRemedy
 Reduce it, at least back to 0.387 but preferably to $0.9/2^4/5^0.387/0.4 = 0.348$ V for a nominal 900 mV +/-20%
 Proposed Response Response Status **O**

Cl **176D** SC **176D.1** P**696** L**44** # **196**
 Li, Tobey MediaTek
 Comment Type **ER** Comment Status **X**
 Figure 176D-1,
 200GAUI-1 shall be 200 Gb/s 1-LANE ATTACHMENT UNIT INTERFACE.
 400GMII shall be 400 Gb/s MEDIA INDEPENDENT INTERFACE
 SuggestedRemedy
 Line 44, change "200GAUI-1 = 100 Gb/s 1-LANE ATTACHMENT UNIT INTERFACE" to "200GAUI-1 = 200 Gb/s 1-LANE ATTACHMENT UNIT INTERFACE"
 Line 47, change "400GMII = 200 Gb/s MEDIA INDEPENDENT INTERFACE" to "400GMII = 400 Gb/s MEDIA INDEPENDENT INTERFACE"
 Proposed Response Response Status **O**

Cl **176D** SC **176D.4.3** P**700** L**23** # **410**
 Dawe, Piers Nvidia
 Comment Type **TR** Comment Status **X**
 1.2 V is quite excessive for C2M, and, considering modern silicon processes, excessive for anything high speed in 2024.
 SuggestedRemedy
 Change to 0.9 V, as is normal for C2M. Similarly, reduce vf max to 450 mV.
 Proposed Response Response Status **O**

Cl 176D SC 176D.4.3 P700 L40 # 408

Dawe, Piers

Nvidia

Comment Type **TR** Comment Status **X**

In 3ck, C2M had just two modes for its "transmitter output waveform training". In this project, COM seems to think that TxFIR setting is not important, although that may be a feature of the abstract COM receiver not real receivers. It is not clear whether CR needs such careful transmitter output waveform rules, and if it does, it does not necessarily follow that C2M, with less loss, also needs them. The editor's note under the COM table says some of this.

SuggestedRemedy

Relax the transmitter output waveform limits as appropriate.
Do the same in other clauses if appropriate.

Proposed Response Response Status

Cl 176D SC 176D.5.3 P700 L22 # 82

Ran, Adeo

Cisco Systems, Inc.

Comment Type **TR** Comment Status **X**

The specification of "Differential peak-to-peak voltage (max)" in Table 176D-1 points to 176D.7.1. In addition, it has footnote a, saying that the measurement uses the method in 93.8.1.3 except that PRBS13Q test pattern is used.

The footnote is not required since there is a full description in 176D.7.1.

As noted in comment #416 against D1.1, the peak-to-peak of PRBS13Q is not indicative of the values that can occur in mission data, unless the channel+equalization attenuate low frequencies that are not present in PRBS13Q.

The specified max peak-to-peak voltage is intended to hold with any data pattern, not just PRBS13Q, and at any equalization setting. It is a clear design requirement that does not require a specific measurement method (the standard is not a measurement specification). Designers and testers know what peak-to-peak voltage is without the reference to 93.8.1.3 (which does not actually define it, it only specifies a test pattern which is inappropriate for this project).

This also applies to module output in Table 176D-2 and to CR and KR transmitter output specifications, although the loss to the measurement point for those is smaller.

SuggestedRemedy

Delete footnote a in this table.

Add a paragraph in 176D.7.1 stating that differential peak-to-peak requirements apply at any equalization setting and with any pattern presented at the service interface.

In Table 176C-1, Table 178-6, and Table 179-7, delete footnote a and replace the reference to 93.8.1.3 with a reference to 176D.7.1

A presentation with measurement results and a detailed suggested remedy is planned.

Proposed Response Response Status

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 176D SC 176D.5.3 P700 L24 # 353
 Simms, William (Bill) NVIDIA
 Comment Type TR Comment Status X
 Table 176D-1 has the Differential pk-pk voltage (max) Output enabled as 1.2V. This should be reduced to 1.0V to be consistent with Vf of 0.500
 SuggestedRemedy
 Reduce Differential pk-pk voltage (max) to 1.0V when Transmitter enabled
 Proposed Response Response Status O

Cl 176D SC 176D.5.3 P700 L34 # 313
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 C2M historically had Vmax of 900 mV or Vf of 450 mV, increasing Vf to 600 mV add additional power and may result in compatability issue with legacy module
 SuggestedRemedy
 Reduce Vf max from 600 mV to 500 mV which offers all the benefit but with reduced crosstalk penalty as was shown in simms_3dj_01a_2409
 Also if we increase Vf to 600 mV the current common mode voltage would need to scale up by the ratio of 600/450 otherwise it will be very difficult to meet common mode limits that came from CK!
 Proposed Response Response Status O

Cl 176D SC 176D.5.3 P700 L34 # 411
 Dawe, Piers Nvidia
 Comment Type TR Comment Status X
 Several inappropriate backplane-style "micro-managing" many-quotas spec items have appeared that are wasteful and unnecessary diagnostics, and some are not measurable with the losses allowed in C2M with reasonable reflections. This is not the way to specify an observable signal. Remember, our task is to specify the *signal at the interface* not hypothesise about the silicon 20-ish dB behind it.
 See other comments noting the impracticality of the 120D style jitter measurement method for this project. See dawe_3dj_01a_2406, calvin_3dj_02a_2407 and successor.

SuggestedRemedy
 Remove vf (min), Rpeak, SNDR, SNR_ISI and output jitter. Add a VEC-like, TDECQ-like spec, which can be measured in a scope using the COM reference receiver parameters from Table 176D-6 (see dawe_3dj_01_2409). The VEC limit is derived from the COM table too.
 Remove RLM; in 120E we decided we didn't need a separate eye linearity spec.
 Add an Eye Amplitude spec based on the same measurement (note that dawe_3dj_01_2409 says Eye Height: Eye Amplitude is meant).
 Note that because of instrument noise, VEC and Eye Amplitude (like SNDR) should not be measured on small signals, but on nominal-minimum signals before any training process has reduced them ("presets").
 Apply to C2M throughout 176D.
 Another comment proposes the same approach for 179, CR.
 Proposed Response Response Status O

Cl 176D SC 176D.5.3 P700 L34 # 354
 Simms, William (Bill) NVIDIA
 Comment Type TR Comment Status X
 Table 176D-1 has Transmitter steady-state voltage, Vf (range) 0.4 to 0.6 V. This range should be reduced to 0.4 to 0.5 to be consistent with Vf of 0.500
 SuggestedRemedy
 change Transmitter steady-state voltage, Vf (range) to 0.4 to 0.5V
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 176D SC 176D.5.3 P700 L49 # 315

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

We currently have no effective output compliance test method for C2M or input calibration of stressor. We replaced VEC with with JRMS, EOJ, and J4U without any demonstration that using transmit jitter is sufficient for receive compliance.

SuggestedRemedy

TDECQ method works given all the data presented and with the work of OIF LPO and RTLRL developing. TDECQ/EECQ already captures the jitter as shown in ghiasi_3dj_01a_2409 but also captures amplitude penalty and the effect of PM to AM conversion in the same way as receiver will observe the penalty. EECQ for receive stress measurement and calibration we need to do the following:

Add editor note encouraging data if current jitter test method can be used for receive compliance and encourage data on EECQ for receive compliance.

Proposed Response Response Status O

CI 176D SC 176D.5.3 P700 L50 # 211

Rysin, Alexander NVIDIA

Comment Type TR Comment Status X

J3u and JRMS measurements at TP1a are highly affected by the effects of slew rate and noise and do not reflect actual uncorrelated jitter. These effects are exacerbated by the characteristics of practical channels between TP0d and TP1a - loss and reflections, and are highly dependent on the transmitted signal amplitude. Accounting only for the faster edges does not work for practical channels at 106.25 Gbd rate and the currently proposed numbers cannot be met (and sometimes cannot be measured) even with commercial test equipment PPG. The issue was demonstrated in rysin_3dj_01a_2407.

SuggestedRemedy

Other method of uncorrelated jitter measurement should be considered.

Proposed Response Response Status O

CI 176D SC 176D.5.4 P701 L19 # 355

Simms, William (Bill) NVIDIA

Comment Type TR Comment Status X

Table 176D-2 has the Differential pk-pk voltage (max) Output enabled as 1.2V. This should be reduced to 1.0V to be consistent with Vf of 0.500

SuggestedRemedy

Reduce Differential pk-pk voltage (max) to 1.0V when Transmitter enabled

Proposed Response Response Status O

CI 176D SC 176D.5.4 P701 L23 # 399

Dawe, Piers Nvidia

Comment Type T Comment Status X

AC common-mode voltages are not as large as this in practice, even at 200G/lane. Notice that while the full-band VCM is lower than for host output, the low-frequency VCM is the same, which is not realistic; a module does not have the very heavy-duty power supply that a host uses.

SuggestedRemedy

Halve the LF ACCM limit for module output (Table 176E-2) because the module output is measured in the MCB which should have a clean power supply. Also in Table 176E-3, host input ACCM tolerance. We may need a sentence of explanation: the host must tolerate this much module-generated ACCM, as well as any that it generates itself.

Proposed Response Response Status O

CI 176D SC 176D.5.4 P701 L31 # 356

Simms, William (Bill) NVIDIA

Comment Type TR Comment Status X

Table 176D-2 has Transmitter steady-state voltage, Vf (max) 0.6 V. This should be reduced to 0.5 to be consistent with Vf of 0.500

SuggestedRemedy

change Transmitter steady-state voltage, Vf (range) to 0.4 to 0.5V

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 176D SC 176D.5.4 P701 L31 # 314
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 C2M historically had Vmax of 900 mV or Vf of 450 mV, increasing Vf to 600 mV add additional power and may result in compatability issue with legacy module
 SuggestedRemedy
 Reduce Vf max from 600 mV to 500 mV which offers all the benefit but with reduced crosstalk penalty as was shown in simms_3dj_01a_2409
 Also if we increase Vf to 600 mV the current common mode voltage would need to scale up by the ratio of 600/450 otherwise it will be very difficult to meet common mode limits that came from CK!
 Proposed Response Response Status O

CI 176D SC 176D.5.4 P701 L46 # 316
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 We currently have no effective output compliance test method for C2M or input calibration of stressor. We replaced VEC with with JRMS, EOJ, and J4U without any demonstration that using transmit jitter is sufficient for receive compliance.
 SuggestedRemedy
 TDECQ method works given all the data presentated and with the work of OIF LPO and RTLRL developing. TDECQ/EECQ already captrues the jitter as shown in ghiasi_3dj_01a_2409 but also captures amplitude penalty and the effect of PM to AM conversion in thre same way as receiver will observe the penalty. EECQ for receive stress measurement and calibration we need to do the follwing:
 Add editor note encouraging data if current jitter test method can be used for receive compliance and encourage data on EECQ for receive compliance.
 Proposed Response Response Status O

CI 176D SC 176D.5.4 P701 L47 # 212
 Rysin, Alexander NVIDIA
 Comment Type TR Comment Status X
 J4u and JRMS measurements at TP4 are highly affected by the effects of slew rate and noise and do not reflect actual uncorrelated jitter. These effects are exacerbated by the characteristics of practical test fixtures - loss and reflections, and are highly dependent on the transmitted signal amplitude. Accounting only for the faster edges does not work for practical channels at 106.25 Gbd rate. The issue was demonstrated in rysin_3dj_01a_2407.
 SuggestedRemedy
 Other method of uncorrelated jitter measurement should be considered.
 Proposed Response Response Status O

CI 176D SC 176D.5.5 P702 L27 # 357
 Simms, William (Bill) NVIDIA
 Comment Type TR Comment Status X
 Table 176D-3 has the Amplitude tolerance set to 1.2V. This should be reduced to 1.0V to be consistent with Vf reduced to 0.5V
 SuggestedRemedy
 Change Amplitude tolerance to 1.0V
 Proposed Response Response Status O

CI 176D SC 176D.5.6 P703 L10 # 156
 Dudek, Mike Marvell
 Comment Type TR Comment Status X
 Having a single-ended voltage tolerance range of -0.4 to 3.3V and a DC common-mode tolerance range of only -0.05 to 1.05V seems incorrect.
 SuggestedRemedy
 Change the single ended voltage tolerance range to -0.4 to 1.4V
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 176D SC 176D.5.6 P703 L17 # 358

Simms, William (Bill) NVIDIA

Comment Type TR Comment Status X

Table 176D-4 has the Amplitude tolerance set to 1.2V. This should be reduced to 1.0V to be consistent with Vf reduced to 0.5V

SuggestedRemedy

Change Amplitude tolerance to 1.0V

Proposed Response Response Status O

CI 176D SC 176D.6.2 P704 L22 # 317

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

The module reference package is TBD

SuggestedRemedy

We need to say "The module may have 1st level package model and when the module has 1st level package model the reference model is based on 4 to 10 mm of package A", see ghiasi_3dj_04a_2409

Proposed Response Response Status O

CI 176D SC 176D.6.2 P705 L5 # 83

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

Table 176D-5 contains parameters for the host channel model, which should be used for host input test calibration (176D.7.12.2, currently TBD).

The table has two package models with "test 1 / test 2" lengths (originating from the KR/C2C adopted packages), We need to have one package model with a set of parameters that are appropriate for this annex. Also, the PCB model was adopted but the PCB length is TBD.

The combination of package model, PCB model, and mated test fixtures should result in the adopted die-to-die channel ILdd of 32 dB (since the module ILdd allocation is identical to that of the HCB).

Also, the adopted ILdd of 32 dB should be used as the high-loss target for the module input test setup.

SuggestedRemedy

Delete the "Class A package model" row and set "Transmission line 1 length" in the "Class B package model" row to 45 mm (one value). Set the host channel mode zp as in Table 179-18. Specific values will be included in a separate presentation.

Refer to this model in "Host channel parameters" in Table 176D-9 (interference tolerance) and in 176D.7.12.2.

In Table 176D-9 change TBDs in "Test channel insertion loss at 53.125 GHz" row to:
Module test 1 (Low loss): min=9.25 dB, max:10.25 dB (mated test fixture allocation is 9.75 dB)
Module test 2 (High loss): min=31.5 dB, max=32.5 dB (maximum TP0d-TP1a loss is 32 dB)

Proposed Response Response Status O

CI 176D SC 176D.6.2 P706 L9 # 359

Simms, William (Bill) NVIDIA

Comment Type TR Comment Status X

Table 176D=6 has Ane set to 0.578V which is consistent with 0.6Vf but should be reduced to 0.482 to match Vf of 0.5V

SuggestedRemedy

Reduce Ane to 0.482

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 176D SC 176D.6.2 P706 L9 # 413
 Dawe, Piers Nvidia
 Comment Type TR Comment Status X
 These voltages Av Afe Ane look like old style backplane-style values, which should be reduced even for CR and KR, and should be reduced further for C2M. The Ane value, 0.578 V, is even worse than in the last draft (0.45 V).
 SuggestedRemedy
 Reduce Av Afe and Ane. Reduce the ratio between Ane and the others (representing the tolerance of the silicon, which should not be +/-20% in 2024). To make the COM table pass and fail the same scenarios, reduce eta0 in proportion.
 Proposed Response Response Status O

CI 176D SC 176D.6.2 P706 L38 # 318
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 Typical gDC1 gain for C2M is just few dB's, and there is no reason to have the same gDC1 as KR/CR
 SuggestedRemedy
 Reduce gDC1 to -12 dB
 Proposed Response Response Status O

CI 176D SC 176D.6.12.1 P711 L34 # 157
 Dudek, Mike Marvell
 Comment Type T Comment Status X
 Incomplete sentence that needs to be completed to make the test complete as pointed out in the editor's note
 SuggestedRemedy
 Implement the editor's note (and then delete the editor's note).
 Proposed Response Response Status O

CI 176D SC 176D.7.11 P710 L36 # 360
 Simms, William (Bill) NVIDIA
 Comment Type TR Comment Status X
 Amplitude tolerance set to 1.2V. This should be reduced to 1.0V to be consistent with Vf reduced to 0.5V
 SuggestedRemedy
 Change Amplitude tolerance to 1.0V
 Proposed Response Response Status O

CI 176D SC 176D.7.12 P711 L31 # 412
 Dawe, Piers Nvidia
 Comment Type TR Comment Status X
 The figures "Example host output test configuration" and "Example module output test configuration" have gone missing.
 SuggestedRemedy
 Reinstate them. They are needed to show the crosstalk calibration, as one cannot assume that the host generates the same crosstalk as the MCB.
 Proposed Response Response Status O

CI 176D SC 176D.7.12.4 P714 L37 # 158
 Dudek, Mike Marvell
 Comment Type T Comment Status X
 It would be good to clarify that Preset 1 is maximum amplitude.
 SuggestedRemedy
 Change "transmitters in the DUT transmit a scrambled idle pattern with equalization turned off (preset 1 condition)." to transmitters in the DUT transmit a scrambled idle pattern at maximum amplitude with equalization turned off (preset 1 condition)."
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 176D SC 176D.7.13.2 P715 L4 # 319
Ghiasi, Ali Ghiasi Quantum
Comment Type E Comment Status X
Extra character
SuggestedRemedy
Remove the "e" between step and 176D.7.12.2
Proposed Response Response Status O

CI 176D SC 176D.7.13.2 P715 L5 # 320
Ghiasi, Ali Ghiasi Quantum
Comment Type T Comment Status X
The test procedure for jitter tolerance is not comprehensive and doesn't stress the receiver at maximum input stress if the noise source is turned off then you turn on the SJ source. Given all the concern about block errors not having comprehensive JTOL only will result in block over compliant links.
SuggestedRemedy
What has been done for several generation of C2M and optical interfaces the noise source is dialed by 0.05 UI then SJ in table 176D-10 is applied. All the SJ in table 176D-10 integrate to 0.05 UI.
Proposed Response Response Status O

CI 176D SC 176D.7.13.2 P715 L18 # 296
Ghiasi, Ali Ghiasi Quantum
Comment Type T Comment Status X
Receiver jitter tolerance frequencies are separated by ~3x but in the case of test case A and B the frequencies are separated by a decade which may mask possible jitter peaking and sensitivity issue in this band
SuggestedRemedy
Add one additional test point between case A and B at frequency of 0.125 MHz with jitter amplitude of 1.6 UI
Proposed Response Response Status O

CI 177 SC 177.2 P290 L37 # 378
Slavick, Jeff Broadcom
Comment Type E Comment Status X
Noting that there is a clock propagation in addition to the actual listed primitives should occur right after we list out those parameters and before we fully define them.
SuggestedRemedy
Move the last paragraph of 177.2 to be after the bullet list of interface primitives.
Proposed Response Response Status O

CI 177 SC 177.4.1 P291 L34 # 54
Opsasnick, Eugene Broadcom
Comment Type TR Comment Status X
The alignment lock function is needed for 200GBASE-R and 400GBASE-R as well as 800G and 1.6T since the convolutional interleaver requires the AM or RS-symbol boundary information. 800GBASE-R and 1.6TBASE-R require the deskew function (while 200G and 400G do not). The alignment lock and deskew functions can be described with references to the same functions within Clause 176 SM-PMA RX and TX processes.
SuggestedRemedy
Add the Alignment lock function for 200G and 400G (but no deskew). Add a description of the alignment lock (common to 200G/400G/800G/1.6T) and the necessary deskew for 800G and 1.6T. A presentation will be made with a more specific proposal.

In addition, since 200G/400G require alignment lock, the "align_status" variable is always present and Table 177-2 can remove the row with "OK | N/A | OK" and remove footnotes (a) and (b).
Proposed Response Response Status O

CI 177 SC 177.4.1 P291 L35 # 371
Slavick, Jeff Broadcom
Comment Type T Comment Status X
Details for Alignment and deskew is needed
SuggestedRemedy
Presentation detailing updates to be submitted.
Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 177 SC 177.4.2 P291 L45 # 383
 Slavick, Jeff Broadcom
 Comment Type T Comment Status X
 With the addition of the deskew process the Convolutional interleaver no longer uses the PMA lanes directly but rather the deskewed lanes.
 SuggestedRemedy
 Add the word "deskewed" before PMA in the first sentence of 177.4.2.
 Proposed Response Response Status O

Cl 177 SC 177.5.2 P298 L22 # 386
 Slavick, Jeff Broadcom
 Comment Type T Comment Status X
 Steps a) and b.2) and c) tell us what step to proceed to but b.1) does not.
 SuggestedRemedy
 Add go to step c) to end of step b) 1)
 Proposed Response Response Status O

Cl 177 SC 177.4.2 P291 L47 # 384
 Slavick, Jeff Broadcom
 Comment Type T Comment Status X
 No mechanism to identify the RS-FEC symbol boundaries is provided.
 SuggestedRemedy
 Change the sentence that begins with "The four RS-FEC symbols in each RS-FEC symbol-quartet are from four different RS-FEC codewords" to "Using the RS-FEC boundaries found by the Alignment and Deksew process (see 177.4.1) the convolutioner interleaver creates groups of four RS-FEC symbols from four RS-FEC codewords."
 Proposed Response Response Status O

Cl 177 SC 177.5.2 P298 L22 # 388
 Slavick, Jeff Broadcom
 Comment Type T Comment Status X
 Explanation of the sync process is not necessary just point to the FSM.
 SuggestedRemedy
 Remove steps a,b,c
 Proposed Response Response Status O

Cl 177 SC 177.4.2 P291 L52 # 385
 Slavick, Jeff Broadcom
 Comment Type E Comment Status X
 There is a , in the 1536 number.
 SuggestedRemedy
 Remove the comma
 Proposed Response Response Status O

Cl 177 SC 177.5.2 P298 L32 # 362
 Slavick, Jeff Broadcom
 Comment Type T Comment Status X
 Where flow 0 is "will be" identified once the lock process is complete, it's not possible to fail to do that.
 SuggestedRemedy
 Change "may be" to "is"
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 177 SC 177.5.2 P298 L45 # 32
Huang, Kechao Huawei
Comment Type T Comment Status X
"FS" should be changed to "FAS", as it is the shortened form of "Frame Alignment Sequence", see subclause 177.4.7.1.
SuggestedRemedy
In page 298, change "FS" to "FAS" in Lines 45, 46, 48, 49, 51;
In page 298, change "FSs" to "FASs" in Line 47;
In page 302, change "FS" to "FAS" in Line 12
Proposed Response Response Status O

CI 177 SC 177.5.2. P298 L27 # 387
Slavick, Jeff Broadcom
Comment Type E Comment Status X
The phrase "at least 140" is intending the minimum value of invalid codewords in which you take this branch. Alternative wording could be used to improve clarity of the function.
SuggestedRemedy
Change "at least 140" to "140 or more"
Proposed Response Response Status O

CI 177 SC 177.6.2.1 P301 L8 # 33
Huang, Kechao Huawei
Comment Type T Comment Status X
"fs" should be changed to "fas", as it is the shortened form of "Frame Alignment Sequence", see subclause 177.4.7.1. Suggest to apply similar changes in subclause 177.6
SuggestedRemedy
Change "fs" to "fas" in subclause 177.6.2.1, 177.6.2.3, and figures 177-9 and 177-10
Proposed Response Response Status O

CI 177 SC 177.6.2.1 P301 L15 # 34
Huang, Kechao Huawei
Comment Type T Comment Status X
"frame sequence" should be changed to "frame alignment sequence"
SuggestedRemedy
In page 301, change "frame sequence" to "frame alignment sequence" in Lines 15,16,19.
Proposed Response Response Status O

CI 177 SC 177.6.3 P303 L11 # 389
Slavick, Jeff Broadcom
Comment Type T Comment Status X
restart_inner_fec_sync should only be controlled by one FSM. The forcing of fs_lock false will cause the pad detection FSM to go to INIT which will clear the restart_inner_fec_sync allowing the self-sync FSM to begin to re-sync.
SuggestedRemedy
Remove "restart_inner_fec_sync <= false" from INNER_FEC_SYNC_INIT
Proposed Response Response Status O

CI 177 SC 177.6.3 P303 L29 # 390
Slavick, Jeff Broadcom
Comment Type T Comment Status X
The exit from CW_CHECK_1 and CW_CHECK_2 for values of 13 have the wrong variable name
SuggestedRemedy
Change valid_cw=13 to valid_cw_cnt=13 two places Fig 177-9
Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 177 SC 177.6.3 P304 L3 # 363
 Slavick, Jeff Broadcom
 Comment Type T Comment Status X
 Why is the dotted box considered optional? This is a new diagram/clause why not make the monitor function mandatory.
 SuggestedRemedy
 Remove the dotted box and associated note from Figure 177-10
 Proposed Response Response Status O

Cl 177 SC 177.8 P305 L15 # 165
 He, Xiang Huawei
 Comment Type TR Comment Status X
 Delay constraints are TBD. Based on convolutional interleaver delays given in the baseline, and a conservative estimation of Inner FEC decoding latency of 51.2ns, propose to use the following delay constraints in number of pause_quanta for 200GE/400GE/800GE/1.6TE, respectively:
 130/150/190/270
 SuggestedRemedy
 In Table 177-5 Use 130/150/190/270 pause_quanta for 200GE/400GE/800GE/1.6TE, respectively, and calculate the rest based on these numbers.
 Proposed Response Response Status O

Cl 177 SC 177.10 P306 L47 # 364
 Slavick, Jeff Broadcom
 Comment Type T Comment Status X
 Support of the "optional" path delay information should be presented as the first information of this section not the last.
 SuggestedRemedy
 Change 177.10 to be:
 177.10 Path data delay (optional)
 Support for the optional path data delay information is indicated by the status variables Inner_FEC_delay_ns_TX_ability, Inner_FEC_delay_subns_TX_ability, Inner_FEC_delay_ns_RX_ability, and Inner_FEC_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported, the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on the first symbol on FEC flow 0 after the 1024-bit pad insertion (see 177.4.7), corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.
 Four separate delays are reported in the following eight path data delay status variables:
 — Inner_FEC_delay_ns_TX_max, Inner_FEC_delay_subns_TX_max
 — Inner_FEC_delay_ns_TX_min, Inner_FEC_delay_subns_TX_min
 — Inner_FEC_delay_ns_RX_max, Inner_FEC_delay_subns_RX_max
 — Inner_FEC_delay_ns_RX_min, Inner_FEC_delay_subns_RX_min
 Proposed Response Response Status O

Cl 177 SC 177.11 P306 L36 # 2
 Marris, Arthur Cadence Design Systems
 Comment Type T Comment Status X
 align_status references 177.4.1 in the transmit path. However align_status seems to be defined in Table 177-2 which references 119.2.6.2.2 which is describing receive PCS functionality.
 SuggestedRemedy
 Rename the align_status variable to something different which makes clear it is referring to transmit operation
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 177 SC 177.12 P311 L1 # 324
 Nicholl, Gary Cisco Systems
 Comment Type **TR** Comment Status **X**
 Need to update PICS to include path data delay for time synchronization (see 177.10) .
 See 175.9.4.7 as an example for what was done for the 1.6TBASE-R PCS in Clause 175.
 SuggestedRemedy
 Updated PICS to include path data delay for time synchronization. See 175.9.4.7 as an
 example.
 Proposed Response Response Status **O**

Cl 178 SC 178.8.1 P320 L50 # 140
 Brown, Matt Alphawave Semi
 Comment Type **T** Comment Status **X**
 Figure 178-2. The signals SLi and DLi are never defined in Clause 178.
 SuggestedRemedy
 In Figure 178-2, add a note similar to the note in Figure 179-2. Do the same for Figure
 176C-2.
 Proposed Response Response Status **O**

Cl 178 SC 178.1 P314 L36 # 163
 Dudek, Mike Marvell
 Comment Type **TR** Comment Status **X**
 The optional clause 120PMA is allowed to operate with a 100ppm clock frequency
 tolerance whereas the tolerance for the normative clause 176 PMA is only 50ppm.
 SuggestedRemedy
 Add a footnote to the clause 120PMA stating. "Usable within an extender without
 restriction. If used between PCSs the transmitter frequency tolerance is reduced to
 <=50ppm Add the same footnote to all the equivalent tables in the other clauses.
 Proposed Response Response Status **O**

Cl 178 SC 178.9.2 P322 L18 # 345
 Simms, William (Bill) NVIDIA
 Comment Type **TR** Comment Status **X**
 Table 178-6 has the Differential pk-pk voltage (max) Transmit enabled as 1.2V. This
 should be reduced to 1.0V to be consistent with Vf of 0.500
 SuggestedRemedy
 Reduce Differential pk-pk voltage (max) to 1.0V when Transmitter enabled
 Proposed Response Response Status **O**

Cl 178 SC 178.2 P318 L51 # 131
 Brown, Matt Alphawave Semi
 Comment Type **T** Comment Status **X**
 The wording for the various error ratio expectations is not in line with various updates in
 Annex 176A in Draft 1.2. The same is true for 179.2, 180.2, 181.2, 182.2., 183.2, 176C.3.1,
 176D.3.1, 185.2.
 SuggestedRemedy
 A contribution to address this will be provided.
 Proposed Response Response Status **O**

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 178 SC 178.9.2 P322 L46 # 64

Ran, Adeo Cisco Systems, Inc.

Comment Type T Comment Status X

In previous projects there were two different specifications, J3u_03 for PMDs and for J4u_03 for AUIs. This was based on the different BER allocations which translated to average FEC symbol error ratios. The limit values were based on the same dual-Dirac model, and the different maximum values are a constant source of confusion.

We now know that jitter creates correlated errors. Therefore, peak-to-peak jitter should be specified at probabilities lower than the expected average symbol error ratio. The probability allowed for jitter peaks should not be higher for PMDs.

With that in mind, having two specifications, J3u and J4u, is not justified anymore. J3u is faster to measure, but if J4u is measurable for an AUI it is also measurable for a PMD.

J4u should be used for PMD specs too. The maximum specs should be changed accordingly, including accounting for measurement degradation due to package or host channel loss.

SuggestedRemedy

For KR (Table 178–6), change J3u_03 to J4u_03 with the same maximum values as in C2C (Table 176C–1): 0.118 for class A and 0.12 for class B.

For CR (Table 179-7), change J3u_03 to J4u_03 with maximum values: 0.128, 0.126, and 0.143 for HL, HN, and HH, respectively.

Change the definitions accordingly, and in other places as necessary with editorial license.

Proposed Response Response Status O

CI 178 SC 178.9.2 P323 L4 # 62

Ran, Adeo Cisco Systems, Inc.

Comment Type T Comment Status X

The editor's note addresses an assumption that measured jitter is affected by the loss to the measurement point. A contribution in July 2024, https://www.ieee802.org/3/dj/public/24_07/calvin_3dj_01b_2407.pdf, demonstrates this effect (see e.g. slide 9 showing the effect of "Slew rate"), so this should not be regarded as an "assumption" anymore.

Similar editor's notes appear in 179.9.4, 176D.3.3, and 176E.4.4.

While further work is still encouraged, the editor's notes should not question the effect.

SuggestedRemedy

In the listed editor's notes, replace "based on the assumption that that the measured jitter is affected by" with "to address the dependence of measured jitter on".

Proposed Response Response Status O

CI 178 SC 178.9.2.1.1 P323 L35 # 65

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

TP0 to TP0v test fixture specifications has multiple TBDs.

As initial values, we can use the values from clause 163 scaled by a factor of 2.

SuggestedRemedy

Use:
 ILdd between 3.4 dB and 10 dB at 53.125 GHz
 ILD magnitude up to 0.4 dB from 0.05 GHz to 53.125 GHz
 Tt is 0.005 ns

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 178 SC 178.9.2.1.1 P323 L35 # 189

Mellitz, Richard Samtec

Comment Type TR Comment Status X

The insertion loss and the delay for the test fixture needs to be tightly controlled to minimize the variability. That is because there will be load variability in the measurement equipment. The idea should be to add enough loss so as not to significantly signal degrade the signal but dampen the effects of test equipment load variability.

SuggestedRemedy

Change to:
The insertion loss of the test fixture shall be between 4 dB and 5 dB at 53.125 GHz. With a delay between 500 and 650 ps. (based on 1.2 dB /inch and 150 ps /inch and e_r approximately 3.2)

Proposed Response Response Status

Cl 178 SC 178.9.2.1.1 P323 L36 # 190

Mellitz, Richard Samtec

Comment Type TR Comment Status X

The fixture frequency content needs to extend beyond the Nyquist rate. S-parameter measurements are required for this test fixture for ERL. This fixture is also required for s-parameter measurements when computing COM for receiver compliance. A transition time of 5 ps is used for ERL computation and is trending to around 4 ps for COM. A frequency range needs to be chosen to minimize the Gibbs Phenomena. There can be significant error due to this for ERL or COM computation. Filtering can help, however, there is still an error. Consider the data has a sinc response, the loss difference of between 53 GHz and 85 GHz with a BT filter is about 10 dB which is just about amount of filtering need to minimize this error. The loss difference between 53 GHz and 67 GHz is about 4 dB which is likely to start showing this error.

SuggestedRemedy

Change to:
The magnitude of the insertion loss deviation of the test fixture shall be less than or equal to 0.2 dB from 0.05 GHz to 85 GHz. Insertion loss deviation is calculated as specified in 93A.4, where Tt is 0.005 ns, and fb and fr values are taken from Table 178–12.

Proposed Response Response Status

Cl 178 SC 178.9.2.1.2 P324 L17 # 192

Mellitz, Richard Samtec

Comment Type TR Comment Status X

N_bx in the Table 187A-7 should be 0 so test fixture will not interfere with measurement as in IEEE802.3ck.

SuggestedRemedy

Relace with the row 5 with:
Equalizer length associated with reflection signal: N_bx : 0

Proposed Response Response Status

Cl 178 SC 178.9.2.1.2 P324 L23 # 66

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

Multiple ERL limits are TBD.

Using 802.3ck as a reference:
For KR test fixture at Tp0v, in 163.9.2.1.2 the minimum is 15 dB.
For CR transmitter at TP2, in 162.9.4 the minimum is 7.3 dB.
For CR receiver at TP3, in 162.9.5 the minimum is 7.3 dB.
For copper cables, in 162.11.2 the minimum is 8.25 dB.
For C2C at Tp0v, in 120F.3.1 dERL is -3 dB (as it is in 802.3dj Table 178–6 for KR).
For C2C channel, in 120F.4.3 the minimum is 9.7 dB.
For C2M host, in 120G.3.1 and in 120G.3.3 the minimum is 7.3 dB.
For C2M module, in 120G.3.2 and in 120G.3.4 the minimum is 8.5 dB.
For mated test fixture, in 162B.4.2 the minimum is 10.3 dB.

Unless shown otherwise, the same ERL requirements are appropriate for this project.

SuggestedRemedy

Use the values in the comment to replace the corresponding TBDs in 178, 179, 176C, 176D, and 179B.

Proposed Response Response Status

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 178 SC 178.9.2.1.2 P324 L23 # 191

Mellitz, Richard Samtec

Comment Type TR Comment Status X

Consider ERL of 7 dB maybe minimal, 10 dB may be marginal, 15 dB may be good, and about 20 dB may be very good. Since ERL was scaled with T_r then relative amount of reflection from the test fixture should be the same as in 803.3ck.

SuggestedRemedy

Change to:

The ERL at TP0v shall be greater than or equal to 15 dB.

Proposed Response Response Status O

CI 178 SC 178.9.2.1.3 P314 L34 # 63

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

Test fixture RLcc parameters are TBD.

In 163.9.2.1.3 the specification is >=6 dB up to 40 GHz.

The suggested remedy is the same minimum with the frequency range adopted for 802.3dj. Alternatively, this specification can be deleted, since RLcc of a bare TP0-TP0v test fixture (without a DUT attached to it) may be impractical to measure.

SuggestedRemedy

Change to "6 dB at all frequencies between 0.2 GHz and 67 GHz".

Proposed Response Response Status O

CI 178 SC 178.9.2.1.3 P324 L33 # 193

Mellitz, Richard Samtec

Comment Type TR Comment Status X

CD or DC are better quality indicator of line the quality of line imbalance because it will catch skew and should augment CC.

SuggestedRemedy

Add section:

178.9.2.1.x Test fixture differential-mode to common-mode return loss

The differential-mode to common-mode return loss of the test fixture at either port shall be less than or than or equal to 10 dB at all frequencies between 0.2 GHz and 85 GHz.

Proposed Response Response Status O

CI 178 SC 178.9.3.3 P327 L53 # 149

Dudek, Mike Marvell

Comment Type TR Comment Status X

Even if the package class is known of a transmitter of unknown S parameters it is only known what the maximum package loss might be. The package loss of the specific port of the package being used could have maybe 8dB less loss than this maximum loss. This would result in the interference test being performed with 8dB too little loss which is unacceptable.

SuggestedRemedy

Delete this option.

Proposed Response Response Status O

CI 178 SC 178.9.3.3 P329 L18 # 207

Healey, Adam Broadcom Inc.

Comment Type T Comment Status X

Table 178-10 note c) refers to 93C.2 step 7) for the broadband noise calibration used to achieve the target COM value. 93C.2 step 7) refers to a procedure in 93A.2 that is not appropriate for specifications based on Annex 178A.

SuggestedRemedy

Define a new broadband noise calibration procedure for Annex 178A COM. A contribution will be provided with a detailed proposal. This would also apply to 176C.4.4.4.

Proposed Response Response Status O

CI 178 SC 178.10.1 P333 L12 # 346

Simms, William (Bill) NVIDIA

Comment Type TR Comment Status X

Table 178-13 has Ane set to 0.578V which is consistent with 0.6Vf but should be reduced to 0.482 to match Vf of 0.5V

SuggestedRemedy

Reduce Ane to 0.482

Proposed Response Response Status O

Cl 178 SC 178.10.2 P334 L35 # 67

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

Channel insertion loss (recommended) is a TBD equation.
As the editor's note says, this recommendation was not included in the baseline proposal and "Contributions in this area are encouraged".

SuggestedRemedy

A contribution providing a recommendation is solicited.

Proposed Response Response Status O

Cl 178A SC 178A P L # 90

Ran, Adeo Cisco Systems, Inc.

Comment Type T Comment Status X

There are multiple electrical specifications that are defined in clause 179 and then referenced by annex 176D.
Also, the Tx and Rx test methodologies of clause 178 are re-used exactly in Annex 176C.
Also, Annex 176D has a "methodology" subclause that generally references the content in clause 179 with some variations.

It would be preferable to have all the common specifications in a single location:

- Linear fit procedure
- Transmitter waveform (coefficient step size and ranges)
- Differential and common-mode PtP specifications (separate for pluggable and for "TP5v" interfaces)
- SNDR and SNR_ISI
- RLM
- Jitter
- ERL (most parameters are common) and dERL
- Receiver interference tolerance (separate calibration methods for pluggable interfaces and for "TP5v" interfaces, but the remainder is common), jitter tolerance, amplitude tolerance.

This should be done with appropriate parameterization to enable referencing from multiple places.

Annex 178A looks like the right place - it is currently titled "Specification methods for 200 Gb/s per lane electrical channels" but as the editor's note hints, it is considered for expansion to address other link components too (as was done in Annex 93A with the addition of ERL).

SuggestedRemedy

Create a new subclause under 178A with subclauses for the common specifications of PMDs and AUIs, and move the details of the common specs from 178, 179, and 176D to the new subclause.
Update the references.
Change the title of Annex 178A adding the words "and interfaces".
Implement with editorial license.

A presentation illustrating the result of this proposal will be submitted if necessary.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 178A SC 178A.1.3 P724 L15 # 194

Mellitz, Richard Samtec
 Comment Type TR Comment Status X

COM and ERL use iDFT to convert frequency domain s-parameters into time responses described in equation 178A-11. A source transition time of 5 ps is used in this time conversion for the ERL computation and is trending to around 4 ps for the COM computation. A frequency range needs to be chosen to minimize the Gibbs Phenomena. There can be significant error due to this for ERL or COM computation. Filtering can help, however, there is still an error. Consider the data has a sinc frequency response, the loss difference of between 53 GHz and 85 GHz with a BT filter is about 10 dB which is just about amount of filtering need to minimize this error. The loss difference between 53 GHz and 67 GHz is about 4 dB which is likely to start showing this error. Frequency extrapolation is used extend to the time step frequency however this is not sufficient to reduce the Gibbs effect from the source transition time. Frequency extrapolation often does not work well for return loss or crosstalk to reduce Gibbs.

SuggestedRemedy

Change line to:
 It is recommended that the scattering parameters be measured with a uniform frequency step from a start frequency no greater than 10 MHz to a stop frequency of at least 85 GHz.

Proposed Response Response Status O

Cl 178A SC 178A.1.4.3 P727 L42 # 197

Li, Tobey MediaTek
 Comment Type TR Comment Status X

Shaunt capacitance is defined in 93A.1.2.2

SuggestedRemedy

Change the reference of shunt capacitor C1 from 93A.1.2.2a to 93A.1.2.2

Proposed Response Response Status O

Cl 178A SC 178A.1.6 P728 L24 # 198

Li, Tobey MediaTek
 Comment Type TR Comment Status X

Transmitter equalizer is defined in 178A.1.6.1

SuggestedRemedy

Change the reference to transmitter equalizer transfer function from 178A.1.2 to 178A.1.6.1

Proposed Response Response Status O

Cl 178A SC 178A.1.7.1 P731 L41 # 407

Dawe, Piers Nvidia
 Comment Type TR Comment Status X

In today's COM, the receiver noise spectral density is a parameter: it does not depend on the channel or how the receiver is tuned. As Hossein has shown us, this is unrealistic. It matters because it gives lower loss channels credit they don't deserve, allowing some bad lower loss channels to pass that shouldn't when the right high-loss channels are passed and failed.

SuggestedRemedy

Implement shakiba_3dj_COM_02_241001 with a "typical" ENOB.

Proposed Response Response Status O

Cl 178A SC 178A.1.10.2 P737 L5 # 141

Banas, David Keysight Technologies, Inc.
 Comment Type T Comment Status X

The current definition of Ani yields an effective DER0 twice that intended, because it considers only the left tail of the distribution, while both left and right tails contribute to DER0.

SuggestedRemedy

P(-Ani) = DER0/2

Proposed Response Response Status O

Cl 178B SC 178B P740 L8 # 137

Brown, Matt Alphawave Semi
 Comment Type T Comment Status X

ILT as defined in Annex 178B is relevant only to Physical Layer implementations that include physically instantiated links with 200 Gb/s or higher per lane. This should be clarified.

SuggestedRemedy

Add new subclause 178A.1 with title "Scope" and text as follows:
 "This clause defines inter-sublayer link training (ILT) for Physical Layer implementations that include one or more inter-sublayer links (ISLs) (see 178B.2) with data rate of 200 Gb/s or higher per lane."

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 178B SC 178B.3.5.1 P746 L20 # 414

Dawe, Piers Nvidia
 Comment Type TR Comment Status X
 Precoded training pattern 1 might not be well balanced.

SuggestedRemedy

Check precoded patterns for balance. If there is a problem, change the default seed so as to rotate the pattern by a few UI to make the precoding start as intended.

Proposed Response Response Status O

Cl 178B SC 178B.4 P741 L49 # 51

Opsasnick, Eugene Broadcom
 Comment Type TR Comment Status X
 The cross-reference to the subclause with the definition of "tx_mode" is incorrect. This occurs three times in Annex 178B. On page 741, line 49, on page 742, line 16, and on page 743, line 4.

SuggestedRemedy

Change: "(tx_mode = data, see 178B.13.2.1)"
 To: "(tx_mode = data, see 178B.13.3.1)"
 with update of the hyperlink to the correct subclause in all three places.

Proposed Response Response Status O

Cl 178B SC 178B.4.2 P742 L49 # 159

Dudek, Mike Marvell
 Comment Type T Comment Status X
 "data may not be available in one interface" doesn't make sense.

SuggestedRemedy

Change to "data may not be available from one interface"

Proposed Response Response Status O

Cl 178B SC 178B.4.2 P743 L8 # 127

Brown, Matt Alphawave Semi
 Comment Type T Comment Status X

There is an editor's note pointing out that the output clock must be appropriately constrained when the source switches from local clock to recovered clock. In order for the link partner receiver to track, the phase transition should be no worse than would occur with worst case jitter. Worst case jitter is 0.05 UI peak to peak at 4 MHz. Maximum phase slope is 0.6283 UI/us.

Derivation:

$$\text{phase}(t) = 0.05 / 2 * \sin(2*\pi*f_jitter*t).$$

$$d_phase(t) / d_t = 0.05 / 2 * 2 * \pi * f_jitter \cos(2*\pi*f_jitter*t)$$

$$\max(d_phase(t) / d_t) = 0.05 \text{ UI} * \pi * 4 \text{ MHz} = 0.6283 \text{ UI} / \text{us}$$

SuggestedRemedy

For each interface that supports ILT specify the that the transmitter output clock as follows:
 The phase at the transmitter output shall deviate from the original clock at a rate no higher than 0.6283 UI / us.
 Applies to Clause 178 through Clause 183.

Proposed Response Response Status O

Cl 178B SC 178B.4.3 P744 L2 # 160

Dudek, Mike Marvell
 Comment Type T Comment Status X

The definition of path means that a link including extenders will include at least two paths and these paths will be brought up independently and move to data mode independently. If this is not the intent then the co-ordination of moving to data mode between the paths needs to be described.

SuggestedRemedy

Decide if moving to data mode independently is OK. If not then add an editor's note "Co-ordination of the move to data mode between an extender and the main path is desirable Contributions are encouraged."

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 178B SC 178B.5 P744 L16 # 117
 Brown, Matt Alphawave Semi
 Comment Type E Comment Status X
 Figure 178B-3. Use of apostrophe <> followed by "s" is for possession, which is not the case here.
 SuggestedRemedy
 Change "3's" to "3s" and "0's" to "0s"
 Proposed Response Response Status O

CI 178B SC 178B.5.4 P748 L27 # 114
 Brown, Matt Alphawave Semi
 Comment Type T Comment Status X
 Mode "PAM4" is ambiguous compared with "PAM4 with precoding".
 SuggestedRemedy
 When referencing the test pattern mode change mode "PAM4" to "PAM4 without precoding". Propagate this change throughout Annex 178B as necessary.
 Proposed Response Response Status O

CI 178B SC 178B.5.3 P745 L26 # 24
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 PRBS13 is mentioned twice, while PRBS31 is missing.
 SuggestedRemedy
 Change: "and for free-running PRBS13 and free-running PRBS13 these two symbols"
 To: "and for free-running PRBS13 and free-running PRBS31 these two symbols"
 Proposed Response Response Status O

CI 178B SC 178B.5.4 P748 L35 # 415
 Dawe, Piers Nvidia
 Comment Type TR Comment Status X
 The free-running precoded training patterns are not adequately defined.
 SuggestedRemedy
 For the 8 precoded PRBS13Q, define the pattern as the one that would be generated if the seed were as in Table 178B-1 (and see another comment), and the precoder state is set to 0. As the pattern runs across the training frame, the actual start position doesn't matter as long as the intent to avoid correlation between lanes is met. For the free-running precoded PRBS31Q, define the pattern as in 120.5.11.2.2 with the precoder state set to 0.
 Proposed Response Response Status O

CI 178B SC 178B.5.3.3 P747 L48 # 25
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 This section defined the PRBS31 behavior, but in many places (including the title) it indicates PRBS13 instead
 SuggestedRemedy
 In section 178B.5.3.3 change 6 occurrences of PRBS13 to PRBS31
 Proposed Response Response Status O

CI 179 SC 179.8.4 P244 L4 # 115
 Brown, Matt Alphawave Semi
 Comment Type E Comment Status X
 Use of possessive "PMD's" not appropriate or necessary in a technical document. Since this clause is about the PMD, it is implicit that ILT here is for the PMD.
 SuggestedRemedy
 Either change "PMD's" to "PMD" or delete "PMD's"
 Do the same in 179.9.4.1.
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 179 SC 179.9.4 P356 L39 # 403

Dawe, Piers Nvidia
 Comment Type TR Comment Status X

Supply voltages and voltage swing trend downwards over the years. This 1.2 V max has not changed since 10GBASE-KR, a long time ago. In 3ck and D1.0, C2M had 750 mV, and other C2M had 900 mV. PCIe have moved from 1.2 V to 1 V max. A high max is harmful when a receiver can ask someone else's transmitter to turn up to the max, causing the second party to suffer unnecessary NEXT in its receiver.

SuggestedRemedy

Reduce 1.2 mV to 1 V, here, in the receiver Table 179-10 and in the text in 179.9.5.2. Reduce the steady-state voltage vf max from 0.6 V to 0.5 V. Make appropriate adjustments to Av Afe Ane and eta0 in COM tables. Similarly for KR and C2C. See another comment for C2M.

Proposed Response Response Status

Cl 179 SC 179.9.4 P356 L40 # 347

Simms, William (Bill) NVIDIA
 Comment Type TR Comment Status X

Table 179-7 has the Differential pk-pk voltage (max) Transmit enabled as 1.2V. This should be reduced to 1.0V to be consistent with Vf of 0.500

SuggestedRemedy

Reduce Differential pk-pk voltage (max) to 1.0V when Transmitter enabled

Proposed Response Response Status

Cl 179 SC 179.9.4 P356 L51 # 348

Simms, William (Bill) NVIDIA
 Comment Type TR Comment Status X

Table 179-7 has Transmitter steady-state voltage, Vf (range) 0.4 to 0.6 V. This range should be reduced to 0.4 to 0.5 to be consistent with Vf of 0.500

SuggestedRemedy

change Transmitter steady-state voltage, Vf (range) to 0.4 to 0.5V

Proposed Response Response Status

Cl 179 SC 179.9.4 P357 L22 # 213

Rysin, Alexander NVIDIA
 Comment Type TR Comment Status X

J3u and JRMS measurements at TP2 are highly affected by the effects of slew rate and noise and do not reflect actual uncorrelated jitter. These effects are exacerbated by the characteristics of practical channels between TP0d and TP2 - loss and reflections, and are highly dependent on the transmitted signal amplitude. Accounting only for the faster edges does not work for practical channels at 106.25 Gbd rate and the currently proposed numbers cannot be met (and sometimes cannot be measured) even with commercial test equipment PPG. The issue was demonstrated in rysin_3dj_01a_2407.

SuggestedRemedy

Other method of uncorrelated jitter measurement should be considered.

Proposed Response Response Status

Cl 179 SC 179.9.4 P357 L22 # 404

Dawe, Piers Nvidia
 Comment Type TR Comment Status X

Our way of measuring jitter doesn't work well enough with the increased max host loss over 3ck: it is very sensitive to signal amplitude, loss to the point of observation, and allowed reflections, so it is very inaccurate. It is not clear that it can or should be fixed. Our way of defining SNDR doesn't work correctly over host loss either. This can be fixed, but "vertical and horizontal noise" act together to degrade BER: more of one goes with less of the other. Attempting to separate them out is diagnostics; it is not the standard's concern how a signal got to be the way it is, only whether it is good enough or not. See calvin_3dj_02a_2407 and successor.

SuggestedRemedy

Delete the SNDR and jitter specs. Add a VEC-like, TDECQ-like spec (see daw_3dj_01_2409) using this clause's COM reference receiver which can be implemented in a scope. Similarly for KR and C2C. Delete SNR_ISI because it is a contributor to eye opening. RLM is a contributor to eye opening defined right, too: see another comment. Define VEC and Eye Amplitude (based on the equalised scope measurement) for nominal maximum signals; don't ask the scope to resolve very small signals (same idea as SNDR being defined for the presents in Table 179-8 today, not for every possible case).

Proposed Response Response Status

Cl 179 SC 179.9.4.2 P361 L26 # 416

Dawe, Piers Nvidia

Comment Type TR Comment Status X

If we look at the signal at TP2 and its equalised eye rather than just hypothesising about it (see other comments), we probably don't need a separate RLM spec. Today, COM doesn't address RLM carefully. 3ck C2M doesn't have an equivalent; if a signal has enough nonlinearity to matter, it shows up in a worse VEC.

SuggestedRemedy

Delete the RLM spec and 179.9.4.2. See another comment for the holistic VEC-like, TDECQ-like spec that includes it.

Proposed Response Response Status

Cl 179 SC 179.9.4.3 P361 L33 # 405

Dawe, Piers Nvidia

Comment Type TR Comment Status X

SNR_ISI is not needed as a separate spec: it is a component of eye opening. There is no need for a not-quite-consistent special equalizer with its special Nb for this.

SuggestedRemedy

Delete the SNR_ISI section and the editor's note. See other comments and dawe_3dj_01_2409 for the holistic VEC-like, TDECQ-like spec that includes it.

Proposed Response Response Status

Cl 179 SC 179.9.4.4 P361 L52 # 93

Ran, Adeo Cisco Systems, Inc.

Comment Type T Comment Status X

The specification of AC-common mode voltage is "all but 1e-4 of the measured distribution". This does not prevent extreme spikes of common mode noise to occur in a transmitter output as long as they are not too frequent.

It is impossible to design a receiver that can handle unspecified levels of occasional common mode noise without creating errors. Therefore we should assume that the current specification can cause errors in the receiver, currently at a probability of 1e-4. These errors can occur in addition to ones that are currently modeled by COM. Additionally, they can be correlated and cause unexpected FEC failures.

We should not allow potential sources of errors that are not budgeted to have such high probability.

The suggested probably of 1e-7 is low enough to enable it to be used for all interfaces. This increases the measurement time, but the specification is not for specific points in the pattern, so measurement can use the whole pattern and be very fast.

SuggestedRemedy

Change the specification to be all but 1e-7 of the measured distribution, from 5e-6 to 1-5e-6 of the cumulative distribution.

Use the same definition for KR, C2C, and C2M. Implement with editorial license.

Proposed Response Response Status

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 179 SC 179.9.4.4 P361 L53 # 94

Ran, Adeo Cisco Systems, Inc.

Comment Type T Comment Status X

The common-mode measurement method is not specified in detail; It is unclear what the "measured distribution" represents. The distribution can depend on the measurement method, e.g., whether or not whether the sampling is synchronous with the clock, the number of samples per UI and the sampling phase.

For example, sampling once per PRBS13Q repetition at a fixed point (as in the measurement of differential noise used in SNDR) may miss common-mode that is correlated with the signal; conversely, capturing a test pattern with many times per UI can cause large enough population to create a distribution from only part of the test pattern, but may miss events at other parts in the test pattern.

We should protect against having excessive noise anywhere within a UI and anywhere in the test pattern. The suggested change ensures that, and allows either synchronous or asynchronous measurement.

SuggestedRemedy

Add a sentence that the distribution is created from measurements over the whole PRBS13Q test pattern, that include between 2 to 3 samples per UI.

Proposed Response Response Status O

CI 179 SC 179.9.4.6 P362 L16 # 400

Dawe, Piers Nvidia

Comment Type TR Comment Status X

As explained in other comments (and see daw_3dj_01a_2406), up to 3ck the SNDR spec acted together with the jitter spec and others to protect the link performance - but we don't have a satisfactory way of measuring jitter at today's speeds and losses with reasonable reflections. Basically, measurements can't tell jitter from noise, and trying to separate the two things out "leaves margin on the table". See calvin_3dj_02a_2407 and successor.

SuggestedRemedy

Delete the SNDR section. Add a VEC-like, TDECQ-like spec using this clause's COM reference receiver which can be implemented in a scope, as in daw_3dj_01_2409. Similarly for KR and C2C.

Proposed Response Response Status O

CI 179 SC 179.9.4.6 P362 L51 # 206

Healey, Adam Broadcom Inc.

Comment Type T Comment Status X

It is stated that SNDR "shall meet the requirement when the transmitter equalization is set to each of the initial conditions defined in Table 179-8." The COM reference transmitter will not meet this requirement and it therefore seems unreasonable to impose it on real transmitters.

SuggestedRemedy

Define the SNDR requirement to be relative to what COM reference transmitter will provide under similar conditions (as is done for v_f , R_{peak} , and ERL). A contribution will be provided with details about the proposed method.

Proposed Response Response Status O

CI 179 SC 179.9.4.7 P363 L1 # 401

Dawe, Piers Nvidia

Comment Type TR Comment Status X

Measuring jitter separately to other impairments relies on a better slew rate to noise ratio than we have at the observation point, and better than what is needed to make good links. calvin_3dj_01b_2407 shows that most of what is measured is not jitter. Also see calvin_3dj_02a_2407 and successor, and zivny_3dj_01_2409 which does not establish if any of the jitter measurements give measure the right thing.

SuggestedRemedy

Delete the jitter section. Add a VEC-like, TDECQ-like spec using this clause's COM reference receiver which can be implemented in a scope, as in daw_3dj_01_2409. Similarly for KR and C2C.

Proposed Response Response Status O

CI 179 SC 179.9.4.9 P364 L4 # 204

Healey, Adam Broadcom Inc.

Comment Type T Comment Status X

Equation (179-9) and Figure 179-4 do not agree.

SuggestedRemedy

In Equation (179-9), change " $4 \leq f < 40$ " to " $4 \leq f < 44$ ".

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 179 SC 179.9.4.10 P364 L46 # 205
 Healey, Adam Broadcom Inc.
 Comment Type T Comment Status X
 Equation (179-10) and Figure 179-5 do not agree.
 SuggestedRemedy
 In Equation (179-10), change "6(f-12.89)/(35-12.89)" to "5(f-12.89)/(35-12.89)". Make the same change to Equation (179-20).
 Proposed Response Response Status O

Cl 179 SC 179.9.5 P365 L39 # 95
 Ran, Adeo Cisco Systems, Inc.
 Comment Type T Comment Status X
 The words "each lane" are not helpful for "signaling rate". All specifications hold for each lane - signaling rate is not special. Also it cannot be aggregated (unlike power and bit rate).
 This was corrected in D1.2 in most places in the electrical clauses, but these words still appear in Table 179-10, Table 176D-3, and Table 176D-4.
 SuggestedRemedy
 Delete "each lane" from the signaling rate in the 3 tables mentioned.
 Proposed Response Response Status O

Cl 179 SC 179.9.5 P365 L40 # 349
 Simms, William (Bill) NVIDIA
 Comment Type TR Comment Status X
 Table 179-10 has the Amplitude tolerance set to 1.2V. This should be reduced to 1.0V to be consistent with Vf reduced to 0.5V
 SuggestedRemedy
 Change Amplitude tolerance to 1.0V
 Proposed Response Response Status O

Cl 179 SC 179.9.5.2 P366 L3 # 96
 Ran, Adeo Cisco Systems, Inc.
 Comment Type T Comment Status X
 Compliance with receiver amplitude tolerance is defined in terms of a test with a specific amplitude which has an associated "shall". This test can either pass or fail. But the requirement in Table 179-10 is in terms of voltage.
 This is how it's been for a long time - but it can be improved.

The test would better be defined as having a parameter, A_0, which is the PtP amplitude at preset 1.
 The test result would be the maximum A_0 that the DUT can tolerate. Compliance will be defined as having the maximum no lower than 1200 mV - which matches Table 179-10 as part of the normative requirements.

This would be more like the way tests are performed in many practical cases (e.g. checking for margin over the specification).

The definition of amplitude tolerance in 176D.7.11 was written in a similar manner to this proposal.

If accepted, this change should be applied in KR and C2C as well.

SuggestedRemedy
 Rewrite the definition of amplitude tolerance based on the definition in 176D.7.11.
 Implement for CR, KR, and C2C, with editorial license.

Proposed Response Response Status O

Cl 179 SC 179.9.5.2 P366 L4 # 406
 Dawe, Piers Nvidia
 Comment Type TR Comment Status X
 Signal Vpkpk are defined and measured and calibrated with PRBS13Q. When used for stressed input testing, the signal is changed to PRBS31Q. This is settled policy. The envelope of the signal depends on the pattern, the loss to the observation point and the Tx emphasis. These are known, so the dependency is known.

SuggestedRemedy
 Assuming that the intent is a 1 V swing at the silicon, the Vpkpk for calibration (with PRBS13Q) at the MCB output is a little less. Add a row to the table for this voltage.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 179 SC 179.9.5.2 P366 L4 # 350
 Simms, William (Bill) NVIDIA
 Comment Type **TR** Comment Status **X**
 Amplitude tolerance set to 1.2V. This should be reduced to 1.0V to be consistent with Vf reduced to 0.5V
 SuggestedRemedy
 Change Amplitude tolerance to 1.0V
 Proposed Response Response Status **O**

Cl 179 SC 179.9.5.3 P366 L30 # 97
 Ran, Adeo Cisco Systems, Inc.
 Comment Type **TR** Comment Status **X**
 Test channel and Cable assembly insertion loss at 53.125 GHz are TBD.
 Since we have the die-to-die maximum loss of 40 dB, and the host channel ILdd allocation for each host class, the high-loss test channel ILdd should be straightforward.
 The low-loss test channel is similar but with the minimum channel parameters in Table 179A-3.
 SuggestedRemedy
 Specific numbers will be provided.
 Proposed Response Response Status **O**

Cl 179 SC 179.9.5.3.3 P367 L16 # 208
 Healey, Adam Broadcom Inc.
 Comment Type **T** Comment Status **X**
 Now that the host channel model is included in the calculation of COM defined in Annex 178A, it is no longer necessary to treat the concatenation of host channels as a separate step in the process. It is now simply a matter of stating which parameters are to be used to calculate the host channel model, or that the model is to be omitted.
 SuggestedRemedy
 Consolidate items a) and b) into the following basic statements. First, the test channel is measured between the Tx and Rx test references shown in Figure 110-3b. Second, that COM is calculated using the the receiver host channel, package, and device models in Table 179-16 corresponding to the class of the receiver under test. A third statement, conditional on different "tests" being defined for a given host class, is that the COM is calculated for all of the tests defined for a given host class and the COM value for the test channel is taken to be the lowest value from the tests. All other information in items a) and b) is redundant with the content of Annex 178A.
 Proposed Response Response Status **O**

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 179 SC 179.9.5.3.3 P367 L38 # 98

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The calibration of the additional noise in steps f-h of the procedure in 179.9.5.3.3 is quite complicated.

It is related to the fact that compliance with receiver interference tolerance is defined in terms of a test with a specific COM target and a binary result (pass/fail).

It can be simplified if instead of describing how to calibrate the noise in order to reach the exact COM value required for passing, the test result would be defined as the minimum COM that the DUT requires in order to meet the required block error ratio; and COM is calibrated by additive noise with the appropriate spectrum.

Compliance can then be defined as having the test result (minimum COM) no higher than 3 dB.

This is simpler to describe and more like the way tests are performed in many cases (e.g. checking for margin over the specification).

If accepted, this change should be applied in KR, C2C, and C2M as well.

SuggestedRemedy

It is proposed to rewrite steps f-h and the test procedure to make the result of the test a numeric value, namely, the minimum COM required by the DUT to meet the block error ratio. The calculation of COM still uses the value of sigma_ne in equation 179-14 and the noise is added per 179.9.5.3.4. The Rx specification would then become "COM_min <= 3 dB".

A similar change should be implemented in receiver tests for KR and C2C where white noise is added near the Rx.

Do either of the following, based on the CRG's preference

A. Implement the above with editorial license

B. Add an editor's note stating that there was support to change the result of the test to a minimum COM value, but a detailed proposal is required for implementing it in the draft.

Proposed Response Response Status O

Cl 179 SC 179.9.5.3.3 P368 L14 # 209

Healey, Adam Broadcom Inc.

Comment Type T Comment Status X

Equation (179-13) is inconsistent with the definition of transmitter output noise in Annex 178A.

SuggestedRemedy

A contribution will be provided with detailed changes to align this equation with the content of Annex 178A.

Proposed Response Response Status O

Cl 179 SC 179.9.5.3.4 P369 L22 # 99

Ran, Adeo Cisco Systems, Inc.

Comment Type T Comment Status X

Figure 179-6 is empty.
Equations 179-17 through 179-19 are identical to equations 162-15 through 162-17 respectively, and are written with fb as a parameter, but the values of f1 and f2 are fixed in GHz. Therefore the figure should be the similar to Figure 162-6 but not identical.

It is not clear whether f1 and f2 should be scaled to the new fb. If they are, then the figure would be the same as Figure 162-6, and the equations and figure can be replaced with references to clause 162.

The suggested remedy assumes that f1 and f2 are fixed (not scaled).

SuggestedRemedy

Create Figure 179-6 based on the equations.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 179 SC 179.9.5.4 P349 L42 # 91

Ran, Adee Cisco Systems, Inc.

Comment Type T Comment Status X

Compliance with receiver jitter tolerance is defined in terms of a test with a specific jitter profile and a binary result (pass/fail). This does not provide a clear means of assessing how much margin a DUT has. For this test, the margin should be in terms of jitter stress, not in terms of the block error ratio achieved (which is a likely misunderstanding).

The jitter stress definition has been like that for a long time - and should be improved.

The test would better be defined based on a parameter, SJ_0, which is the SJ PtP amplitude at 40 MHz; and all jitter test cases are defined based on this parameter (using the same profile as today, but scaled by SJ_0).

The test result would be the maximum SJ_0 that the DUT can tolerate. Compliance will be defined as having the maximum no lower than 0.05 UI - which can be put in Table 179-10 as part of the normative requirements.

This would allow defining the margin over the specification in a standardized way

If accepted, this change should be applied in KR, C2C, and C2M as well.

SuggestedRemedy

Rewrite the definition of jitter tolerance as a value rather than a procedure. Change the test procedure to use a parameter SJ_0 as described in the comment.

Change the value of "jitter tolerance" in Table 179-10 from "table 179-12" to the minimum SJ_0 required, 0.05 UI. Delete the test requirement ("shall") from the procedure.

Implement for CR, KR, C2C, and C2M, with editorial license.

Proposed Response Response Status O

Cl 179 SC 179.9.5.4.2 P370 L40 # 418

Dawe, Piers Nvidia

Comment Type T Comment Status X

Missing jitter tolerance frequency point ("case")

SuggestedRemedy

Insert a case at 0.1333 MHz, 1.5 UI. Similarly in Table 176D-10.

Proposed Response Response Status O

Cl 179 SC 179.11 P372 L23 # 100

Ran, Adee Cisco Systems, Inc.

Comment Type TR Comment Status X

The four cable assembly classes are mentioned here and described as differing in only their maximum insertion loss, with reference to 179.11.2, but there is no indication of the classes there. The max Nyquist ILdd per class are listed in Table 179-13.

Also, there is nothing in this draft about cable reach. In previous standards there was some indication of the reach provided by the cable.

It would be helpful for readers to have in this subclause a table that lists the maximum reach and Nyquist ILdd for each cable assembly class. This is more important than the existing dashed list of CR1/CR2/CR4/CR8; the cable types per width are described in detail in Annex 179C and Annex 179D.

The suggested remedy is based on slide 5 in https://www.ieee802.org/3/dj/public/23_07/tracy_3dj_01a_2307.pdf with lengths interpolated between 1 m and 2 m.

SuggestedRemedy

Change the reference from 179.11.2 to Table 179-13.
 In Table 179-13, create four columns for CA-A through CA-D. Move the "Insertion loss at 53.125 GHz, ILdd (max)" values to these columns.
 Add a row with expected reach in meters: CA-A: 1, CA-B: 1.33, CA-C: 1.66, CA-D: 2.
 Make other parameters common to all classes (straddled cells).

Proposed Response Response Status O

Cl 179 SC 179.11.3 P374 L47 # 101

Ran, Adee Cisco Systems, Inc.

Comment Type TR Comment Status X

Cable assembly ERL parameters N and Nbx are TBD.
 In 162.11.3 the values were 4500 and 0 respectively. In 802.3dj, the UI is halved and the maximum length is assumed to be the same (2 m for CA-D class).

SuggestedRemedy

Use N=9000 and Nbx=0.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 179 SC 179.11.5 P375 L15 # 102

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

Differential-mode to common-mode insertion loss equation is TBD. The reference in the text is to an equation in clause 162.

The parameter name in 178.10.5 was changed to "mode conversion insertion loss" to cover both ILcd and ILdc. It should be applied here too.

In 802.3ck the specification of this parameter are the same in KR (163.10.5) and CR (162.11.5). Therefore we can use the same equation and figure as in KR (178.10.5).

SuggestedRemedy

Rename the parameter to "mode conversion insertion loss" and use the same equation and figure as in 178.10.5. Implement with editorial license.
Change the reference in the text to point to the correct equation and figure.

Proposed Response Response Status O

Cl 179 SC 179.11.7.1 P378 L34 # 351

Simms, William (Bill) NVIDIA

Comment Type TR Comment Status X

Table 179-17 has Ane set to 0.578V which is consistent with 0.6Vf but should be reduced to 0.482 to match Vf of 0.5V

SuggestedRemedy

Reduce Ane to 0.482

Proposed Response Response Status O

Cl 179 SC 179.11.7.2 P359 L46 # 92

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The host PCB lengths for each host designation in Table 179-18 are TBD. These values are required for calculation of COM.

Now that we have a host PCB model, The lengths should be defined such that, combined with a suitable reference package and mated test fixture, the ILdd would match the "TP0d to TP2 or TP3 to TP5" values in Table 179A-1.

It is suggested to assume package class A for host class HL, and package class B for host classes HN and HH.

The package class and trace length per host class should be added to Table 179-18. It would be preferable to transpose it such that HL, HN, and HH would be the columns.

SuggestedRemedy

A detailed proposal for the table content is planned.

Proposed Response Response Status O

Cl 179 SC 179.11.7.2 P380 L17 # 68

Ran, Adeo Cisco Systems, Inc.

Comment Type ER Comment Status X

"mated test fixture" - it is "fixtures" everywhere else.

SuggestedRemedy

Change to "mated test fixtures"

Proposed Response Response Status O

Cl 179A SC 179A.4 P774 L12 # 161

Dudek, Mike Marvell

Comment Type T Comment Status X

TP5 should be TP5d in Table 179A-1 as stated in the text.

SuggestedRemedy

Change TP5 to TP5d

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 179A SC 179A.5 P698 L # 308

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Transmitter jitter specifications is ineffective and. Not sensitive for farend TP1a specifications as was demonstrtd by Rysin_3dj_01_2407.pdf
It makes no sense to use transmit jitter at TP1a when TP1a is actually at receiver pin, and what receiver care about is VEO, VEC, and possibly EW.

SuggestedRemedy

Replace Ouput jitter and SNDR with, see ghiasi_01_2407
VEO=8 mV
VEC=10.7 dB
If you want jitter then we should consider adding EW.

Proposed Response Response Status O

Cl 179A SC 179A.5 P774 L34 # 85

Ran, Adee Cisco Systems, Inc.

Comment Type TR Comment Status X

Equations 179A-1 and 179A-2 have "TP2d" and "TP3d" which should be TP2 and TP3 (there is no "d" version). Also in the parameter list.

SuggestedRemedy

Change TP2d to TP2, and TP3d to TP3, in the equation and parameter list.

Proposed Response Response Status O

Cl 179A SC 179A.5 P775 L7 # 86

Ran, Adee Cisco Systems, Inc.

Comment Type ER Comment Status X

In the "ILddCA,max (dB)" columns, the content should be numbers, and the cable assembly class should be in parentheses.

SuggestedRemedy

per comment.

Proposed Response Response Status O

Cl 179A SC 179A.5 P775 L22 # 87

Ran, Adee Cisco Systems, Inc.

Comment Type TR Comment Status X

"CA-Min (16)"
The value 16 is defined only here (Table 179A-3—Minimum Insertion loss budget values at 53.125 GHz). This is a budget table in an informative annex about "channel parameters associated with test points TP0d and TP5d" - not the right place.
This should be a normative requirement for cable assemblies.
We currently have a minimum loss for cable assemblies as a TBD equation in 179.11.2. If no equation is provided, we should (at least for the time being) have a normative minimum loss at 53.125 GHz.

SuggestedRemedy

Replace the equation in 179.11.2 with a value of 16 dB at 53.125 GHz, with editorial license. Change the references to "ILdd_CA,min" from Table 179A-3 to 179.11.2 (including in Table 179A-3 itself).

Proposed Response Response Status O

Cl 179A SC 179A.5 P776 L13 # 88

Ran, Adee Cisco Systems, Inc.

Comment Type ER Comment Status X

The horizontal locations of TP0d and TP5d (still) appear almost aligned with those of TP1 and TP4, but these are very different test points. This could be improved.
Also, in the mated test fixture the test points should be annotated.

SuggestedRemedy

Move the TP0d line to the left and the TP5d line to the right, flush with the transmit and receive function, respectively. Extend the arrows appropriately.

In the mated test fixtures part of the diagram, add TP1 and TP2 labels on the top and TP4 and TP5 labels on the bottom, or in another way if preferred.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 179A SC 179A.5 P777 L28 # 309

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Min channel loss considering 2.45 dB connector loss is less than one MCB loss, where our assumption always has been the min loss is one MCB loss

SuggestedRemedy

Given the MCB loss is 2.7 dB and connector loss is 2.45 dB the total loss become 5.15 dB. In Figure 179A-3 and other figure where host channel is labeled is actually host channel + connector

Proposed Response Response Status W

[Editor's note: Changed clause/subclause from 176E/176E.4.4 to 179A/179A.5.]

Cl 179B SC 179B.2 P778 L12 # 310

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Figure is not visible just the labels are visible

SuggestedRemedy

Please use an import that is visible in pdf

Proposed Response Response Status O

Cl 179B SC 179B.4.1 P747 L47 # 34

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The signaling rate and reference receiver bandwidth have been adopted. (This was addressed by comment #442 against D1.1, but the resolution was not fully implemented).

SuggestedRemedy

Replace TBDs: f_b=106.25 GBd and f_r=0.55*f_b.

Proposed Response Response Status O

Cl 179B SC 179B.4.1 P782 L12 # 311

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Figure is not visible just the labels are visible

SuggestedRemedy

Please use an import that is visible in pdf

Proposed Response Response Status O

Cl 179B SC 179B.4.2 P783 L2 # 89

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

ERL is currently defined without a specified reference impedance. This means that the 100 Ohm specified for s-parameter measurements in 178A.1.3 is used.

But test fixtures transmission lines should be designed for impedance matching with the connectors which are practically lower impedance (92.5 Ohm is typical). Otherwise, when connected to boards or cables with 92.5 Ohms they will have a reflection, which will degrade all results (frequency and time domain)

Using a different reference impedance for measuring the test fixtures will encourage design with the correct impedance.

The suggested remedy is to specify a reference impedance of 92.5 Ohm differential for test fixture ERL. Optionally, this should apply to all test fixture S-parameter-based specifications.

SuggestedRemedy

Add an exception to the test fixture ERL calculation to use an impedance of 92.5 Ohm, with editorial license.

Proposed Response Response Status O

Cl 179C SC 179C.2 P796 L35 # 344

Kocsis, Sam Amphenol

Comment Type E Comment Status X

Editor's note is no longer needed

SuggestedRemedy

See contribution kocsis_3dj_01_2411

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 179C SC 179C.2.1 P796 L51 # 332
 Kocsis, Sam Amphenol
 Comment Type E Comment Status X
 SFF-TA-1031 Rev 1.0 does not include SFP224
 SuggestedRemedy
 Add an Editor's note: The reference for SFP224 does not currently include 200G per lane specificatoins but it's expected to include before publication of this standard.
 Proposed Response Response Status O

Cl 179C SC 179C.2.2 P798 L29 # 334
 Kocsis, Sam Amphenol
 Comment Type T Comment Status X
 Figure 179C-4 is missing
 SuggestedRemedy
 Add for SFP-DD224 PMD receptacle from kocsis_3dj_01_2411 on slide TBD
 Proposed Response Response Status O

Cl 179C SC 179C.2.1 P797 L11 # 330
 Kocsis, Sam Amphenol
 Comment Type T Comment Status X
 Figure 179C-1 is missing
 SuggestedRemedy
 Add for SFP224 cable assembly plug from kocsis_3dj_01_2411 on slide TBD
 Proposed Response Response Status O

Cl 179C SC 179C.2.3 P798 L42 # 337
 Kocsis, Sam Amphenol
 Comment Type E Comment Status X
 SFF-TA-1027 Rev 1.0 does not include QSFP224
 SuggestedRemedy
 Add an Editor's note: The reference for QSFP224 does not currently include 200G per lane specificatoins but it's expected to include before publication of this standard.
 Proposed Response Response Status O

Cl 179C SC 179C.2.1 P797 L28 # 331
 Kocsis, Sam Amphenol
 Comment Type T Comment Status X
 Figure 179C-2 is missing
 SuggestedRemedy
 Add for SFP224 PMD receptacle from kocsis_3dj_01_2411 on slide TBD
 Proposed Response Response Status O

Cl 179C SC 179C.2.3 P799 L12 # 335
 Kocsis, Sam Amphenol
 Comment Type T Comment Status X
 Figure 179C-5 is missing
 SuggestedRemedy
 Add for QSFP224 cable assembly plug from kocsis_3dj_01_2411 on slide TBD
 Proposed Response Response Status O

Cl 179C SC 179C.2.2 P798 L15 # 333
 Kocsis, Sam Amphenol
 Comment Type T Comment Status X
 Figure 179C-3 is missing
 SuggestedRemedy
 Add for SFP-DD224 cable assembly plug from kocsis_3dj_01_2411 on slide TBD
 Proposed Response Response Status O

Cl 179C SC 179C.2.3 P799 L27 # 336
 Kocsis, Sam Amphenol
 Comment Type T Comment Status X
 Figure 179C-6 is missing
 SuggestedRemedy
 Add for QSFP224 PMD receptacle from kocsis_3dj_01_2411 on slide TBD
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 179C SC 179C.2.4 P799 L36 # 338
 Kocsis, Sam Amphenol
 Comment Type E Comment Status X
 QSFP-DD MSA Revision to 7.?
 SuggestedRemedy
 Update QSFP-DD MSA Revision to 7.1
 Proposed Response Response Status O

Cl 179C SC 179C.2.5 P800 L41 # 342
 Kocsis, Sam Amphenol
 Comment Type T Comment Status X
 Figure 179C-9 is missing
 SuggestedRemedy
 Add for OSFP1600 cable assembly plug from kocsis_3dj_01_2411 on slide TBD
 Proposed Response Response Status O

Cl 179C SC 179C.2.4 P799 L52 # 339
 Kocsis, Sam Amphenol
 Comment Type T Comment Status X
 Figure 179C-7 is missing
 SuggestedRemedy
 Add for QSFP-DD1600 cable assembly plug from kocsis_3dj_01_2411 on slide TBD
 Proposed Response Response Status O

Cl 179C SC 179C.2.5 P801 L12 # 343
 Kocsis, Sam Amphenol
 Comment Type T Comment Status X
 Figure 179C-10 is missing
 SuggestedRemedy
 Add for OSFP1600 PMD receptacle from kocsis_3dj_01_2411 on slide TBD
 Proposed Response Response Status O

Cl 179C SC 179C.2.4 P800 L13 # 340
 Kocsis, Sam Amphenol
 Comment Type T Comment Status X
 Figure 179C-8 is missing
 SuggestedRemedy
 Add for QSFP-DD1600 PMD receptacle from kocsis_3dj_01_2411 on slide TBD
 Proposed Response Response Status O

Cl 179C SC 179C.3.1 P802 L8 # 187
 D'Ambrosia, John Futurewei, U.S. Subsidiary of Huawei
 Comment Type TR Comment Status X
 Looks like cut / paste error
 Reference to Annex 162C is incorrect for Annex 179C.3.1
 Wrong PMDs are referenced
 SuggestedRemedy
 Correct 1st sentence to
 The supplier of a protocol implementation that is claimed to conform to Annex 179C, MDIs
 for
 200GBASE-CR1, 400GBASE-CR2, 800GBASE-CR4, and 1.6TBASE-CR8 shall complete
 the following protocol
 implementation conformance statement (PICS) proforma.
 Proposed Response Response Status O

Cl 179C SC 179C.2.5 P800 L22 # 341
 Kocsis, Sam Amphenol
 Comment Type E Comment Status X
 OSFP MSA Revision to 5.0?
 SuggestedRemedy
 Update OSFP MSA Revision to 5.1
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 179D SC 179D.1.1 P805 L15 # 162

Dudek, Mike Marvell
 Comment Type T Comment Status X

Table 179D-2 should also have the QSFP-DD1600 to OSFP1600 just as tables 179D-3, 179D-4 and 179D-5 do, otherwise it is implied that for some reason that connector combination can't be used for 200GBASE-CR1.

SuggestedRemedy

Add a row for QSFP-DD1600 to OSFP1600 with 8 supportable PMDs

Proposed Response Response Status O

Cl 180 SC 180.1 P389 L46 # 327

Nicholl, Gary Cisco Systems
 Comment Type E Comment Status X

Is there a reason that "90-Time synchronization" was added as the last row in the Table 180-1. According to "https://www.ieee802.org/3/dj/public/24_09/nicholl_3dj_01a_2409.pdf" , slide 24, it should have been added at the top of the table. Similar comment for Table 180-2, 180-3, 180-4. and against equivlanet tables in clauses 178, 179, 181, 182, 183, 185 and 187.

SuggestedRemedy

Move "90-Time synchronization" row to the top of Table 180-1 in accordance with "https://www.ieee802.org/3/dj/public/24_09/nicholl_3dj_01a_2409.pdf" , slide 24. Similar change to Table 180-2, 180-3, 180-4, and to equivalent tables in clauses 178, 179, 181, 182, 183, 185 and 187.

Proposed Response Response Status O

Cl 180 SC 180.1 P389 L49 # 69

Ran, Adeo Cisco Systems, Inc.
 Comment Type E Comment Status X

The text in footnote b, "If one or two 200GAUI-n is implemented in a PHY", has a numeric mismatch (two / is).

The fact that one or two AUIs can be included is mentioned in footnote c. Footnote b is a condition for having additional PMAs, and does not need to repeat what footnote c states.

Also, footnote c uses "instantiated" instead of "implemented" when talking about the same thing. We should be consistent.

In D1.2, for KR and CR PHYs (where only one AUI can be included in a PHY), this statement was changed to "If a 200GAUI-n is implemented in a PHY <...>". This wording is correct for all PHYs.

There are 11 instances of "if one or two" with 200GAUI-n, 400GAUI-n, 800GAUI-n, and 1.6TAUI-n.

SuggestedRemedy

Change "If one or two" to "If a" (in this instance, "If a 200GAUI-n is implemented in a PHY"). Apply similarly for all instances.

Change "implemented in a PHY" to "instantiated in a PHY" (19 instances).

Proposed Response Response Status O

Cl 180 SC 180.2 P393 L37 # 433

Mi, Guangcan Huawei Technologies Co., Ltd

Comment Type TR Comment Status X

"A PMD is expected to meet the block error ratio specifications in 174A.6, measured at a PMA, withBERadded equal to 6.4×10^{-5} . the statement of measured at a PMA may not be sufficient, for the following reason. The optical PMD interfaces with PMA at both side of the link, shown in Figure 180-2. Checking across the clauses, Figure 176C-2 and Figure 176D-2 showed both AUI C2C and AUI C2M interface with PMA. therefore, a user could use the PMA before an C2C/C2M channel as transmitter and the PMA after an C2C/C2M channel as receiver, and still be measuring the block error ratio of an optical PMD at PMA. However in this case, employing BERadded would mean double counting the error allocation to C2C/C2M. It is therefore suggested to either specify by wording or provide an illustrative drawing.. "

SuggestedRemedy

Add description where appropriate, such as "the test pattern should be generated by the PMA sub-layer immediately before the PMD interface at the transmitting side, while the error ratio measured by the PMA sublayer immediately after the PMD interface at the receiving side." A figure may also be helpful, will provide in a contribution.

Proposed Response Response Status O

Cl 180 SC 180.2 P393 L40 # 434

Mi, Guangcan Huawei Technologies Co., Ltd

Comment Type TR Comment Status X

BERadded at PMA being $6.4e-5$, which corresponds to Table 174A-1, adding two C2C and two C2M allocation. BER added at PCS being $3.2e-5$, which doesn't seem write. Need to recheck.

SuggestedRemedy

If the test pattern is generated by and transmitted from the PCS layer at the transmitting side, then there should be no BER_added needed. If the test pattern is generated by and transmitted from the PMA layer at the transmitting side, where the PMA is the PMA immediately before the PMD interface, then BER_added of $3.2e-5$, equivalent to a two-part AUI link at the receiver side only, seems correct. Some clarification will be good.

Proposed Response Response Status O

Cl 180 SC 180.2 P393 L45 # 259

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Direct block error measurement require Golden HW receiver that may not exist and even then may introduce its own set of block erros.

SuggestedRemedy

Instead the recommendation is to measure block TDECQ where block TDECQ is by capturing 10x the SSPRQ waveform and only using worst 10% of block data for "Block TDECQ" limit. When all the blocks data are used the reporting value would be "Average TDECQ". Initial conversation with Oscope supplier is that this measurement is feasible and we won't need to change any limit or introduce any new test limit. The current average TDECQ will be changed to "Block TDECQ". See Ghiasi_3dJ_02_2411

Proposed Response Response Status O

Cl 180 SC 180.5.1 P396 L1 # 250

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

The Signal_OK and ILT fuction are hanging in the air and not clear how they propgate from TX to RX

SuggestedRemedy

Just like global_PMD_signal_detect that touches all 4 PMD Receive function the ILT block should also touch/connect to all 4 PMA transmit function and PMA Receive function

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 180 SC 180.6 P398 L36 # 128

Brown, Matt Alphawave Semi

Comment Type T Comment Status X

In addition to mapping signal lanes to fiber positions within a PHY, the fibers such that the transmitting signal lane number (SLi) is the same as the receiving signal lane number (DLi) at the other end of the fiber. See Figure 180-2 and Figure 178B-1. The requirement should be written such that it is relevant to the break-out cases defined in Annex 180A.

SuggestedRemedy

In 180.6 add the following paragraph:

"Each fiber between the transmitter of one PHY and the receiver of another PHY shall connect to the same signal lane number. For example, a fiber connects SL1 at the transmitting end to DL1 at the receiving end."

Do the same for 182.6.

Proposed Response Response Status O

Cl 180 SC 180.7.1 P399 L26 # 70

Ran, Adeo Cisco Systems, Inc.

Comment Type E Comment Status X

The words "each lane" are not appropriate for "signaling rate", since it cannot be aggregated (unlike power and bit rate).

This was corrected in D1.2 in most places in the electrical clauses, but these words still appear in optical clauses (8 instances).

This comment is specific to the signaling rate parameter; other parameters are subject of other comments.

SuggestedRemedy

Delete "each lane" from "signaling rate" in all optical Tx and Rx specifications tables. Apply in all optical PMD clauses.

Proposed Response Response Status O

Cl 180 SC 180.7.1 P399 L32 # 71

Ran, Adeo Cisco Systems, Inc.

Comment Type TR Comment Status X

The words "each lane" appear in some Tx parameters but not in others. The distinction is not clear; it seems that all specifications in Table 180-7 apply to each lane separately - but the way it is written may be interpreted otherwise (e.g. Transmitter power excursion does not have "each lane" - is it an aggregate specification?)

In Table 181-5 (WDM) there is a similar situation, but there are specific parameters that apply for the sum of all lanes (total average power, and maybe others). These should be clearly marked as such, e.g., "(total of all lanes)".

The same concern exist in Rx characteristics in Table 180-8 and Table 181-6. All seem to be per lane.

Clauses 182 and 183 are similar. This should preferably be aligned across optical clauses.

SuggestedRemedy

Delete "each lane" from the specific parameter names, and add a statement in the text above each table, stating that the transmit (or receiver) characteristics apply separately to each lane of a PMD unless specified otherwise.

Implement for both Tx and Rx across the multi-lane optical clauses (where appropriate), and also in references to the parameter names, with editorial license.

Proposed Response Response Status O

Cl 180 SC 180.7.1 P399 L48 # 227

Johnson, John Broadcom

Comment Type T Comment Status X

Transmitter power excursion (max) is TBD in Table 180-7 for all DRn PMDs

SuggestedRemedy

In existing 100G PHYs from P803.2cu, TPE(max) was chosen to give approximately 8% reduction in overshoot at OMA(max), i.e. maximum allowable OS is reduced from 22% at low OMA to ~ 14% at OMA(max).

Change TBD to 2.3 dB in Table 180-7. This results in OS at OMA(max) = 14.6%, consistent with 100G PHYs.

A supporting presentation will be submitted for the Nov plenary.

Proposed Response Response Status O

Cl 180 SC 180.7.1 P400 L10 # 72

Ran, Adee Cisco Systems, Inc.

Comment Type E Comment Status X

For RINxxOMA , it seems that the xx in this case should be 15.5 for 200G and 21.4 for other cases. But this is not clear that these are different parameters (and they have the same maximum value; does it make sense?)

Footnote c says "with "xx" referring to the value for Optical return loss tolerance.", but it should be the maximum value.

In previous PMD clauses the RIN parameter name included specific values. For example, in Table 167-7, RIN14OMA.

SuggestedRemedy

Either change footnote c to "Optical return loss tolerance (max)" and state clearly that this creates different parameters for 200G and for 400G/800G/1.6T, or preferably replace xx with numbers (separating to two rows).

Proposed Response Response Status O

Cl 180 SC 180.7.2 P401 L29 # 145

Dudek, Mike Marvell

Comment Type TR Comment Status X

There is no requirement to have the OMA of all the Tx lanes within a given limit and there is no restriction on the difference in losses between the lanes in the optical channel.

Therefore the value of Max OMA of the aggressor lanes should match the MaxOMA of the Tx. This is similar to comment 169 against Clause 181 in D1.2 which was rejected with the comment "The proposed value is incorrect for DR-2/4/8 and would only apply to multiple DR1s in a single module. " What is the justification for saying the proposed value is incorrect?

SuggestedRemedy

Change the OMA outer of each aggressor lane from 2.9dB to 4.2dB. Change this from TBD to 4.2dB in Table 181-6. Add a footnote to this row in Table 181-6 that is similar to the one in Table 180-8 " No aggressors needed for 200GBASE-DR1-2 in a single lane device. "

Proposed Response Response Status O

Cl 180 SC 180.7.2 P401 L29 # 228

Johnson, John Broadcom

Comment Type T Comment Status X

The value of Stressed receiver sensitivity (max) is nominally given by the minimum TX OMA at TDECQ(max), minus the maximum channel insertion loss and MPI+DGD penalties. Because the fibers in a DRn PHY (n>1) without breakout share the same parallel fiber cabling and connectors, the Aggressor lanes for SRS testing should be considered to have the same insertion loss as the lane under test.

SuggestedRemedy

For DRn PHYs in Table 180-8, change the value of OMAouter of each aggressor lane from 2.9 dBm to 0.9 dBm, which is equal to 4dBm TX OMA(max), minus 3dB max insertion loss, minus 0.1dB MPI+DGD penalty.

To cover the case of breakout, add text to footnote (e), "If the device is being used to breakout lower line rate PMDs as described in Annex 180A, OMAouter of each aggressor lane should be equal to the value of Outer Optical Modulation Amplitude (OMAouter), each lane (max) given in Table 180-7."

A supporting presentation will be submitted for the Nov plenary.

Proposed Response Response Status O

Cl 180 SC 180.7.2 P402 L3 # 73

Ran, Adee Cisco Systems, Inc.

Comment Type T Comment Status X

Figure 180-4 does not show the pass and fail regions for receiver sensitivity vs. TECQ. Also in Figure 181-4, Figure 182-4, and Figure 183-4.

SuggestedRemedy

Add labels (e.g. "pass region" and "fail region") in the figures to clarify.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 180 SC 180.7.3 P402 L46 # 328

Nicholl, Gary Cisco Systems

Comment Type TR Comment Status X

Note b in Table 180-9 states that "Link penalties are used for link budget calculations. They are not requirements and are not meant to be tested. This value includes an allocation of 0.1 dB for MPI and DGD penalties" If memory serves me correctly the MPI/DGD penalty of 0.1dB for DRn links was based on running the Jonathan King MPI spreadsheet with the assumption of only MPO connectors (much lower return loss) in the channel. Can the same value of penalty be assumed for a 200GBASE-DR1 PMD using a LC connector (higher return loss) ?

Table 180-12 clearly shows a very different set of allowed maximum values for each discrete reflectances in the channel for 200GBASE-DR1 versus in the channel for 400GBASE-DR2/800GBASE-DR4/1.6TBASE-DR8. It is not clear which set of values in Table 180-12 was used when calculating the worst case MPI/DGD penalty ?

I understand the desire to have a single link budget and associated MPI/DGD penalty for 200GBASE-DR1, 400GBASE-DR2, 800GBASE-DR4 and 1.6TBASE-DR8, but in that case shouldn't we use the worst case value which I assume would be for 200GBASE-DR1 with an LC connector and likely to be higher than the stated value of 0.1dB.

SuggestedRemedy

Re-run the Jonathan King MPI spreadsheet for the 200GBASE-DR1 case with an LC connector , and if the MPI/DSP penalty is greater than 0.1dB, update the penalty called out in note b and update the associated link budget in Table 180-9 for all PMDs accordingly.

Proposed Response Response Status O

Cl 180 SC 180.7.3 P404 L11 # 262

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Table 180-9 allocation for penalties covers 200G-DR which has optical return loss tolerance of 15.5 dB only because PC connectors with 35 dB RL are used. The assumed 0.1 dB MPI penalty is accurate for 400G-DR2, 800G-DR4 where APC connectors with better than 45 dB return loss used but not in case of 200G-DR where connector RL will be 35 dB.

SuggestedRemedy

Add note to 200G-DR1 with allocation for penalties increased to 0.4 dB per table 140-12 for 6 connectors and 0.2 dB incase of 4 connectors.

Proposed Response Response Status O

Cl 180 SC 180.8.3 P405 L36 # 169

Huber, Thomas Nokia

Comment Type T Comment Status X

The 'breakout applications' in Annex 180A are creating additional MDIs for the lower speed DRn PHYs. The text in this clause needs to be more clear that there are multiple MDIs. In cases where there is only one PMD using an MPO connector, we specify exactly what fiber positions are used to carry which lanes as part of the definition of the MDI. That property must also be true when a single connector provides the MDI for multiple PMDs. E.g., it's not any arbitrary set of four positions in a 12-position MPO that can compose an MDI for a 400GBASE-DR2; there are two specific sets of four positions that can do that on a module that has 800G of capacity, and only one set on a module that has 400G of capacity.

SuggestedRemedy

Rework clause 180.8.3 (and 182.8.3) to indicate that there are multiple MDIs based on different connectors and module capacities, and point to annex 180A for the details. Move the information about the mapping of PMD signals to fiber positions in the connectors and the other details about the MDIs to an annex so they don't have to be replicated in 180 and 182.

Proposed Response Response Status O

Cl 180 SC 180.8.3.1.1 P406 L2 # 220

Johnson, John Broadcom

Comment Type E Comment Status X

MDI nomenclature is inconsistent with Annex 180A here, as well as in 180.8.3.1.2 and 180.8.3.1.3.

SuggestedRemedy

Change "MDI pin" to "MDI position" in the text and tables to be consistent with nomenclature used in Annex 180A.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 180 SC 180.9.1 P410 L9 # 170
 Huber, Thomas Nokia
 Comment Type T Comment Status X
 In Table 180-16, the cross-references for the PRBS31Q, PRBS13Q, and SSPRQ patterns are incorrect; PRBS13Q is defined in 120.5.11.2.1, PRBS31Q in 120.5.11.2.2, SSPRQ in 120.5.11.2.4
 SuggestedRemedy
 Correct the references.
 Proposed Response Response Status O

Cl 180 SC 180.9.5 P376 L22 # 260
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 With concern rasied regarding block errors and if TDECQ captures jitter, need additional condition in the TDECQ setup to make sure TDECQ is representative of worst case operation
 SuggestedRemedy
 If the PMD under test has an optional AUI (C2M) the TDECQ is measured with the module in mission mode with the clock driving SSPRQ recovered from the AUI input. The AUI is operating with PRBS31Q pattern and worst case interference tolerance applied, see https://www.ieee802.org/3/dj/public/24_09/ghiasi_3dj_01a_2409.pdf
 Proposed Response Response Status O

Cl 180 SC 180.9.5 P412 L35 # 268
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(-1)=0.05 is too restricted
 SuggestedRemedy
 Recomend to increase C(-1) positive limit to +0.1 from 0.05, see ghiasi_3dj_01_2411
 Proposed Response Response Status O

Cl 180 SC 180.9.5 P412 L36 # 269
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(-2)=0.2 is too restricted given that we have C(-1)=0.5, to correct for C(-1)=-0.5 C(-2) can be as large as 0.25
 SuggestedRemedy
 Recomend to increase C(-2) positive limit to +0.25 from 0.2, see ghiasi_3dj_01_2411
 Proposed Response Response Status O

Cl 180 SC 180.9.5 P412 L37 # 270
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(1)=0.05 is too restricted in cases of fast transmitter ability to use positive tap can be very beneficial
 SuggestedRemedy
 Recomend to increase C(1) positive limit to +0.2 from 0.05 helpful on fast transmitters to reduce the BW and noise see ghiasi_3dj_01_2411
 Proposed Response Response Status O

Cl 180 SC 180.9.5 P412 L39 # 272
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps negative limit C(3)=-0.1 is too restricted and exceed limited data in the ghiasi_3dj_01_2411
 SuggestedRemedy
 Recomend to increase C(3) positive limit to -0.15 from 0.1 and C(3) negative from -0.1 to -0.15 given the data in ghiasi_3dj_01_2411 data show can be as large as 0.129
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 180 SC 180.9.5 P412 L39 # 273
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(4)=0.1 is too restricted and exceed limited data in the ghiasi_3dj_01_2411
 SuggestedRemedy
 Recommend to increase C(4) positive limit to -0.15 from 0.1 and C(4) negative from -0.1 to -0.15 given the data in ghiasi_3dj_01_2411 with some taps exceeding 0.1
 Proposed Response Response Status O

CI 180 SC 180.9.5 P412 L39 # 274
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps negative limit C(5)=-0.1 is too restricted and exceed limited data in the ghiasi_3dj_01_2411
 SuggestedRemedy
 Recommend to increase 5(4) positive limit to -0.15 from 0.1 and C(5) negative from -0.1 to -0.15 given the data in ghiasi_3dj_01_2411 with some taps exceeding -0.1
 Proposed Response Response Status O

CI 180 SC 180.9.5 P412 L39 # 271
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(2)=-0.1 and C(2)=0.2 is too restricted and exceed limited data in the ghiasi_3dj_01_2411
 SuggestedRemedy
 Recommend to increase C(2) positive limit to +0.3 from 0.2 given that C(-1)=-0.6 the follow on tap can be as much as prior tap weight. C(2) negative limit ghiasi_3dj_01_2411 data show can be as large as 0.129, recommending to increase C(2) negative limit from -0.1 to -0.2.
 Proposed Response Response Status O

CI 180 SC 180.9.5.1 P413 L12 # 229
 Johnson, John Broadcom
 Comment Type T Comment Status X
 PMD types in Table 180-19 are wrong
 SuggestedRemedy
 Change PMD types from DRn-2 to DRn in Table 180-19
 Proposed Response Response Status O

CI 180 SC 180.9.5.1 P413 L20 # 221
 Johnson, John Broadcom
 Comment Type E Comment Status X
 The nomenclature of footnote (c) in Table 180-19 should match the nomenclature in Table 180-7.
 SuggestedRemedy
 Change footnote (c) to read: "The optical return loss tolerance (max) from Table 180-7 is applied at TP2." as in footnote (c) of Table 182-19.
 Proposed Response Response Status O

CI 180 SC 180.9.11 P415 L3 # 74
 Ran, Adeo Cisco Systems, Inc.
 Comment Type ER Comment Status X
 The dashed list item "N0 and N3 are to be measured <...>" is not part of the variable list for this equation; N0 and N3 are already defined.
 SuggestedRemedy
 Move the text of this item to a regular paragraph after the list.
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 180 SC 180.9.13 P415 L28 # 300
 Ghiasi, Ali Ghiasi Quantum
 Comment Type E Comment Status X
 121.8.10 is the Wrong reference
 SuggestedRemedy
 It should be 121.8.9
 Proposed Response Response Status O

Cl 180A SC 180A.0 P807 L9 # 312
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 lower optics rate is actually lower MAC rate
 SuggestedRemedy
 Add and say lwoer MAC rate, also MAC rate to other instacnes in this clause
 Proposed Response Response Status O

Cl 180A SC 180A P807 L1 # 188
 D'Ambrosia, John Futurewei, U.S. Subsidiary of Huawei
 Comment Type TR Comment Status X
 The annex is not written in an ethernet standards approach, where it addresses the breakout implementation, and doesn't address the MDI choices of the DRx / DRx-2. Additionally, Clauses 180 and 182 are making normative statements regarding the MDIs, despite the annex then providing additinoal MDI Connector choices.
 SuggestedRemedy
 Update Annex 180A using the approach for CR MDIs used in Clause 179 and Annex 179C.
 Supporting presentation to be provided
 Proposed Response Response Status O

Cl 180A SC 180A.1 P807 L15 # 183
 Huber, Thomas Nokia
 Comment Type T Comment Status X
 The scope needs to be clear that this annex applies to PMDs that use parallel fibers, and should als be more clear that new MDIs are being specified (whether they are here or in clause 180.8.3 per other comments)
 SuggestedRemedy
 Rewrite the clause:
 This annex describes how a multi-position connceter that provides the MDI for a PMD that uses multiple fiber pairs can also be used to provide the MDIs for multiple lower speed PMDs by allocating subsets of those fiber pairs to each of the lower speed PMDs.
 Proposed Response Response Status O

Cl 180A SC 180A P807 L10 # 182
 Huber, Thomas Nokia
 Comment Type T Comment Status X
 What we call "breakout" is really about alternative MDIs for PMDs that use parallel fibers. The title should reflect that.
 SuggestedRemedy
 Change the title to "Support of multiple PMDs in a single multi-position connector"
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 180A SC 180A.2 P807 L24 # 184

Huber, Thomas

Nokia

Comment Type T Comment Status X

The text of the second and third paragraphs makes it sound like the higher-speed PMD is being broken out to lower speed ones, which is not what is really happening in these breakout scenarios

SuggestedRemedy

Rewrite the text:

The 16-position connector provides the MDI for PMDs that use 8 optical lanes (with one fiber pair per lane). This connector can also be used to provide the MDIs for multiple lower speed PMDs by allocating groups of one, two, or four fiber pairs as the MDI for each lower speed PMD.

The 12-position connector provides the MDI for PMDs that use 2 or 4 optical lanes (one fiber pair per lane), with either 8 or 4 positions, respectively unused. This connector can also be used to provide the MDIs for multiple lower speed PMDs by allocating groups of one or two fiber pairs as the MDI for each lower speed PMD.

Proposed Response Response Status O

Cl 180A SC 180A.2 P807 L24 # 329

Nicholl, Gary

Cisco Systems

Comment Type E Comment Status X

The second paragraph is referencing 16-position optical connectors and the 3rd paragraph then goes on to reference 12-position optical connectors. But the following sections then switch the order with 180A.3 referring to 12-position optical connectors and 180A.4 referring to 16-position optical connectors.

SuggestedRemedy

Suggest switching the order of the 2nd and 3rd paragraphs in 180A.2, to match the order of the subsequent subclauses 180A.3 and 180A.4.

Proposed Response Response Status O

Cl 180A SC 180A.3 P807 L35 # 185

Huber, Thomas

Nokia

Comment Type T Comment Status X

This clause should be reworked to be a complete spec for all the MDIs that use the 12-position connector. This would include the information about mapping PMD signals to fiber positions that is currently in 180.8.3

SuggestedRemedy

Reorganize the material as described.

Proposed Response Response Status O

Cl 180A SC 180A.4 P809 L1 # 186

Huber, Thomas

Nokia

Comment Type T Comment Status X

This clause should be reworked to be a complete spec for all the MDIs that use the 16-position connector. This would include the information about mapping PMD signals to fiber positions that is currently in 180.8.3

SuggestedRemedy

Reorganize the material as described.

Proposed Response Response Status O

Cl 181 SC 181.1 P420 L9 # 130

Brown, Matt

Alphawave Semi

Comment Type E Comment Status X

Acronym WDM is first introduced here in the clause but is not defined. Use same wording as provided for WDM in subclause 1.5 (base standard).

SuggestedRemedy

Change "WDM" to "Wavelength division multiplexing (WDM)"
Do the same in 183.1.

Proposed Response Response Status O

Cl 181 SC 181.2 P421 L36 # 435

Mi, Guangcan Huawei Technologies Co., Ltd

Comment Type TR Comment Status X

"A PMD is expected to meet the block error ratio specifications in 174A.6, measured at a PMA, withBERadded equal to 6.4×10^{-5} . the statement of measured at a PMA may not be sufficient, for the following reason. The optical PMD interfaces with PMA at both side of the link, shown in Figure 180-2. Checking across the clauses, Figure 176C-2 and Figure 176D-2 showed both AUI C2C and AUI C2M interface with PMA. therefore, a user could use the PMA before an C2C/C2M channel as transmitter and the PMA after an C2C/C2M channel as receiver, and still be measuring the block error ratio of an optical PMD at PMA. However in this case, employing BERadded would mean double counting the error allocation to C2C/C2M. It is therefore suggested to either specify by wording or provide an illustrative drawing.. "

SuggestedRemedy

Add description where appropriate, such as "the test pattern should be generated by the PMA sub-layer immediately before the PMD interface at the transmitting side, while the error ratio measured by the PMA sublayer immediately after the PMD interface at the receiving side." A figure may also be helpful, will provide in a contribution.

Proposed Response Response Status O

Cl 181 SC 181.2 P421 L39 # 436

Mi, Guangcan Huawei Technologies Co., Ltd

Comment Type TR Comment Status X

BERadded at PMA being $6.4e-5$, which corresponds to Table 174A-1, adding two C2C and two C2M allocation. BER added at PCS being $3.2e-5$, which doesn't seem write. Need to recheck.

SuggestedRemedy

If the test pattern is generated by and transmitted from the PCS layer at the transmitting side, then there should be no BER_added needed. If the test pattern is generated by and transmitted from the PMA layer at the transmitting side, where the PMA is the PMA immediately before the PMD interface, then BER_added of $3.2e-5$, equivalent to a two-part AUI link at the receiver side only, seems correct. Some clarification will be good.

Proposed Response Response Status O

Cl 181 SC 181.2 P421 L45 # 256

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Direct block error measurement require Golden HW receiver that may not exist and even then may introduce its own set of block erros.

SuggestedRemedy

Instead the recommendation is to measure block TDECQ where block TDECQ is by capturing 10x the SSPRQ waveform and only using worst 10% of block data for "Block TDECQ" limit. When all the blocks data are used the reporting value would be "Average TDECQ". Initial conversation with Oscope supplier is that this measurement is feasible and we won't need to change any limit or introduce any new test limit. The current average TDECQ will be changed to "Block TDECQ". See Ghiasi_3dJ_02_2411

Proposed Response Response Status O

Cl 181 SC 181.5.1 P423 L12 # 251

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

The Signal_OK and ILT fuction are hanging in the air and not clear how they propgate from TX to RX

SuggestedRemedy

Just like global_PMD_signal_detect that touches all 4 PMD Receive function the ILT block should also touch/connect to all 4 PMA transmit function and PMA Receive function

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 181 SC 181.6. P426 L17 # 75

Ran, Adee Cisco Systems, Inc.

Comment Type T Comment Status X

The NOTE says "There is no requirement to associate a particular electrical lane with a particular optical lane, as the PCS is capable of receiving lanes in any arrangement". However, with ILT, the assignment of lane numbers on the PMD service interface to wavelengths must be fixed, because precoding (which is negotiated in ILT) is implemented outside of the PMD.

Also in 183.6.

SuggestedRemedy

Change the notes in both clauses to state that, unlike some other WDM PMDs, there is a requirement to associate the PMD lanes (as defined at the service interface) with the wavelengths in the table, in order to enable the ILT function.

Proposed Response Response Status O

Cl 181 SC 181.7.1 P427 L31 # 230

Johnson, John Broadcom

Comment Type T Comment Status X

Transmitter power excursion (max) is TBD in Table 181-5 for 800GBASE-FR4-500

SuggestedRemedy

In existing 100G PHYs from P803.2cu, TPE(max) was chosen to give approximately 8% reduction in overshoot at OMA(max), i.e. maximum allowable OS is reduced from 22% at low OMA to ~ 14% at OMA(max).

Change TBD to 2.9 dB in Table 181-5. This results in OS at OMA(max) = 14.6%, consistent with 100G PHYs.

A supporting presentation will be submitted for the Nov plenary.

Proposed Response Response Status O

Cl 181 SC 181.7.2 P429 L27 # 222

Johnson, John Broadcom

Comment Type E Comment Status X

In "lanec", footnote "c" should be superscripted

SuggestedRemedy

Make "c" superscripted.

Proposed Response Response Status O

Cl 181 SC 181.7.2 P429 L32 # 231

Johnson, John Broadcom

Comment Type T Comment Status X

In 100G/L FR4 and LR4 PHYs, OMAouter of each aggressor lane is equal to the Stressed receiver sensitivity (OMAouter) plus the Difference in receive power between any two lanes (OMAouter) (max), within ±0.1dB. The same methodology should be applied to 800GBASE-FR4-500.

SuggestedRemedy

For 800GBASE-FR4-500 in Table 181-6, change the value of OMAouter of each aggressor lane from 1.9 dBm to 3.4 dBm, which is equal to -0.7 dBm SRS(max) plus 4.1 dB maximum difference in receive power between lanes.

A supporting presentation will be submitted for the Nov plenary.

Proposed Response Response Status O

Cl 181 SC 181.8 P432 L17 # 214

Stassar, Peter Huawei

Comment Type TR Comment Status X

The value for optical return loss (ORL) is the same as Tx optical return loss tolerance, which is wrong. The ORL should be the same as for 100GBASE-DR and 200GBASE-DR1.

SuggestedRemedy

In Table 181-8 change optical return loss to 27 dB minimum

Proposed Response Response Status O

Cl 181 SC 181.9.1 P434 L17 # 171

Huber, Thomas Nokia

Comment Type T Comment Status X

In Table 181-11, the cross-references for the PRBS31Q, PRBS13Q, and SSPRQ patterns are incorrect; PRBS13Q is defined in 120.5.11.2.1, PRBS31Q in 120.5.11.2.2, SSPRQ in 120.5.11.2.4

SuggestedRemedy

Correct the references.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 181 SC 181.9.5 P412 L33 # 265
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 Maximum equalizer pre-cursors equal 3 also implies that we could have 0, 1, or 2 pre-cursors
 SuggestedRemedy
 Given the intention that equalizer doesn't float repalce "Maximum equalizer pre-cursors" with "Number of equalizer pre-cursors tap" and put 3 also in the min or create table with min-value-max. Make post taps i explicit 3 to 11. Feedforward equalizer length should be listed under Value col as 15, this is not a max as there is no Min!
 Proposed Response Response Status O

CI 181 SC 181.9.5 P436 L22 # 261
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 With concern rasied regarding block errors and if TDECQ captures jitter, need additional condition in the TDECQ setup to make sure TDECQ is representative of worst case operation
 SuggestedRemedy
 If the PMD under test has an optional AUI (C2M) the TDECQ is measured with the module in mission mode with the clock driving SSPRQ recovered from the AUI input. The AUI is operating with PRBS31Q pattern and worst case interference tolerance applied, see https://www.ieee802.org/3/dj/public/24_09/ghiasi_3dj_01a_2409.pdf
 Proposed Response Response Status O

CI 181 SC 181.9.5 P436 L35 # 275
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(-1)=0.05 is too restricted
 SuggestedRemedy
 Recomend to increase C(-1) positive limit to +0.1 from 0.05, see ghiasi_3dj_01_2411
 Proposed Response Response Status O

CI 181 SC 181.9.5 P436 L36 # 276
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(-2)=0.2 is too restricted given that we have C(-1)=0.5, to correct for C(-1)=-0.5 C(-2) can be as large as 0.25
 SuggestedRemedy
 Recomend to increase C(-2) positive limit to +0.25 from 0.2, see ghiasi_3dj_01_2411
 Proposed Response Response Status O

CI 181 SC 181.9.5 P436 L37 # 277
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(1)=0.05 is too restricted in cases of fast transmitter ability to use positive tap can be very beneficial
 SuggestedRemedy
 Recomend to increase C(1) positive limit to +0.2 from 0.05 helpful on fast transmitters to reduce the BW and noise see ghiasi_3dj_01_2411
 Proposed Response Response Status O

CI 181 SC 181.9.5 P436 L39 # 281
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps negative limit C(5)=-0.1 is too restricted and exceed limited data in the ghiasi_3dj_01_2411
 SuggestedRemedy
 Recomend to increase 5(4) positive limit to -0.15 from 0.1 and C(5) negative from -0.1 to -0.15 given the data in ghiasi_3dj_01_2411 with some taps exceeding -0.1
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 181 SC 181.9.5 P436 L39 # 278
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(2)=-0.1 and C(2)=0.2 is too restricted and exceed limited data in the ghiasi_3dj_01_2411
 SuggestedRemedy
 Recommend to increase C(2) positive limit to +0.3 from 0.2 given that C(-1)=-0.6 the follow on tap can be as much as prior tap weight. C(2) negative limit ghiasi_3dj_01_2411 data show can be as large as 0.129, recommending to increase C(2) negative limit from -0.1 to -0.2.
 Proposed Response Response Status O

Cl 181 SC 181.9.5 P436 L39 # 279
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps negative limit C(3)=-0.1 is too restricted and exceed limited data in the ghiasi_3dj_01_2411
 SuggestedRemedy
 Recommend to increase C(3) positive limit to -0.15 from 0.1 and C(3) negative from -0.1 to -0.15 given the data in ghiasi_3dj_01_2411 data show can be as large as 0.129
 Proposed Response Response Status O

Cl 181 SC 181.9.5 P436 L39 # 280
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(4)=0.1 is too restricted and exceed limited data in the ghiasi_3dj_01_2411
 SuggestedRemedy
 Recommend to increase C(4) positive limit to -0.15 from 0.1 and C(4) negative from -0.1 to -0.15 given the data in ghiasi_3dj_01_2411 with some taps exceeding 0.1
 Proposed Response Response Status O

Cl 181 SC 181.9.5 P490 L22 # 290
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(-2)=0.2 is too restricted given that we have C(-1)=0.5, to correct for C(-1)=-0.5 C(-2) can be as large as 0.25
 SuggestedRemedy
 Recommend to increase C(-2) positive limit to +0.25 from 0.2, see ghiasi_3dj_01_2411
 Proposed Response Response Status O

Cl 181 SC 181.9.5 P490 L23 # 291
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(1)=0.05 is too restricted in cases of fast transmitter ability to use positive tap can be very beneficial
 SuggestedRemedy
 Recommend to increase C(1) positive limit to +0.2 from 0.05 helpful on fast transmitters to reduce the BW and noise see ghiasi_3dj_01_2411
 Proposed Response Response Status O

Cl 181 SC 181.9.5 P490 L24 # 292
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(2)=-0.1 and C(2)=0.2 is too restricted and exceed limited data in the ghiasi_3dj_01_2411
 SuggestedRemedy
 Recommend to increase C(2) positive limit to +0.3 from 0.2 given that C(-1)=-0.6 the follow on tap can be as much as prior tap weight. C(2) negative limit ghiasi_3dj_01_2411 data show can be as large as 0.129, recommending to increase C(2) negative limit from -0.1 to -0.2.
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 181 SC 181.9.5 P490 L25 # 293
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps negative limit C(3)=-0.1 is too restricted and exceed limited data in the ghiasi_3dj_01_2411
 SuggestedRemedy
 Recommend to increase C(3) positive limit to -0.15 from 0.1 and C(3) negative from -0.1 to -0.15 given the data in ghiasi_3dj_01_2411 data show can be as large as 0.129
 Proposed Response Response Status O

Cl 181 SC 181.9.5 P490 L26 # 294
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(4)=0.1 is too restricted and exceed limited data in the ghiasi_3dj_01_2411
 SuggestedRemedy
 Recommend to increase C(4) positive limit to -0.15 from 0.1 and C(4) negative from -0.1 to -0.15 given the data in ghiasi_3dj_01_2411 with some taps exceeding 0.1
 Proposed Response Response Status O

Cl 181 SC 181.9.5.1 P437 L10 # 232
 Johnson, John Broadcom
 Comment Type T Comment Status X
 Lane lables {L0, L1, L2, L3} in Table 181-14 should be {0, 1, 2, 3}
 SuggestedRemedy
 Change lane labels {L0, L1, L2, L3} in Table181-14 to {0, 1, 2, 3}, in order to match lane assignments in Table 181-3.
 Proposed Response Response Status O

Cl 181 SC 181.9.13 P439 L8 # 301
 Ghiasi, Ali Ghiasi Quantum
 Comment Type E Comment Status X
 121.8.10 is the Wrong reference
 SuggestedRemedy
 It should be 121.8.9
 Proposed Response Response Status O

Cl 182 SC 182.2 P446 L39 # 429
 Mi, Guangcan Huawei Technologies Co., Ltd
 Comment Type TR Comment Status X
 "A PMD is expected to meet the block error ratio specifications in 174A.6, measured at a PMA, withBERadded equal to 6.4×10^{-5} . the statement of measured at a PMA may not be sufficient, for the following reason. The optical PMD interfaces with PMA at both side of the link, shown in Figure 180-2. Checking across the clauses, Figure 176C-2 and Figure 176D-2 showed both AUI C2C and AUI C2M interface with PMA. therefore, a user could use the PMA before an C2C/C2M channel as transmitter and the PMA after an C2C/C2M channel as receiver, and still be measuring the block error ratio of an optical PMD at PMA. However in this case, employing BERadded would mean double counting the error allocation to C2C/C2M. It is therefore suggested to either specify by wording or provide an illustrative drawing.. "
 SuggestedRemedy
 Add description where appropriate, such as "the test pattern should be generated by the PMA sub-layer immediately before the PMD interface at the transmitting side, while the error ratio measured by the PMA sublayer immediately after the PMD interface at the receiving side." A figure may also be helpful, will provide in a contribution.
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 182 SC 182.2 P446 L42 # 430

Mi, Guangcan Huawei Technologies Co., Ltd

Comment Type TR Comment Status X

BERadded at PMA being 6.4e-5, which corresponds to Table 174A-1, adding two C2C and two C2M allocation. BER added at PCS being 3.2e-5, which doesn't seem write. Need to recheck.

SuggestedRemedy

If the test pattern is generated by and transmitted from the PCS layer at the transmitting side, then there should be no BER_added needed. If the test pattern is generated by and transmitted from the PMA layer at the transmitting side, where the PMA is the PMA immediatedly before the PMD interface, then BER_added of 3.2e-5, equivalent to a two-part AUI link at the receiver side only, seems correct. Some clarification will be good.

Proposed Response Response Status O

Cl 182 SC 182.2 P446 L46 # 258

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Direct block error measurement requirie Golden HW receiver that may not exist and even then may introduce its own set of block erros.

SuggestedRemedy

Instead the recommendation is to measure block TDECQ where block TDECQ is by capturing 10x the SSPRQ waveform and only using worst 10% of block data for "Block TDECQ" limit. When all the blocks data are used the reporting value would be "Average TDECQ". Initial conversation with Oscope supplier is that this measurement is feasible and we won't need to change any limit or introduce any new test limit. The current average TDECQ will be changed to "Block TDECQ". See Ghiasi_3dJ_02_2411

Proposed Response Response Status O

Cl 182 SC 182.5.1 P449 L1 # 252

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

The Signal_OK and ILT fuction are hanging in the air and not clear how they propgate from TX to RX

SuggestedRemedy

Just like global_PMD_signal_detect that touches all 4 PMD Receive function the ILT block should also touch/connect to all 4 PMA transmit function and PMA Receive function

Proposed Response Response Status O

Cl 182 SC 182.5.1 P476 L2 # 254

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Inner FEC TX/RX function is a PMA

SuggestedRemedy

Suggest to replace with PMA Transmit or Receive Function (Inner FEC), if there is no room then just put in the text

Proposed Response Response Status O

Cl 182 SC 182.7.1 P430 L43 # 146

Dudek, Mike Marvell

Comment Type TR Comment Status X

The value of TDECQ is TBD. Other specifications are related to this. Having a value that can be confirmed later moves the project forward. A presentation in support of this will be provided.

SuggestedRemedy

ChangeTDECQ(max) TBD to 3.4dB to match DR spec. Also Change TECQ(max) to 3.4dB, TDECQ-TECQ to 2.5dB, Stessed eye closure in table 182-8 to 3.4dB and stressed receiver sensitivity to -1.5dBm, (or -2.2dBm if another comment that reduces the OMAouter is accepted) . In table 182-9 change the allocation for penalties to 3.8dB and the Power budget (for max TDECQ) to 7.8dB. Note that the proposed value of 3.4dB is matching the value where the curves stop in figures 182-3 and 182-4. If a different value is chosen these figures would need to be modified. Add an editor's note below table 182-7 "Editor's note (to be removed by D2.0): The maximum value of TDECQ is 3.4 dB. This maximum value and related specifications may need adjustment if receivers have trouble with this value of TECQ calculated with the higher value of SER used in this clause. Further study of this area is encouraged.

Proposed Response Response Status O

Cl 182 SC 182.7.1 P452 L43 # 103

Welch, Brian Cisco

Comment Type TR Comment Status X

Current TDECQ (max) value is "TBD"

SuggestedRemedy

Update TDECQ (max) and Target PAM4 symbol error ratio to 3.4 dB and 4.8 x 10^-4 (both must be changed), respectively per welch_3dj_01_1124

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 182 SC 182.7.1 P452 L43 # 397
 Rodes, Roberto Coherent
 Comment Type T Comment Status X
 TDECQmax for DRx-2 is currently 'TBD'
 SuggestedRemedy
 Propose to replace TBD with 3.4 dB. Supporting presentation will be provided
 Proposed Response Response Status O

CI 182 SC 182.7.1 P452 L47 # 105
 Welch, Brian Cisco
 Comment Type TR Comment Status X
 Current |TDECQ - TECQ| (max) value is "TBD"
 SuggestedRemedy
 Update |TDECQ-TECQ| (max) and Target PAM4 symbol error ratio to 2.5 dB and 4.8×10^{-4} (both must be changed), respectively per welch_3dj_01_1125
 Proposed Response Response Status O

CI 182 SC 182.7.1 P452 L45 # 306
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ, TECQ, and TDECQ-TECQ are TBD
 johnson_3df_01a_221011 presentation which include both dispersion penalty for FR4 and LR4 was used to set the LR4 TDECQ limit to 3.9 dB, the difference between the LR4 and DR-2 links is a dispersion about 1/5 of LR4
 SuggestedRemedy
 see ghiasi_3dj_03_2411 for additional details with following limits for
 TDECQ= 3.4 dB
 TECQ= 3.0 dB
 |TDECQ-TECQ|(max)=2.5 dB
 Proposed Response Response Status O

CI 182 SC 182.7.1 P452 L50 # 233
 Johnson, John Broadcom
 Comment Type T Comment Status X
 Transmitter power excursion (max) is 2 dB in Table 182-7 for all DRn-2 PMDs. This value results in overshoot at OMA(max) being restricted to only 10.3%, which is less than existing 100G PHYs.
 SuggestedRemedy
 In existing 100G PHYs from P803.2cu, TPE(max) was chosen to give approximately 8% reduction in overshoot at OMA(max), i.e. maximum allowable OS is reduced from 22% at low OMA to ~ 14% at OMA(max).
 Change 2 dB to 2.3 dB in Table 182-7. This results in OS at OMA(max) = 14.6%, consistent with 100G PHYs.
 A supporting presentation will be submitted for the Nov plenary.
 Proposed Response Response Status O

CI 182 SC 182.7.1 P452 L45 # 104
 Welch, Brian Cisco
 Comment Type TR Comment Status X
 Current TECQ (max) value is "TBD"
 SuggestedRemedy
 Update TECQ (max) and Target PAM4 symbol error ratio to 3.4 dB and 4.8×10^{-4} (both must be changed), respectively per welch_3dj_01_1125
 Proposed Response Response Status O

CI 182 SC 182.7.2 P454 L27 # 106
 Welch, Brian Cisco
 Comment Type TR Comment Status X
 Current SECQ value is "TBD"
 SuggestedRemedy
 Update SECQ and Target PAM4 symbol error ratio to 3.4 dB and 4.8×10^{-4} (both must be changed), respectively per welch_3dj_01_1125
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 182 SC 182.7.2 P454 L29 # 234

Johnson, John Broadcom

Comment Type T Comment Status X

The value of Stressed receiver sensitivity (max) is nominally given by the minimum TX OMA at TDECQ(max), minus the maximum channel insertion loss and MPI+DGD penalties. Because the fibers in a DRn-2 PHY (n>1) without breakout share the same parallel fiber cabling and connectors, the Aggressor lanes for SRS testing should be considered to have the same insertion loss as the lane under test.

SuggestedRemedy

For DRn-2 PHYs in Table 182-8, change the value of OMAouter of each aggressor lane from TBD to -0.2 dBm, which is equal to 4.2 dBm TX OMA(max), minus 4 dB max insertion loss, minus 0.4dB MPI+DGD penalty.

To cover the case of breakout, add text to footnote (e), "If the device is being used to breakout lower line rate PMDs as described in Annex 180A, OMAouter of each aggressor lane should be equal to the value of Outer Optical Modulation Amplitude (OMAouter), each lane (max) given in Table 182-7."

A supporting presentation will be submitted for the Nov plenary.

Proposed Response Response Status O

Cl 182 SC 182.7.2 P454 L35 # 235

Johnson, John Broadcom

Comment Type T Comment Status X

The requirement of no aggressors for 200G-DR1-2 only applies to single lane devices. If a DR1-2 PMD shares a multi-lane device with other DRn-2 PMDs, then the aggressor lanes must be used.

SuggestedRemedy

Change Table 182-8 footnote (e) to read: "No aggressors needed for 200GBASE-DR1-2 in a single lane device." as in footnote (e) of Table 180-8.

Proposed Response Response Status O

Cl 182 SC 182.7.3 P455 L37 # 307

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Power budget and allocation for penalties are TBDs

SuggestedRemedy

see ghiasi_3dj_03_2411 for additional details by leveraging Table 180-9 but increasing the loss by 0.75 dB to support 2000 m instead of 500 m the illustrative link budget becomes: Power budget for max TDECQ= 7.8 dB Allocation for penalties=3.8 dB

Proposed Response Response Status O

Cl 182 SC 182.8.3.1.1 P459 L25 # 223

Johnson, John Broadcom

Comment Type E Comment Status X

MDI nomenclature is inconsistent with Annex 180A here, as well as in 182.8.3.1.2 and 182.8.3.1.3.

SuggestedRemedy

Change "MDI pin" to "MDI position" in the text and tables to be consistent with nomenclature used in Annex 180A.

Proposed Response Response Status O

Cl 182 SC 182.9.1 P463 L9 # 172

Huber, Thomas Nokia

Comment Type T Comment Status X

In Table 182-16, the cross-references for the PRBS31Q and PRBS13Q patterns are incorrect; PRBS13Q is defined in 120.5.11.2.1, PRBS31Q in 120.5.11.2.2

SuggestedRemedy

Correct the references.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 182 SC 182.9.1 P463 L9 # 139

Brown, Matt Alphawave Semi

Comment Type T Comment Status X

Table 182-16. Test pattern 3, currently PRBS31Q is defined for use for receiver sensitivity. Since the PMD types defined in Clause 182 use Inner FEC, the PRBS31Q should be encoded with Inner FEC, similar to Pattern 5.

SuggestedRemedy

In Table 182-16, change test pattern 4 from "PRBS31Q" to "PRBS31Q encoded by the 200GBASE-R, 400GBASE-R, 800GBASE-R, or 1.6TBASE-R Inner FEC" and update the defining references.
Make the same change in Table 183-12.

Proposed Response Response Status O

Cl 182 SC 182.9.1 P463 L9 # 121

Brown, Matt Alphawave Semi

Comment Type T Comment Status X

Table 182-16. The Inner FEC is specifically called 200GBASE-R Inner FEC, 400GBASE-R Inner, etc. Reference it by name.

SuggestedRemedy

Change "Scrambled idle test pattern encoded by the Inner FEC used by 200GBASE-R, 400GBASE-R, 800GBASE-R, or 1.6TBASE-R"
To "Scrambled idle test pattern encoded by the 200GBASE-R, 400GBASE-R, 800GBASE-R, or 1.6TBASE-R Inner FEC"

Proposed Response Response Status O

Cl 182 SC 182.9.1 P463 L32 # 199

Brown, Matt Alphawave Semi

Comment Type T Comment Status X

In Table 182-17... The last pattern listed is "valid 200GBASE-R, 400GBASE-R, 800GBASE-R or 1.6TBASE-R signal". But this is not correct. It should be encoded by the Inner FEC, similar to test pattern 5. Given we repeated refer to this valid BASE-R signal, why not just define it as a test pattern.

SuggestedRemedy

In Table 182-16 add a new test pattern as follows:

Pattern: 7

Pattern description: "Valid 200GBASE-R, 400GBASE-R, 800GBASE-R, or 1.6TBASE-R signal encoded by the 200GBASE-R, 400GBASE-R, 800GBASE-R, or 1.6TBASE-R Inner FEC.

In Table 182-17 replace "valid 200GBASE-R, 400GBASE-R, 800GBASE-R or 1.6TBASE-R signal" with "7".

Similarly update Table 183-12 and Table 183-13.

Proposed Response Response Status O

Cl 182 SC 182.9.5 P436 L33 # 266

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Maximum equalizer pre-cursors equal 3 also implies that we could have 0, 1, or 2 pre-cursors

SuggestedRemedy

Given the intention that equalizer doesn't float replace "Maximum equalizer pre-cursors" with "Number of equalizer pre-cursors tap" and put 3 also in the min or create table with min-value-max. Make post taps i explicit 3 to 11. Feedforward equalizer length should be listed under Value col as 15, this is not a max as there is no Min!

Proposed Response Response Status O

Cl 182 SC 182.9.5 P465 L9 # 107

Welch, Brian Cisco

Comment Type TR Comment Status X

Current Target PAM4 symbol error ratio is 9.6×10^{-3}

SuggestedRemedy

Update Target PAM4 symbol error ratio to 4.8×10^{-4} per welch_3dj_01_1124

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 182 SC 182.9.5 P465 L22 # 263

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

With concern raised regarding block errors and if TDECQ captures jitter, need additional condition in the TDECQ setup to make sure TDECQ is representative of worst case operation

SuggestedRemedy

If the PMD under test has an optional AUI (C2M) the TDECQ is measured with the module in mission mode with the clock driving SSPRQ recovered from the AUI input. The AUI is operating with PRBS31Q pattern and worst case interference tolerance applied, see https://www.ieee802.org/3/dj/public/24_09/ghiasi_3dj_01a_2409.pdf

Proposed Response Response Status O

CI 182 SC 182.9.5 P465 L35 # 282

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

TDECQ taps positive limit C(-1)=0.05 is too restricted

SuggestedRemedy

Recommend to increase C(-1) positive limit to +0.1 from 0.05, see ghiasi_3dj_01_2411

Proposed Response Response Status O

CI 182 SC 182.9.5 P465 L36 # 283

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

TDECQ taps positive limit C(-2)=0.2 is too restricted given that we have C(-1)=0.5, to correct for C(-1)=-0.5 C(-2) can be as large as 0.25

SuggestedRemedy

Recommend to increase C(-2) positive limit to +0.25 from 0.2, see ghiasi_3dj_01_2411

Proposed Response Response Status O

CI 182 SC 182.9.5 P465 L37 # 284

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

TDECQ taps positive limit C(1)=0.05 is too restricted in cases of fast transmitter ability to use positive tap can be very beneficial

SuggestedRemedy

Recommend to increase C(1) positive limit to +0.2 from 0.05 helpful on fast transmitters to reduce the BW and noise see ghiasi_3dj_01_2411

Proposed Response Response Status O

CI 182 SC 182.9.5 P465 L39 # 288

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

TDECQ taps negative limit C(5)=-0.1 is too restricted and exceed limited data in the ghiasi_3dj_01_2411

SuggestedRemedy

Recommend to increase 5(4) positive limit to -0.15 from 0.1 and C(5) negative from -0.1 to -0.15 given the data in ghiasi_3dj_01_2411 with some taps exceeding -0.1

Proposed Response Response Status O

CI 182 SC 182.9.5 P465 L39 # 285

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

TDECQ taps positive limit C(2)=-0.1 and C(2)=0.2 is too restricted and exceed limited data in the ghiasi_3dj_01_2411

SuggestedRemedy

Recommend to increase C(2) positive limit to +0.3 from 0.2 given that C(-1)=-0.6 the follow on tap can be as much as prior tap weight. C(2) negative limit ghiasi_3dj_01_2411 data show can be as large as 0.129, recommending to increase C(2) negative limit from -0.1 to -0.2.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 182 SC 182.9.5 P465 L39 # 287

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

TDECQ taps positive limit C(4)=0.1 is too restricted and exceed limited data in the ghiasi_3dj_01_2411

SuggestedRemedy

Recommend to increase C(4) positive limit to -0.15 from 0.1 and C(4) negative from -0.1 to -0.15 given the data in ghiasi_3dj_01_2411 with some taps exceeding 0.1

Proposed Response Response Status O

Cl 182 SC 182.9.5 P465 L39 # 286

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

TDECQ taps negative limit C(3)=-0.1 is too restricted and exceed limited data in the ghiasi_3dj_01_2411

SuggestedRemedy

Recommend to increase C(3) positive limit to -0.15 from 0.1 and C(3) negative from -0.1 to -0.15 given the data in ghiasi_3dj_01_2411 data show can be as large as 0.129

Proposed Response Response Status O

Cl 182 SC 182.9.13 P468 L4 # 302

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

121.8.10 is the Wrong reference

SuggestedRemedy

It should be 121.8.9

Proposed Response Response Status O

Cl 182 SC 182.9.13 P468 L8 # 402

Dawe, Piers Nvidia

Comment Type TR Comment Status X

At present, the LF jitter slope for 113.4375 GBd (with inner FEC) and the LF jitter slope for 106.25 GBd (PMDs and PMAs without or before inner FEC) are both based on 4 MHz, 0.05 UI pk-pk but the UI differ, so they are incompatible. This causes a buffering requirement that is finite at 4 MHz but unbounded at low jitter frequencies (which themselves are unbounded), because the timing with inner FEC is inherited from the timing without inner FEC. One of the slopes must be adjusted to match the other in absolute time units (not UI) at low frequencies so that there is not an unbounded buffering requirement and modules can meet the spec when plugged into any compliant host. The proposed remedy is very simple.

A similar issue was discussed in multiple presentations:

- dawe_3cd_02a_0118 Options to fix the low frequency jitter (gearbox) issue
 - Dawe, Ran, Dietrich and
 - ghiasi_3dj_02a_2303 CRU Bandwidth Recommendation for 200G Interfaces
 - ghiasi_3cd_01_0118 Considerations for CRU BW and Amount of Untracked Jitter
 - ran_011718_3cd_adhoc Jitter considerations for 100GAUI-2 with 100GBASE-DR
 - dawe_3cd_03_0717 Making the jitter specs ... compatible Dawe
 - and Wertheim
 - dawe_3bs_02_0717 Making the jitter specs ... compatible Dawe
 - and Wertheim
- but this situation is much easier to fix.

SuggestedRemedy

For the FECi PMDs (182.9.13 and 183.9.13), instead of referring to 121.8.10.4 (Table 121-12, Applied sinusoidal jitter, which is based on $2e5/f$, 0.05 UI which is $J^*f \leq 1.882$ us, $J \leq 0.471$ ps as there is no inner FEC there), use $2.13e5/f$, 0.053 UI, which is also $J^*f \leq 1.882$ us and $J \leq 0.471$ ps. The jitter corner remains at 4 MHz.

Proposed Response Response Status O

Cl 183 SC 183.2 P474 L38 # 431

Mi, Guangcan Huawei Technologies Co., Ltd

Comment Type TR Comment Status X

"A PMD is expected to meet the block error ratio specifications in 174A.6, measured at a PMA, withBERadded equal to 6.4×10^{-5} . the statement of measured at a PMA may not be sufficient, for the following reason. The optical PMD interfaces with PMA at both side of the link, shown in Figure 180-2. Checking across the clauses, Figure 176C-2 and Figure 176D-2 showed both AUI C2C and AUI C2M interface with PMA. therefore, a user could use the PMA before an C2C/C2M channel as transmitter and the PMA after an C2C/C2M channel as receiver, and still be measuring the block error ratio of an optical PMD at PMA. However in this case, employing BERadded would mean double counting the error allocation to C2C/C2M. It is therefore suggested to either specify by wording or provide an illustrative drawing.. "

SuggestedRemedy

Add description where appropriate, such as "the test pattern should be generated by the PMA sub-layer immediately before the PMD interface at the transmitting side, while the error ratio measured by the PMA sublayer immediately after the PMD interface at the receiving side." A figure may also be helpful, will provide in a contribution.

Proposed Response Response Status O

Cl 183 SC 183.2 P474 L41 # 432

Mi, Guangcan Huawei Technologies Co., Ltd

Comment Type TR Comment Status X

BERadded at PMA being $6.4e-5$, which corresponds to Table 174A-1, adding two C2C and two C2M allocation. BER added at PCS being $3.2e-5$, which doesn't seem write. Need to recheck.

SuggestedRemedy

If the test pattern is generated by and transmitted from the PCS layer at the transmitting side, then there should be no BER_added needed. If the test pattern is generated by and transmitted from the PMA layer at the transmitting side, where the PMA is the PMA immediately before the PMD interface, then BER_added of $3.2e-5$, equivalent to a two-part AUI link at the receiver side only, seems correct. Some clarification will be good.

Proposed Response Response Status O

Cl 183 SC 183.2 P474 L45 # 257

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Direct block error measurement require Golden HW receiver that may not exist and even then may introduce its own set of block erros.

SuggestedRemedy

Instead the recommendation is to measure block TDECQ where block TDECQ is by capturing 10x the SSPRQ waveform and only using worst 10% of block data for "Block TDECQ" limit. When all the blocks data are used the reporting value would be "Average TDECQ". Initial conversation with Oscope supplier is that this measurement is feasible and we won't need to change any limit or introduce any new test limit. The current average TDECQ will be changed to "Block TDECQ". See Ghiasi_3dJ_02_2411

Proposed Response Response Status O

Cl 183 SC 183.5.1 P449 L18 # 255

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

Inner FEC TX/RX function is a PMA

SuggestedRemedy

Suggest to replace with PMA Transmit or Receive Function (Inner FEC), if there is no room then just put in the text

Proposed Response Response Status O

Cl 183 SC 183.5.1 P476 L18 # 253

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

The Signal_OK and ILT function are hanging in the air and not clear how they propagate from TX to RX

SuggestedRemedy

Just like global_PMD_signal_detect that touches all 4 PMD Receive function the ILT block should also touch/connect to all 4 PMA transmit function and PMA Receive function

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 183 SC 183.6 P479 L30 # 129

Brown, Matt Alphawave Semi

Comment Type T Comment Status X

The note at the end of 183.6 should have been deleted.
 "NOTE—There is no requirement to associate a particular electrical lane with a particular optical lane, as the PCS is capable of receiving lanes in any arrangement."
 The explicit assignment of signal lanes to optical lanes is required in order to support ILT, similar to mapping to connector positions and fibers in 180.6 and 182.6. This evident when viewing Figure 183-2 which depicts lane assignments along with the mapping of lanes to wavelengths in 183.6.

SuggestedRemedy

Change the note to read:
 "NOTE--Each functional lane, denoted SLi at the transmitter and DLi at the receiver, is mapped to a specific wavelength to support ILT operation."
 Change the note in 181.6 as well.

Proposed Response Response Status O

CI 183 SC 183.7.1 P480 L34 # 147

Dudek, Mike Marvell

Comment Type TR Comment Status X

The value of TDECQ for FR4 is TBD. Other specifications are related to this. Having a value that can be confirmed later moves the project forward. A presentation in support of this comment will be provided.

SuggestedRemedy

In Table 183-6 ChangeTDECQ(max) TBD to 3.4dB. Also Change TECQ(max) to 3.4dB, and the inequality in the conditions on page480 line 29 from TBD to 3.4dB. TDECQ-TECQ to 2.5dB, Stessed eye closure in table 183-7 to 3.4dB and stressed receiver sensitivity to -1.2dBm. In table 183-8 change the allocation for penalties to 3.9dB and the Power budget (for max TDECQ) to 7.9dB. Delete the editor's notes on page 481 line 35 and page 483 line 26. Add an editor's note below table 183-6 "Editor's note (to be removed by D2.0): The maximum value of TDECQ is 3.4 dB. This maximum value and related specifications may need adjustment if receivers have trouble with this value of TECQ calculated with the higher value of SER used in this clause. Further study of this area is encouraged.

Proposed Response Response Status O

CI 183 SC 183.7.1 P480 L34 # 396

Rodes, Roberto Coherent

Comment Type T Comment Status X

TDECQmax for FR4 is currently 'TBD'

SuggestedRemedy

Propose to replace TBD with 3.4 dB. Supporting presentation will be provided

Proposed Response Response Status O

CI 183 SC 183.7.1 P480 L34 # 108

Welch, Brian Cisco

Comment Type TR Comment Status X

Current TDECQ (max) value is "TBD"

SuggestedRemedy

Update TDECQ (max) and Target PAM4 symbol error ratio to 3.4 dB and 4.8×10^{-4} (both must be changed), respectively per welch_3dj_01_1124

Proposed Response Response Status O

CI 183 SC 183.7.1 P480 L35 # 295

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

TDECQ taps negative limit C(5)=-0.1 is too restricted and exceed limited data in the ghiasi_3dj_01_2411

SuggestedRemedy

Recomend to increase 5(4) positive limit to -0.15 from 0.1 and C(5) negative from -0.1 to -0.15 given the data in ghiasi_3dj_01_2411 with some taps exceeding -0.1

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 183 SC 183.7.1 P480 L35 # 298

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

johnson_3df_01a_221011 presentation which include both dispersion penalty for FR4 and LR4 was used to set the LR4 TDECQ limit to 3.9 dB, and given slightly lower dispersion penalty for FR4 the same presentation show dispersion penalty of 3.4 dB

SuggestedRemedy

see ghiasi_3dj_03_2411 for additional details with following limits for
TDECQ= 3.4 dB
TECQ= 3.0 dB
|TDECQ-TECQ|(max)=2.5 dB

Proposed Response Response Status O

Cl 183 SC 183.7.1 P480 L37 # 109

Welch, Brian Cisco

Comment Type TR Comment Status X

Current TECQ (max) value is "TBD"

SuggestedRemedy

Update TECQ (max) and Target PAM4 symbol error ratio to 3.4 dB and 4.8×10^{-4} (both must be changed), respectively per welch_3dj_01_1125

Proposed Response Response Status O

Cl 183 SC 183.7.1 P480 L38 # 110

Welch, Brian Cisco

Comment Type TR Comment Status X

Current |TDECQ - TECQ| (max) value is "TBD"

SuggestedRemedy

Update |TDECQ-TECQ| (max) and Target PAM4 symbol error ratio to 2.5 dB and 4.8×10^{-4} (both must be changed), respectively per welch_3dj_01_1125

Proposed Response Response Status O

Cl 183 SC 183.7.1 P480 L41 # 236

Johnson, John Broadcom

Comment Type T Comment Status X

Transmitter power excursion (max) is 3.1 dB in Table 183-7 for 800GBASE-LR4. This value results in overshoot at OMA(max) being restricted to only 5%, which is less than existing 100G PHYs.

SuggestedRemedy

In existing 100G PHYs from P803.2cu, TPE(max) was chosen to give approximately 8% reduction in overshoot at OMA(max), i.e. maximum allowable OS is reduced from 22% at low OMA to ~ 14% at OMA(max).
Change 3.1 dB to 3.8 dB in Table 183-7. This results in OS at OMA(max) = 14.6%, consistent with 100G PHYs.
A supporting presentation will be submitted for the Nov plenary.

Proposed Response Response Status O

Cl 183 SC 183.7.2 P482 L30 # 111

Welch, Brian Cisco

Comment Type TR Comment Status X

Current SECQ value is "TBD"

SuggestedRemedy

Update SECQ and Target PAM4 symbol error ratio to 3.4 dB and 4.8×10^{-4} (both must be changed), respectively per welch_3dj_01_1125

Proposed Response Response Status O

Cl 183 SC 183.7.2 P482 L31 # 304

Ghiasi, Ali Ghiasi Quantum

Comment Type T Comment Status X

johnson_3df_01a_221011 presentation can also be used to address TBDs for the stressed sensitivity

SuggestedRemedy

see also ghiasi_3dj_03_2411 for additional details with following limits for
Stressed receiver sensitivity (OMAouter) (max)=-3.7 dB + 2.5 dB=-1.2 dBm
Stressed eye closure for PAM4(SECQ), each lane is the max TDECQ=3.4 dB

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 183 SC 183.7.3 P483 L39 # 297
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 FR4 power budget is TBD
 SuggestedRemedy
 channel lossfor FR4 is =4.0 dB with addition of allocation penalties of 4.3 dB result in power budget of 8.3 dB
 Proposed Response Response Status O

Cl 183 SC 183.8 P485 L38 # 305
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 DGD_max is TBD
 SuggestedRemedy
 Per kuschnerov_3df_01_2211. contribution DGD_max=PMD_max*SQRT(L in km), per value on page DGD max is 2.28 with rouding will be 2.3 which is the same as 400GBASE-FR4
 Proposed Response Response Status O

Cl 183 SC 183.7.3 P483 L52 # 148
 Dudek, Mike Marvell
 Comment Type T Comment Status X
 Footnote f to Table 183-8 is incorrect. When calculating the link budget from the adopted power levels the allocation for MPI and DGD penalties is 0.5dB the same as in clause 181
 SuggestedRemedy
 Change the value of the allocation for MPI and DGD penalties in footnote f from 0.4dB to 0.5dB.
 Proposed Response Response Status O

Cl 183 SC 183.9.1 P488 L9 # 173
 Huber, Thomas Nokia
 Comment Type T Comment Status X
 In Table 183-12, the cross-references for the PRBS31Q, PRBS13Q, and SSPRQ patterns are incorrect; PRBS13Q is defined in 120.5.11.2.1, PRBS31Q in 120.5.11.2.2, SSPRQ in 120.5.11.2.4
 SuggestedRemedy
 Correct the references.
 Proposed Response Response Status O

Cl 183 SC 183.8 P463 L17 # 299
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 Optical return losses are TBD for FR4 and LR4
 SuggestedRemedy
 Given the same cable plant as FR4-500 propose to use 17.1 dB for FR4 and 15.6 dB for LR4 optical return losses
 Proposed Response Response Status O

Cl 183 SC 183.9.5 P489 L48 # 112
 Welch, Brian Cisco
 Comment Type TR Comment Status X
 Current Target PAM4 symbol error ratio is 9.6×10^{-3}
 SuggestedRemedy
 Update Target PAM4 symbol error ratio to 4.8×10^{-4} per welch_3dj_01_1124
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 183 SC 183.9.5 P490 L3 # 264
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 With concern rasied regarding block errors and if TDECQ captures jitter, need additional condition in the TDECQ setup to make sure TDECQ is representative of worst case operation
 SuggestedRemedy
 If the PMD under test has an optional AUI (C2M) the TDECQ is measured with the module in mission mode with the clock driving SSPRQ recovered from the AUI input. The AUI is operating with PRBS31Q pattern and worst case interference tolerance applied, see https://www.ieee802.org/3/dj/public/24_09/ghiasi_3dj_01a_2409.pdf
 Proposed Response Response Status O

Cl 183 SC 183.9.5 P490 L23 # 267
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 Maximum equalizer pre-cursors equal 3 also implies that we could have 0, 1, or 2 pre-cursors
 SuggestedRemedy
 Given the intention that equalizer doesn't float repalce "Maximum equalizer pre-cursors" with "Number of equalizer pre-cursors tap" and put 3 also in the min or create table with min-value-max. Make post taps i explicit 3 to 11. Feedforward equalizer length should be listed under Value col as 15, this is not a max as there is no Min!
 Proposed Response Response Status O

Cl 183 SC 183.9.5 P490 L35 # 289
 Ghiasi, Ali Ghiasi Quantum
 Comment Type T Comment Status X
 TDECQ taps positive limit C(-1)=0.05 is too restricted
 SuggestedRemedy
 Recomend to increase C(-1) positive limit to +0.1 from 0.05, see ghiasi_3dj_01_2411
 Proposed Response Response Status O

Cl 183 SC 183.9.5.1 P491 L4 # 237
 Johnson, John Broadcom
 Comment Type T Comment Status X
 Lane lables {L0, L1, L2, L3} in Table 183-15 should be {0, 1, 2, 3}
 SuggestedRemedy
 Change lane labels {L0, L1, L2, L3} in Table183-15 to {0, 1, 2, 3}, in order to match lane assignments in Table 183-3 and 183-4.
 Proposed Response Response Status O

Cl 183 SC 183.9.5.1 P491 L4 # 224
 Johnson, John Broadcom
 Comment Type E Comment Status X
 If no informative Annex is planned in D1.3, remove the reference in footnote (a)
 SuggestedRemedy
 Make footnote (a) consistent with other PMD clauses. Remove the phrase, "and the optical channel characteristics methodology described in Annex TBD".
 Proposed Response Response Status O

Cl 183 SC 183.9.5.1 P491 L11 # 126
 Brown, Matt Alphawave Semi
 Comment Type T Comment Status X
 In Table 183-5... In the column labelled "Insertion loss" the "value" provided for both PMD types is "Minimum". It is not evident what this means. Perhaps it means the minimum insertion loss specified in Table 183-9 "Optical channel characteristics". If that is that case then either use this value (0 dB) or reference this table (e.g., with a footnote). If it means something else then provide a bit more context, perhaps in a footnote.
 SuggestedRemedy
 Clarify "Minimum" in Table 183-15 per comment.
 Proposed Response Response Status O

Cl 183 SC 183.9.5.1 P491 L21 # 123

Brown, Matt Alphawave Semi

Comment Type T Comment Status X

In Table 183-5 footnote a the is reference to an annex describing statistical link design methodology. However, this annex does not exist. Also, it seems that all of the necessary background is provided in the reference to G.652 Appendix I.

SuggestedRemedy

Delete ", and the optical channel characteristics methodology described in Annex TBD"

Proposed Response Response Status O

Cl 183 SC 183.9.5.1 P491 L21 # 125

Brown, Matt Alphawave Semi

Comment Type T Comment Status X

Table 183-15 footnote b states "There is no intent to stress the sensitivity of the O/E converter associated with the oscilloscope." 183.9.5.1 specifies characteristics of a test channel to be used for transmitter compliance testing. It seems rather obvious that this isn't about stress testing the scope O/E converter. Is there something subtle that's missing in this statement?

SuggestedRemedy

Either (a) delete footnote c or (b) provide missing context.

Proposed Response Response Status O

Cl 183 SC 183.9.5.1 P491 L23 # 124

Brown, Matt Alphawave Semi

Comment Type T Comment Status X

In Table 183-5 footnote c it says "The optical return loss is applied at TP2." And in a later paragraphs it says "The channel provides an optical return loss specified in Table 183-15." Return loss is a ratio of transmitted signal to the reflected signal. The intent I believe is that the channel provides back-reflection with a target return loss given in Table 183-15. Subclause 139.7.5.1 uses the following text "The optical splitter and variable reflector are adjusted so that each transmitter is tested with the optical return loss specified in Table 139-11."

SuggestedRemedy

Change footnote b to "The back-reflection is applied at TP2."

Change "The channel provides an optical return loss specified in Table 183-15." to "The channel provides back reflection with return loss specified in Table 183-15."

Proposed Response Response Status O

Cl 183 SC 183.9.13 P493 L11 # 303

Ghiasi, Ali Ghiasi Quantum

Comment Type E Comment Status X

121.8.10 is the Wrong reference

SuggestedRemedy

It should be 121.8.9

Proposed Response Response Status O

CI 184 SC 184.2 P498 L43 # 420

Kota, Kishore Marvell Semiconductor

Comment Type E Comment Status X

ADC input signals in Figure 184-2 are labelled RX_Ai, RX_Aq, RX_Bi and RX_Bq. I think the labels A/B are used to highlight the fact that the polarization angle at the receiver is not necessarily aligned with the X/Y polarizations at the transmitter. However, A/B are somewhat arbitrary and do not clearly reflect the fact that those are orthogonal polarizations.

SuggestedRemedy

My suggestion is to use H/V (for horizontal and vertical) instead of A/B because it is common to use these letters in coherent DSPs instead of X/Y to indicate orthogonal polarizations. i.e. use RX_Hi, RX_Hq, RX_Vi, RX_Vq. Same change would also apply to uses of these names in 184.5.1 on page 508, lines 45, 47 and 51 and in 184.5.2 on page 509, line 5 and 184.5.7 on page 510, line 10.

Proposed Response Response Status O

CI 184 SC 184.4 P500 L1 # 426

Kota, Kishore Marvell Semiconductor

Comment Type TR Comment Status X

Text in Clause 184.4 was changed from prior drafts. However, it appears some of the original intent and precision was lost in the process.

SuggestedRemedy

Supporting contribution to be provided to address all the places where precision was lost in this text in the pursuit of simplified text.

Proposed Response Response Status O

CI 184 SC 184.4.1 P500 L5 # 423

Kota, Kishore Marvell Semiconductor

Comment Type TR Comment Status X

Text in this clause was changed from earlier drafts and the original intent was lost in the process. Lane alignment lock in D1.2 refers to 172.2.5.1 for deskew. However, 172.2.5.1 specifies a complete de-skew of all the PCS lanes. However, the permutation function only requires a partial deskew of 20-bits (i.e. dual 10-bit RS symbol boundaries). A full deskew places an unreasonable burden on implementations which are targeted at low-power applications

SuggestedRemedy

Supporting contribution to be provided.

Proposed Response Response Status O

CI 184 SC 184.4.2 P500 L9 # 422

Kota, Kishore Marvell Semiconductor

Comment Type TR Comment Status X

The text of this clause was changed from earlier drafts and the original intent was lost in the process. Lane reorder in D1.2 refers to 172.2.5.2 which specifies that all the lanes are completely reordered to match the PCS lane ordering. However, 800GBASE-LR1 permutation function only requires a partial reorder where flow 0 and flow 1 are separated without any requirement on the order of the PCS lanes within each flow. Requiring a full reorder places an unreasonable burden on implementations which are targeted at low-power applications.

SuggestedRemedy

Supporting contribution to be provided.

Proposed Response Response Status O

CI 184 SC 184.4.3 P500 L17 # 174

Huber, Thomas Nokia

Comment Type T Comment Status X

pcsla[q,i] is defined both here and in the first bullet at line 21, using slightly different words.

SuggestedRemedy

Delete the sentence at line 17.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 184 SC 184.4.5 P503 L14 # 424

Kota, Kishore Marvell Semiconductor

Comment Type TR Comment Status X

Text says "Define parity[15:0] to be the coefficients of the computed parity polynomial" where it is implied but not stated that parity[15] corresponds to p15 in Equation (184-2). This should be stated precisely to eliminate any ambiguity.

SuggestedRemedy

Replace with "Define parity[15:0] to be the coefficients of the computed parity polynomial where parity[15] corresponds to p15 in Equation (184-2) and so on."

Proposed Response Response Status O

Cl 184 SC 184.4.6 P503 L29 # 425

Kota, Kishore Marvell Semiconductor

Comment Type TR Comment Status X

Text implies but does not state what the bits circo[j] should be for j=110 to 125.

SuggestedRemedy

Need to say encodeo[j] is assigned to circo[j] for j=110 to 125

Proposed Response Response Status O

Cl 184 SC 184.4.9 P505 L15 # 175

Huber, Thomas Nokia

Comment Type T Comment Status X

Table 184-2 and Table 184-4 (in 184.4.11.1) both show the entire pilot sequence. The first table shows it as bit pairs, the second as 4-level signal values as defined by the mapping in Table 184-3. It seems unnecessary to duplicate the information in both formats. The concept of the pilot sequence needs to be introduced in 184.4.9, at least up through Table 184-1 with the generator polynomial and seeds. Some of the information in 184.4.11.1 is also useful to understand, ie., that the values of the pilot sequence are chosen such that they will produce symbols that use the 'outer' points of the constellation, but otherwise the information in 184.4.11.1 seems unnecessary since 184.4.11 is about mapping bit pairs to symbols, and that mapping is itself the same for all bits in the DSP frame

SuggestedRemedy

Insert this text in 184.4.9, following table 184-1:
The bit-pairs that compose the pilot sequence are shown in table 184-2. They are selected such that they will produce symbols that use the outer 16QAM constellation points, as shown in figure 184-2.

Move figure 184-7 to be above table 184-2.

Delete clause 184.4.11.1.

Proposed Response Response Status O

Cl 184 SC 184.4.9 P506 L21 # 27

Huang, Kechao Huawei

Comment Type T Comment Status X

In Figure 184-6, the bit "0" after "Seed X:" (and "Seed Y:") is not necessary.

SuggestedRemedy

In Figure 184-6, delete "0" after "Seed X:"; delete "0" after "Seed Y:"

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 184 SC 184.5.1 P508 L44 # 201

Brown, Matt Alphawave Semi

Comment Type T Comment Status X

Now that the signal names between the PMD receive and Inner FEC receiver have been appropriately renamed, the service interface parameter names should be renamed to match.

SuggestedRemedy

Make the following substitutions throughout Clause 184, 185, 186, and 187.

- rx_signal_xi to rx_signal_ai
- rx_signal_xq to rx_signal_aq
- rx_signal_yi to rx_signal_bi
- rx_signal_yq to rx_signal_bq

Also, update any related text to match.

Proposed Response Response Status O

Cl 184 SC 184.8 P516 L31 # 365

Slavick, Jeff Broadcom

Comment Type T Comment Status X

Support of the "optional" path delay information should be presented as the first information of this section not the last.

SuggestedRemedy

Change 184.8 to be:

184.8 Path data delay (optional)

Support for the optional path data delay information is indicated by the status variables Inner_FEC_delay_ns_TX_ability, Inner_FEC_delay_subns_TX_ability, Inner_FEC_delay_ns_RX_ability, and Inner_FEC_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported, the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on dspfo[3,1894] (see 184.4.10), corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:

- Inner_FEC_delay_ns_TX_max, Inner_FEC_delay_subns_TX_max
- Inner_FEC_delay_ns_TX_min, Inner_FEC_delay_subns_TX_min
- Inner_FEC_delay_ns_RX_max, Inner_FEC_delay_subns_RX_max
- Inner_FEC_delay_ns_RX_min, Inner_FEC_delay_subns_RX_min

Proposed Response Response Status O

Cl 184 SC 184.10 P519 L1 # 325

Nicholl, Gary Cisco Systems

Comment Type TR Comment Status X

Need to update PICS to include path data delay for time synchronization (see 184.8) . See 175.9.4.7 as an example for what was done for the 1.6TBASE-R PCS in Clause 175.

SuggestedRemedy

Updated PICS to include path data delay for time synchronization. See 175.9.4.7 as an example.

Proposed Response Response Status O

Cl 185 SC 185.5 P531 L17 # 427

Kota, Kishore Marvell Semiconductor

Comment Type TR Comment Status X

TBDs in Table 185-5

SuggestedRemedy

Supporting contribution to be provided to address TBDs

Proposed Response Response Status O

Cl 185 SC 185.5.1 P528 L32 # 421

Kota, Kishore Marvell Semiconductor

Comment Type E Comment Status X

ADC input signals in Figure 185-5 are labelled RX_Ai, RX_Aq, RX_Bi and RX_Bq. I think the original X/Y were changed to A/B to highlight the fact that the polarization angle at the receiver is not necessarily aligned with the X/Y polarizations at the transmitter. However, A&B are somewhat arbitrary and do not clearly reflect the fact that those are orthogonal polarizations.

SuggestedRemedy

My suggestion is to use H/V (for horizontal and vertical) instead of A/B because it is common to use these letters in coherent DSPs instead of X/Y to indicate orthogonal polarizations. i.e. use RX_Hi, RX_Hq, RX_Vi, RX_Vq. Same change would also apply to uses of these names in 185.5.3 on page 529 line 25,

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 185 SC 185.5.5 P530 L5 # 241

Maniloff, Eric

Ciena

Comment Type T Comment Status X

A value is needed for the Signal Detection Criteria. Currently for a Minimum Tx Power, the sensitivity would be -18dBm with no impairments. Based on our Max Average Power for an Off Transmitter of -20dBm, a value of -19dBm is recommended

SuggestedRemedy

Replace TBD in Table 185-3 with -19dBm

Proposed Response Response Status O

Cl 185 SC 185.6 P532 L20 # 428

Kota, Kishore

Marvell Semiconductor

Comment Type TR Comment Status X

TBDs in Table 185-6

SuggestedRemedy

Supporting contribution to be provided to address TBDs

Proposed Response Response Status O

Cl 185 SC 185.6.1 P531 L33 # 242

Maniloff, Eric

Ciena

Comment Type T Comment Status X

The Transmitter Quality being developed is ETCC. This should be updated in Table 185-5.

SuggestedRemedy

Replace Transmitter Quality Metric in Table 185-5 with ETCC with a maximum value of 3.4dB.

Proposed Response Response Status O

Cl 185 SC 185.6.1 P531 L42 # 238

Johnson, John

Broadcom

Comment Type T Comment Status X

The units shown for Transmitter in-band OSNR (min) do not follow IEEE standard conventions

SuggestedRemedy

The intent of the unit "dB (12.5GHz)" is to indicate that the noise power density reference bandwidth is 12.5GHz. This is more properly given as a test condition in the spec Description than in the Units column, or it can be left out completely since the test method is adequately spelled out in 185.9.12.

Propose to change the spec Description to "Transmitter OSNR in 12.5 GHz band (min)" and change the unit to "dB". The spec limit is unchanged.

Proposed Response Response Status O

Cl 185 SC 185.6.1 P531 L50 # 243

Maniloff, Eric

Ciena

Comment Type T Comment Status X

Tx frequency Slew rates and clock phase noise need definition

SuggestedRemedy

A contribution with updated values will be provided

Proposed Response Response Status O

Cl 185 SC 185.6.2 P532 L34 # 239

Johnson, John

Broadcom

Comment Type T Comment Status X

ETCC inequality is pointing the wrong way

SuggestedRemedy

Change condition to read: "for 1 < ETCC <= 3.4 dB"

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 185 SC 185.6.2 P532 L40 # 245
 Maniloff, Eric Ciena
 Comment Type T Comment Status X
 A value of Rx PDL (max) is required. An additional 0.5dB above the Tx X/Y imbalance is recommended
 SuggestedRemedy
 Replace TBD for Polarization dependent loss (max) with 2.0dB
 Proposed Response Response Status O

Cl 185 SC 185.7.2.2 P535 L8 # 216
 Stassar, Peter Huawei
 Comment Type TR Comment Status X
 Currently the maximum discrete reflectance is TBD, but it is unclear that such a specification is necessary for coherent interfaces and that it is sufficient to specify only channel ORL.
 SuggestedRemedy
 Remove subclause 185.7.2.2
 Proposed Response Response Status O

Cl 185 SC 185.6.2 P532 L40 # 244
 Maniloff, Eric Ciena
 Comment Type T Comment Status X
 SOP evolution needs definition. Based on the available data, a value ≥ 20 kRad/s should be specified. Aligning with previous standards of 50kRad/s, as well as 800GBASE-ER1-20 is recommended.
 SuggestedRemedy
 Replace TBD for State of polarization (max) with 50 kRad/s
 Proposed Response Response Status O

Cl 185 SC 185.8.1 P536 L8 # 200
 Brown, Matt Alphawave Semi
 Comment Type T Comment Status X
 The table refers to "valid 800GBASE-LR1" but does not define what this is.
 SuggestedRemedy
 Change "valid 800GBASE-LR1" to "valid 800GBASE-R signal encoded by the 800GBASE-LR1 Inner FEC".
 Alternately, (see similar comment against 182.9.1) consider defining a test pattern number for this signal.
 In Table 185-10 add a new test pattern...
 Pattern: 7
 Pattern description: "Valid 800GBASE-R signal encoded by the 800GBASE-LR1 Inner FEC"
 Proposed Response Response Status O

Cl 185 SC 185.7 P534 L19 # 215
 Stassar, Peter Huawei
 Comment Type TR Comment Status X
 Note b reads "Over the wavelength range 1304.5 nm to 1317.5 nm.". This is the same wavelength range as the DR specifications in Clauses 180 and 182 and far too wide for a coherent TX/RX specified at 228.675 THz which is 1311 nm. The range is +/- 20 GHz which is very narrow, 1310.88 - 1311.11 nm.
 SuggestedRemedy
 In Table 185-8 rewrite note b stating "at 1311 nm".
 Proposed Response Response Status O

Cl 185 SC 185.9 P537 L45 # 246
 Maniloff, Eric Ciena
 Comment Type T Comment Status X
 TQM should be replaced with ETCC. More details on the implementation are needed.
 SuggestedRemedy
 A contribution with more details on the ETCC measurement methodology will be provided.
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 185 SC 185.9.1 P538 L12 # 143
 Fetz, Brian Keysight Technologies
 Comment Type T Comment Status X
 A line width of 30kHz is not available on current generation test equipment and 100kHz is an acceptable maximum value.
 SuggestedRemedy
 change line width value from 30kHz to 100kHz in table
 Proposed Response Response Status O

CI 185 SC 185.9.2 P538 L46 # 391
 Pfieffe, Joerg Keysight Technologies
 Comment Type T Comment Status X
 There is no calibration for local oscillator linewidth and hence there is no calibration residual. The local oscillator linewidth definition in previous section 185.9.1 is sufficient.
 SuggestedRemedy
 Remove this line in Table 185-13
 Proposed Response Response Status O

CI 185 SC 185.9.1 P538 L33 # 393
 Pfieffe, Joerg Keysight Technologies
 Comment Type T Comment Status X
 A coherent front-end calibration residual I-Q skew of 0.2 ps is not available on current generation test equipment and 0.5 ps is an acceptable maximum value
 SuggestedRemedy
 change I-Q skew for X value from 0.2 to 0.5 in table 185-13 and analog change I-Q skew for Y value.
 Proposed Response Response Status O

CI 185 SC 185.9.2 P538 L46 # 144
 Fetz, Brian Keysight Technologies
 Comment Type T Comment Status X
 A line width of 30kHz is not available on current generation test equipment and 100kHz is an acceptable maximum value.
 SuggestedRemedy
 change line width value from 30kHz to 100kHz in table
 Proposed Response Response Status O

CI 185 SC 185.9.1 P538 L35 # 395
 Pfieffe, Joerg Keysight Technologies
 Comment Type T Comment Status X
 There is no coherent front-end calibration for I-Q DC offset or I-Q instantaneous offset, hence there is also no post calibration residual.
 SuggestedRemedy
 Remove the four lines, I-Q DC offset for X, I-Q instantaneous offset for X, I-Q DC offset for Y and I-Q DC offset for Y from Table 185-13
 Proposed Response Response Status O

CI 185A SC 185A.2.2 P814 L51 # 225
 Johnson, John Broadcom
 Comment Type E Comment Status X
 grammar: "comprises of"
 SuggestedRemedy
 Change "comprises of" to "comprises"
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 185A SC 185A.2.2.1 P815 L15 # 226

Johnson, John Broadcom

Comment Type E Comment Status X

The text suggests that the residual spec values are given in Table 185A-2, but only the parameters are in this table. The specs are given in tables in the PMD clauses.

SuggestedRemedy

Reword this sentence along the lines of, "Post-calibration residual parameters for the calibrated coherent detector front-end are listed in Table 185A-2. The values assigned to these parameters are defined by the Physical Layer specification that invokes the method."

Proposed Response Response Status O

Cl 185A SC 185A.2.5 P820 L1 # 219

Issenhuth, Tom Huawei

Comment Type T Comment Status X

This subclause "TQM Calculation" is incomplete.

SuggestedRemedy

Update the subclause as proposed in the supporting presentation to be provided.

Proposed Response Response Status O

Cl 186 SC 186.2.2 P550 L17 # 417

Dawe, Piers Nvidia

Comment Type T Comment Status X

Some of the material here is not "overview, it is part of the transmit function or the receive function as Figure 186-3 shows.

SuggestedRemedy

Move some of the material in lines 17 to 34 to 186.2.3, and some of the material in lines 36 to 47 to 186.2.4, with editorial licence.

Proposed Response Response Status O

Cl 186 SC 186.2.2 P550 L29 # 419

Dawe, Piers Nvidia

Comment Type TR Comment Status X

This says "a spatially-coupled TPC-like code". "TPC" and "spatial" do not appear anywhere else in the draft.

SuggestedRemedy

Explain what is meant by "spatially-coupled" and "TPC" and "TPC-like code".

Proposed Response Response Status O

Cl 186 SC 186.2.3.1 P550 L1 # 76

Ran, Adee Cisco Systems, Inc.

Comment Type ER Comment Status X

"One 800GMII data transfer is encoded into one 66-bit block. Idle characters are removed from the stream of 66b blocks"
"66b" seems to refer to "66-bit block" in the previous sentence. This inconsistency is not helpful.

There are many similar instances of block sizes in this clause, such as 66B and 257B in 186.2.3.2, and 128B elsewhere. The "B" suffix is potentially confusing as it often denotes bytes. Although this format is common for the encoding/transcoding schemes, we should avoid using it for block sizes.

SuggestedRemedy

Change all instances of block sizes written as #b or #B to "#-bit" except in the transcoder labels (64B/66B to 256B/257B transcoder). Also in subclause headings.

Proposed Response Response Status O

Cl 186 SC 186.2.3.4 P552 L19 # 9

Bruckman, Leon Nvidia

Comment Type ER Comment Status X

In Figure 186-5, the frames are contiguous, but they are shown with spaces between them

SuggestedRemedy

In Figure 186-5 make the frames contiguous, without space between them

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 186 SC 186.2.3.5.1 P553 L31 # 10
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 The acronym AM is overloaded and creates confusion
 SuggestedRemedy
 Change the name of the AM field to: GMP Alignment Marker, abbreviated as GAM
 Proposed Response Response Status O

Cl 186 SC 186.2.3.9 P557 L32 # 15
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 Four times in the clause the CRC32 is written as CRC-32
 SuggestedRemedy
 Change four times CRC-32 to CRC32 in the whole clause.
 Proposed Response Response Status O

Cl 186 SC 186.2.3.6 P553 L52 # 11
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 We should also define what does the receiver do with the unused bits.
 SuggestedRemedy
 Add to the end of the first paragraph in the section: "and ignored by the receiver"
 Proposed Response Response Status O

Cl 186 SC 186.2.3.9 P557 L32 # 16
 Bruckman, Leon Nvidia
 Comment Type T Comment Status X
 The sentence: "extended by 29 CRC-32 and an additional 64 pad bits after the 29th CRC-32 (total 992 bits)," is hard to parse
 SuggestedRemedy
 Change to: "extended by 29 CRC32 values with an additional 64 pad bits after the 29th CRC32 (total 992 bits),"
 Proposed Response Response Status O

Cl 186 SC 186.2.3.6.10 P556 L26 # 12
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 Pointers like the AML are prone to wrong interpretation
 SuggestedRemedy
 Add an example of the AML value. It can either be a figure, or just text that says: "If the removed AM was located immediately before the Nth 66B block in the GMP payload, then the value of the AML will be 0xXX"
 Proposed Response Response Status O

Cl 186 SC 186.2.3.10 P558 L26 # 13
 Bruckman, Leon Nvidia
 Comment Type T Comment Status X
 ITU-T refers to a OFBGkj frame. It will be usefull to specify the relationship between the FEC frame and the ITU-T OFBGkj
 SuggestedRemedy
 Add the folowing text at the end of the section: "The FEC frame in this standard corresponds to the OFBGkj structure defined in ITU-T G.709.6"
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 186 SC 186.2.4.4 P561 L19 # 17
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 it is not clear how shall the OH fields be handled if CRC-32 errors are detected in their row
 SuggestedRemedy
 Add specification that OH fields shall be ingored if a CRC32 error was detected in their row.
 Proposed Response Response Status O

Cl 186 SC 186.2.4.6.3 P562 L51 # 14
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 The sentence: "If either..." is repeated in 186.2.4.7. No need (and may be confusing) to have the same requirement twice
 SuggestedRemedy
 Delete last sentence of 186.2.4.6.3
 Proposed Response Response Status O

Cl 186 SC 186.3.3.1.1 P568 L1 # 28
 Huang, Kechao Huawei
 Comment Type T Comment Status X
 The FEC codeword with 1376256 bits are mapped to 172032 DP-16QAM symbols, not 173032
 SuggestedRemedy
 Change "173032" to "172032" in Line 1;
 Change "173031" to "172031" in Line 2
 Proposed Response Response Status O

Cl 186 SC 186.3.3.1.2 P568 L50 # 18
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 A frame carries 7296 symbols not 175 104
 SuggestedRemedy
 Change: "for a total of 175 104 symbols per frame"
 To: "for a total of 175 104 symbols per multi-frame"
 Proposed Response Response Status O

Cl 186 SC 186.3.3.1.2 P569 L17 # 29
 Huang, Kechao Huawei
 Comment Type T Comment Status X
 In Figure 186-12, the indexes of payload symbols should be modified such that the total number of payload symbols are 172032
 SuggestedRemedy
 In Frame 0: "S<0:29>", "S<30:92>", "S<93:155>" should be changed to "S<0:19>", "S<20:82>", "S<83:145>"
 In Frame 1: "S<14195:14257>" should be changed to "S<14185:14247>"
 In Frame 23: "S<164870:164922>", "S<164923:164985>", "S<171979:172041>" should be changed to "S<164860:164912>", "S<164913:164975>", "S<171969:172031>"
 Proposed Response Response Status O

Cl 186 SC 186.3.3.1.3 P570 L51 # 30
 Huang, Kechao Huawei
 Comment Type T Comment Status X
 In Table 186-4, there are 4 pilot symbols should be modified to aligned with that in OIF 800ZR.
 SuggestedRemedy
 Index 91 YQ: "-3" should be changed to "3"
 Index 35 XQ: "-3" should be changed to "3"
 Index 41 YI: "3" should be changed to "-3"
 Index 71 XI: "-3" should be changed to "3"
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 186 SC 186.3.3.1.7 P574 L15 # 31
Huang, Kechao Huawei
Comment Type T Comment Status X
In Figure 186-14, "Insert Reserved field" should be included
SuggestedRemedy
Add "Insert Reserved field (X)" function below the "Insert TS field (X)"
Add "Insert Reserved field (Y)" function below the "Insert TS field (Y)"
Proposed Response Response Status O

Cl 186 SC 186.3.3.2.2 P575 L20 # 20
Bruckman, Leon Nvidia
Comment Type TR Comment Status X
The I and Q components shall also be identified
SuggestedRemedy
Add to the list: "Identify the I and Q component of each polarization"
Proposed Response Response Status O

Cl 186 SC 186.3.3.2.1 P574 L44 # 19
Bruckman, Leon Nvidia
Comment Type TR Comment Status X
The analog receive signals were ramed (see Figure 186-11 and its footnote)
SuggestedRemedy
Change: "Four analog signals RX_XI, RX_XQ, RX_YI, and RX_YQ"
To: "Four analog signals RX_AI, RX_AQ, RX_BI, and RX_BQ"
Proposed Response Response Status O

Cl 186 SC 186.4.2.1 P578 L18 # 118
Brown, Matt Alphawave Semi
Comment Type T Comment Status X
PCS_reset and PMA_reset definition refers to MDIO, rather than management in general.
SuggestedRemedy
Define reset, PCS_reset, and PMA_reset as done for the 1.6TBASE-R PCS in 175.2.6.2.2.
Proposed Response Response Status O

Cl 186 SC 186.3.3.2.1 P574 L44 # 202
Brown, Matt Alphawave Semi
Comment Type T Comment Status X
The signal names RX_XI, RX_XQ, RX_YI, and RX_YQ need to be renamed to match the
signal names in Figure 186-11 and in 187.5.3.
SuggestedRemedy
Rename the signals to Rx_AI, Rx_AQ, Rx_AI, Rx_AQ.
Proposed Response Response Status O

Cl 186 SC 186.6.1 P586 L5 # 366

Slavick, Jeff Broadcom

Comment Type T Comment Status X

Support of the "optional" path delay information should be presented as the first information of this section not the last.

SuggestedRemedy

Change 186.6.1 to be:
 186.6.1 PCS path data delay (optional)
 Support for the optional path data delay information is indicated by the PCS status variables PCS_delay_ns_TX_ability, PCS_delay_subns_TX_ability, PCS_delay_ns_RX_ability, and PCS_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported, the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on the start of the first non-fixed-stuff 257-bit GMP word of the tributary 0 multi-frame, where the start of the 800GBASE-ER1 tributary frame is also the start of a FEC frame, taking into account the maximum (transmit) and minimum (receive) data delay through the GMP mechanism. This corresponds to the PCS's longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
 — PCS_delay_ns_TX_max, PCS_delay_subns_TX_max
 — PCS_delay_ns_TX_min, PCS_delay_subns_TX_min
 — PCS_delay_ns_RX_max, PCS_delay_subns_RX_max
 — PCS_delay_ns_RX_min, PCS_delay_subns_RX_min

Proposed Response Response Status O

Cl 186 SC 186.6.2 P586 L25 # 367

Slavick, Jeff Broadcom

Comment Type T Comment Status X

Support of the "optional" path delay information should be presented as the first information of this section not the last.

SuggestedRemedy

Change 186.6.2 to be:
 186.6.2 PMA path data delay (optional)
 Support for the optional path data delay information is indicated by the PMA status variables PMA_delay_ns_TX_ability, PMA_delay_subns_TX_ability, PMA_delay_ns_RX_ability, and PMA_delay_subns_RX_ability. Path delay information is utilized by protocols such as time synchronization (see Clause 90).

When path delay information is supported, the transmit and receive path data delay values are reported as if the DDMP (data delay measurement point) occurs on the first data symbol of the PMA frame S<0>, corresponding to the longest delay for transmit and the shortest delay for receive. See 90.7 for more information.

Four separate delays are reported in the following eight path data delay status variables:
 — PMA_delay_ns_TX_max, PMA_delay_subns_TX_max
 — PMA_delay_ns_TX_min, PMA_delay_subns_TX_min
 — PMA_delay_ns_RX_max, PMA_delay_subns_RX_max
 — PMA_delay_ns_RX_min, PMA_delay_subns_RX_min

Proposed Response Response Status O

Cl 186 SC 186.8 P589 L1 # 326

Nicholl, Gary Cisco Systems

Comment Type TR Comment Status X

Need to update PICS to include path data delay for time synchronization (see 186.6) . See 175.9.4.7 as an example for what was done for the 1.6TBASE-R PCS in Clause 175.

SuggestedRemedy

Updated PICS to include path data delay for time synchronization. See 175.9.4.7 as an example.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

Cl 187 SC 187.3.1.2.1 P597 L38 # 176
 Huber, Thomas Nokia
 Comment Type T Comment Status X
 The names of the receive components were changed from X and Y to A and B in the 800GBASE-ER1 PMA
 SuggestedRemedy
 Change X and Y to A and B
 Proposed Response Response Status O

Cl 187 SC 187.5.1 P599 L33 # 178
 Huber, Thomas Nokia
 Comment Type T Comment Status X
 In figure 187-5, the receive signals show two sets of AI and AQ
 SuggestedRemedy
 Change the second set of signals to BI and BQ
 Proposed Response Response Status O

Cl 187 SC 187.5.1 P598 L47 # 177
 Huber, Thomas Nokia
 Comment Type T Comment Status X
 Missing a reference to the clause where the tests and measurements for the transmitter are defined.
 SuggestedRemedy
 In the text "... all transmitter measurements and tests defined in are made at TP2...", insert "187.8 and 187.9" between "in" and "are"
 Proposed Response Response Status O

Cl 187 SC 187.5.2 P600 L4 # 179
 Huber, Thomas Nokia
 Comment Type T Comment Status X
 The title of Table 187-2 needs to be modified - the PMD only deals with analog signals, not DP16QAM symbols. The table is indicating how those analog signals received from the PMA can be mapped to the inputs to the modulator.
 SuggestedRemedy
 Change the title to "Allowed analog signal to modulator input mappings"
 Proposed Response Response Status O

Cl 187 SC 187.5.1 P599 L32 # 21
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 The naming of the analog signals in Figure 187-5 is wrong
 SuggestedRemedy
 In Figure 187-5 change the second occurrence of RX_AI to RX_BI and the second occurrence of RX_AQ to RX_BQ
 Proposed Response Response Status O

Cl 187 SC 187.5.3 P600 L25 # 22
 Bruckman, Leon Nvidia
 Comment Type TR Comment Status X
 The naming of the analog signals is wrong
 SuggestedRemedy
 In the first sentence of the paragraph change the second occurrence of RX_AI to RX_BI and the second occurrence of RX_AQ to RX_BQ
 Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 187 SC 187.5.3 P600 L25 # 180

Huber, Thomas Nokia
 Comment Type T Comment Status X

In the parenthetical text, both polarizations are being identified as A

SuggestedRemedy

Change the second AI and AQ to BI and BQ

Proposed Response Response Status O

CI 187 SC 187.6.1 P602 L42 # 240

Johnson, John Broadcom
 Comment Type T Comment Status X

The units shown for Transmitter in-band OSNR (min) do not follow IEEE standard conventions

SuggestedRemedy

The intent of the unit "dB (12.5GHz)" is to indicate that the noise power density reference bandwidth is 12.5GHz. This is more properly given as a test condition in the spec Description than in the Units column, or it can be left out completely since the test method is adequately spelled out in 187.9.12.

Propose to change the spec Description to "Transmitter OSNR in 12.5 GHz band (min)" and change the unit to "dB". The spec limit is unchanged.

Proposed Response Response Status O

CI 187 SC 187.6.3 P603 L43 # 23

Bruckman, Leon Nvidia
 Comment Type TR Comment Status X

In table 187-7, the Channel insertion loss for ER1-20 is 6.5 dB, but with a loss of 0.25 dB/Km and 2 dB for the 2 dB total connection and splice loss defined in 187.7.2.1 the value should be 7 dB

SuggestedRemedy

In table 187-7 change the Channel insertion loss for ER1-20 to 7 dB

Proposed Response Response Status O

CI 187 SC 187.7 P604 L44 # 217

Stassar, Peter Huawei
 Comment Type TR Comment Status X

Note b reads "Over the wavelength range 1530 nm to 1565 nm.". This was appropriate for DWDM specifications in Clause 154 and draft CW and far too wide for a single channel coherent TX/RX specified at 193.7 THz which is 1547.7 nm. The range is +/- 1.8 GHz which is very narrow. There is no need to tie the CD range to a wavelength (range) because it's a rough upper limit as in Clause 154.

SuggestedRemedy

In Table 187-8 rewrite note b stating "at 1547.7 nm" or alternatively "at 1550 nm", which is sufficiently accurate. Also remove the reference to note b for dispersion.

Proposed Response Response Status O

CI 187 SC 187.7.2.2 P605 L # 218

Stassar, Peter Huawei
 Comment Type TR Comment Status X

Currently the maximum discrete reflectance is TBD, but it is unclear that such a specification is necessary for coherent interfaces. Especially PAM4 IMDD systems are reflection sensitive.

SuggestedRemedy

Remove subclause 187.7.2.2

Proposed Response Response Status O

CI 187 SC 187.8.1 P606 L14 # 181

Huber, Thomas Nokia
 Comment Type T Comment Status X

The test pattern listed in Table 187-10 is not aligned with the specification of test patterns in 186.2.3.13 (which points to PRBS31 rather than scrambled Idle).

SuggestedRemedy

Change the table to describe PRBS31 and point to clause 186.2.3.13.

Proposed Response Response Status O

EEE P802.3dj D1.2 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet 3rd Task Force review comment

CI 187 SC 187.9.1 P608 L28 # 142
Fetz, Brian Keysight Technologies
Comment Type T Comment Status X
A line width of 30kHz is not available on current generation test equipment and 100kHz is an acceptable maximum value.
SuggestedRemedy
change line width value from 30kHz to 100kHz in table
Proposed Response Response Status O

CI 187 SC 187.9.2 P608 L49 # 392
Pfiefle, Joerg Keysight Technologies
Comment Type T Comment Status X
A coherent front-end calibration residual I-Q skew of 0.2 ps is not available on current generation test equipment and 0.5 ps is an acceptable maximum value
SuggestedRemedy
change I-Q skew for X value from 0.2 to 0.5 in table 187-13 and analog change I-Q skew for Y value.
Proposed Response Response Status O

CI 187 SC 187.9.2 P608 L50 # 394
Pfiefle, Joerg Keysight Technologies
Comment Type T Comment Status X
There is no coherent front-end calibration for I-Q DC offset or I-Q instantaneous offset, hence there is also no post calibration residual.
SuggestedRemedy
Remove the four lines, I-Q DC offset for X, I-Q instantaneous offset for X, I-Q DC offset for Y and I-Q DC offset for Y from Table 187-13
Proposed Response Response Status O