

Clause 177 Inner FEC Counters

Comments 175, 176, 183, 493

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Supporters

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- Dave Ofelt, Juniper
- Xiang He, Huawei
- Gary Nicholl, Cisco

Introduction

- There are four comments against the counters defined for the Inner FEC decoder specified in 177.5.3.
- There are few improvements to this list of counters.
- Some wording could be improvement.
- Clarify whether counts is per FEC lane or aggregate.
- Define other useful counters(s), e.g.,
 - Uncorrectable codewords
 - Bin counters similar to RS-FEC

Counter comments against D1.0

CI 177 SC 177.5.3 P257 L29 # 183
Brown, Matt Alphawave Semi
Comment Type T Comment Status X
177.5.3 lists a few counter to be supported by the inner FEC. The definition for some of these could be improved. Further, additional counters should be included provides bins of error counts to help estimate quality of the link.
SuggestedRemedy
A contribution with more details will be provided.
Proposed Response Response Status O

CI 177 SC 177.5.3.1 P257 L45 # 493
Slavick, Jeff Broadcom
Comment Type T Comment Status X
Defining how a miscorrected codeword can occur could be phrased more clearly.
SuggestedRemedy
Change:
"Note that for soft-decision decoded Inner FEC codewords, when there is more than one bit error in a codeword, there is always a non-zero chance that miscorrection could happen."
To:
"Note that when there is more than one bit error in a codeword there is a chance that the soft decision decoder could miscorrect the codeword."
Proposed Response Response Status O

CI 177 SC 177.6.2.3 P260 L3 # 176
Ramesh, Sridhar Maxlinear Inc
Comment Type TR Comment Status X
Counters defined here do not seem consistent with those defined in Table 177-4.
SuggestedRemedy
Please make definitions of counters consistent with status variables shown on Table 177-4, page 263
Proposed Response Response Status O

CI 177 SC 177.6.2.3 P260 L3 # 175
Ramesh, Sridhar Maxlinear Inc
Comment Type TR Comment Status X
Add a counter for uncorrectable codewords (detected with additional one bit parity)
SuggestedRemedy
uncorr_cw_cnt
Counts the number of inner FEC codewords considered uncorrectable by inner FEC decoder
Proposed Response Response Status O

Counter definitions in Draft 1.0

177.5.3 Inner FEC decode

The Inner FEC decoder is a soft-decision decoder that requires a higher resolution than two bits for each received PAM4 symbols. The resolution is implementation specific and is beyond the scope of this standard. The decoder evaluates the incoming codeword and determines the most likely codeword value.

177.5.3.1 Inner_FEC_corrected_cw_counter

Editor's Note (to be removed in the next draft):

A consensus presentation is need to determine an appropriate set of counters.

A corrected Inner FEC codeword is a codeword that contained errors and was corrected or miscorrected. Note that for soft-decision decoded Inner FEC codewords, when there is more than one bit error in a codeword, there is always a non-zero chance that miscorrection could happen. The output of the Inner FEC decoder will recognize the miscorrected codewords as corrected codewords.

The Inner_FEC_corrected_cw_counter is a 32-bit counter that counts once for each corrected Inner FEC codeword when Inner_FEC_sync_status is true.

177.5.3.2 Inner_FEC_uncorrected_cw_counter

An uncorrected Inner FEC codeword is a codeword that contains errors that were not able to be corrected.

The Inner_FEC_uncorrected_cw_counter is a 32-bit counter that counts once for each uncorrected Inner FEC codeword processed when Inner_FEC_sync_status is true.

177.5.3.3 Inner_FEC_total_bits_counter

The Inner_FEC_total_bits_counter is a 64-bit counter that counts once for each bit processed by the Inner FEC decoder. This may be used together with the Inner_FEC_corrected_bits_counter (see 177.5.3.4) to roughly measure the pre-FEC BER.

177.5.3.4 Inner_FEC_corrected_bits_counter

The Inner_FEC_corrected_bits_counter is a 64-bit counter that counts once for each bit modified by the Inner FEC decoder. This may be used together with the Inner_FEC_total_bits_counter (see 177.5.3.3) to roughly measure the pre-FEC BER.

Table 177–4—Inner FEC status variables and MDIO mapping

Status variable	Variable reference	MDIO register/bit number	MDIO register/bit reference
Inner FEC sync status	177.6.2.1	1.2246.13	45.2.1.223
Inner FEC pad lock status	177.6.2.1	1.2246.14	45.2.1.223
Inner FEC corrected codewords	177.5.3	1.2276, 1.2277	45.2.1.227
Inner FEC uncorrected codewords	177.5.3	1.2278, 1.2279	45.2.1.228
Inner FEC total bits	177.5.3	1.2280, 1.2281, 1.2282, 1.2283	45.2.1.229
Inner FEC corrected bits	177.5.3	1.2284, 1.2285, 1.2286, 1.2287	45.2.1.230

Counter scope

- The counter definitions are not clear as to whether they are instantiated per flow, per FEC lane, or per aggregate of set of FEC lanes for the PHY.
- In many cases, a module may be designed to support various Ethernet rates, so with 1 lane, 2 lane, 4 lane, or 8 lane.
- There is no good reason to implement per flow.
- It would therefore be more scalable for the counters to be implemented per FEC lane (not flow).
- Also, it is likely that one FEC lane, which maps to a PMD lane, could be quite different from another. Diagnostics per FEC/PMD lane could be very helpful.
- Proposal is to explicitly define the counters as being implemented one per FEC lane.
 - The aggregate for a whole PHY with multiple lanes can be accumulated by software, if necessary.

Status variables

- The counters defined in 177.5.3 appear with no context.
 - Consider adding new subclause under 177.5.3 (it would be 175.5.3.1) called “Decoder counters” and change 177.5.3.1 through 177.5.3.4 to level 5 headers starting with 177.5.3.1.1.
 - This might be the correct place to discuss the scope of the counters as discussed on the previous slide.
- Subclause 177.7 should be moved to the end of the clause, just before 177.7 (PICS) to be consistent with other clauses in this draft.
- The status variables names in Table 177-4 do not match the names in 177.5.3.
 - Update the status variable names in Table 177-4 to match the counters in 177.5.3.
- The subclause references in Table 177-4 are to the decoder subclause rather than the individual counter subclauses
 - Update the subclause reference to the subclause that defines the counter.

Bin counters, intro

- For the RS-FEC used in the 800GBASE-R PCS and 1.6TBASE-R PCS, counters are provided counting the number of codewords with 1, ... 15, errors are provided.
- This set of counters, in combination with uncorrectable counters, provides a high-resolution histogram of the number of errors in a large block of bits or PAM4 symbols.
- These bins can be used to estimate the quality of the link, perhaps differentiating between lightly correlated and heavily correlated errors and to extrapolate UCR (uncorrectable codeword ratio).
- A similar approach would be helpful for the Inner FEC, since an optical module would have no visibility of the RS-FEC counters, unless it implements an offline RS-FEC decoder.

Bin counters, option #1

- One simple and obvious approach is as follows...
- Three or more bin counters as follows:
 - Number of codewords with 1 bit error corrected
 - Number of codewords with 2 bits corrected
 - Number of codewords with 3 (or more) bits corrected
 - Never incremented if decoder is not capable of correcting more than 2 bits
- “Corrected” means that a bit was modified by the assumed value provided as input to the decoder.
- The counters might provide visibility into how close to edge the inner FEC might be but does not give ability to extrapolate to probability of larger groups of errors.

Bin counters, option #2

- Another more complex approach follows...
- If error binning is done over a larger block of data, then better resolution of error probabilities is possible.
- Counter bins based a group of 8 codewords (8x120 – 960 bits), one from each flow.
- Bins for 1 to 24 error bit errors
- For each block sum errors from each codeword:
 - +0 if no bit errors detected/corrected
 - +1 if one bit error detected/corrected
 - +2 if two bit errors detected/corrected
 - +3 otherwise (3 or more errors detected, uncorrectable)
- Possible alternates:
 - Count only codewords with errors.
 - Increase block size for better resolution.

Summary

- Some improvements to the current counter specifications are proposed.
- Also, expanding the counter list to include binned error counters is along with two options are proposed.
 - These may need so verification before adopting.

Thanks