Timestamp Accuracy for Inner FEC sublayers (Clause 177 and 184)

For comments #369, #370, #603, #604 & #605

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Introduction

- IEEE 802.3cx-2023 resolved multiple causes that could affect PTP timestamp accuracy
  - Inconsistent message timestamp point – start of SFD vs start of symbol after SFD
  - Path delay variance from idle insertion/removal and alignment markers
  - Multi-PCS lane distribution path delay variance
- For P802.3dj, there are two clauses with Inner FEC sublayer with similar logic as multi-PCS lane distribution, that could affect PTP timestamp accuracy.
- This presentation will go over different causes and propose a solution.

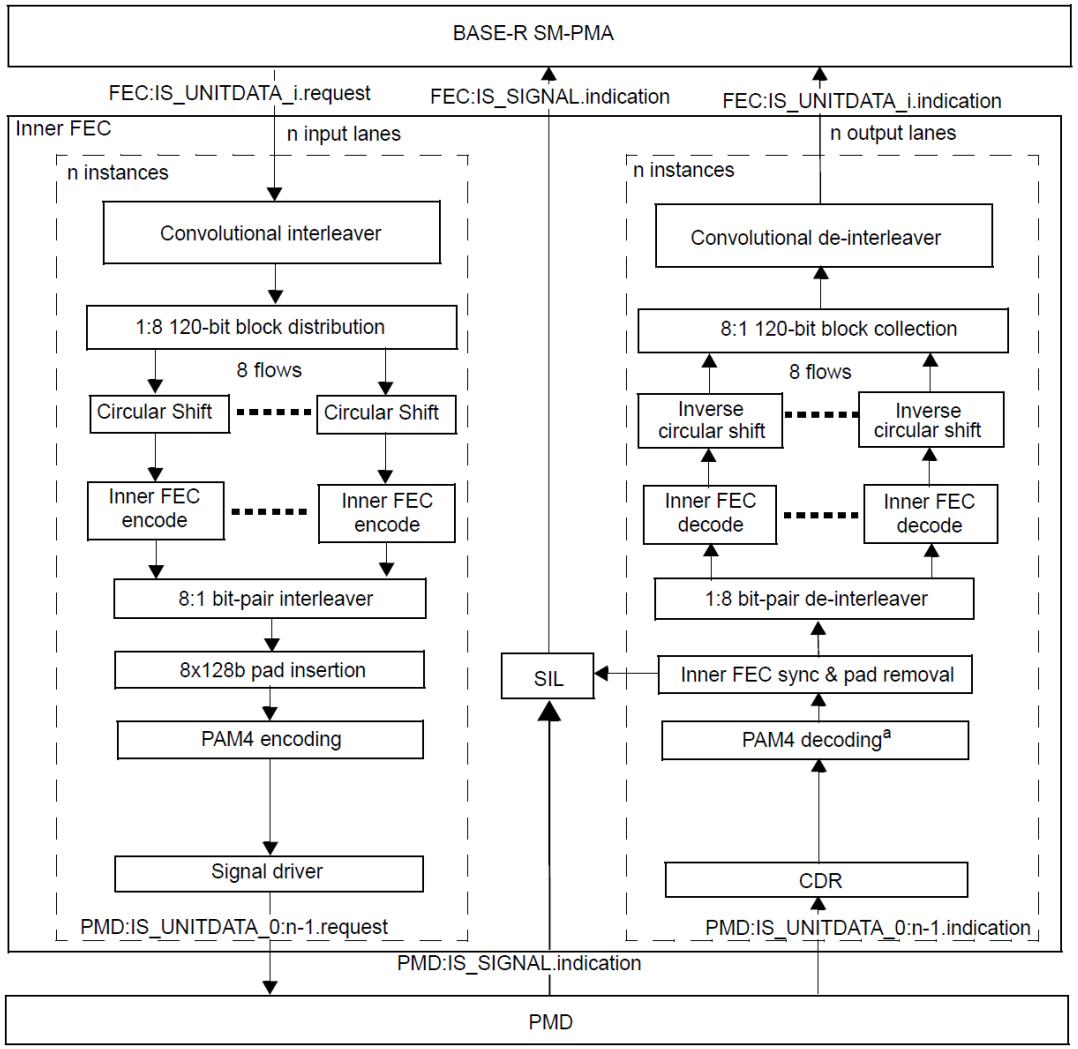
- Note: MII Extenders could co-exist with Inner FEC, and the timestamp accuracy over an MII Extender is a separate topic irrelevant to the Inner FEC itself.

Revisit: 802.3cx approach

- Fixed delays are reported.
  - Includes fixed logic delays, whether intrinsic or implementation dependent.
- Unpredictable dynamic delays are compensated.
  - Idle and AM insertion/deletion and other dynamic delays can be compensated by Dynamic path data delay (aka NUM_BIT_CHANGE)
- Cyclical delay variation through the PHY relies on Tx-Rx cancellation.
  - The transmit and receive path data delays are reported **as if the DDMP* is at the start** of the FEC codeword and/or **at the start** of the PCS lane distribution sequence.
  - Allocate **max delay for the Tx** path data delay and **min delay for the Rx** path data delay

*DDMP: data delay measurement point, either the beginning of the start-of-frame delimiter or the beginning of the first symbol after the SFD (used by IEEE Std 1588 Precision Clock Synchronization Protocol for Networked Measurement and Control Systems)

Contributors Affecting Timestamp Accuracy in Clause 177



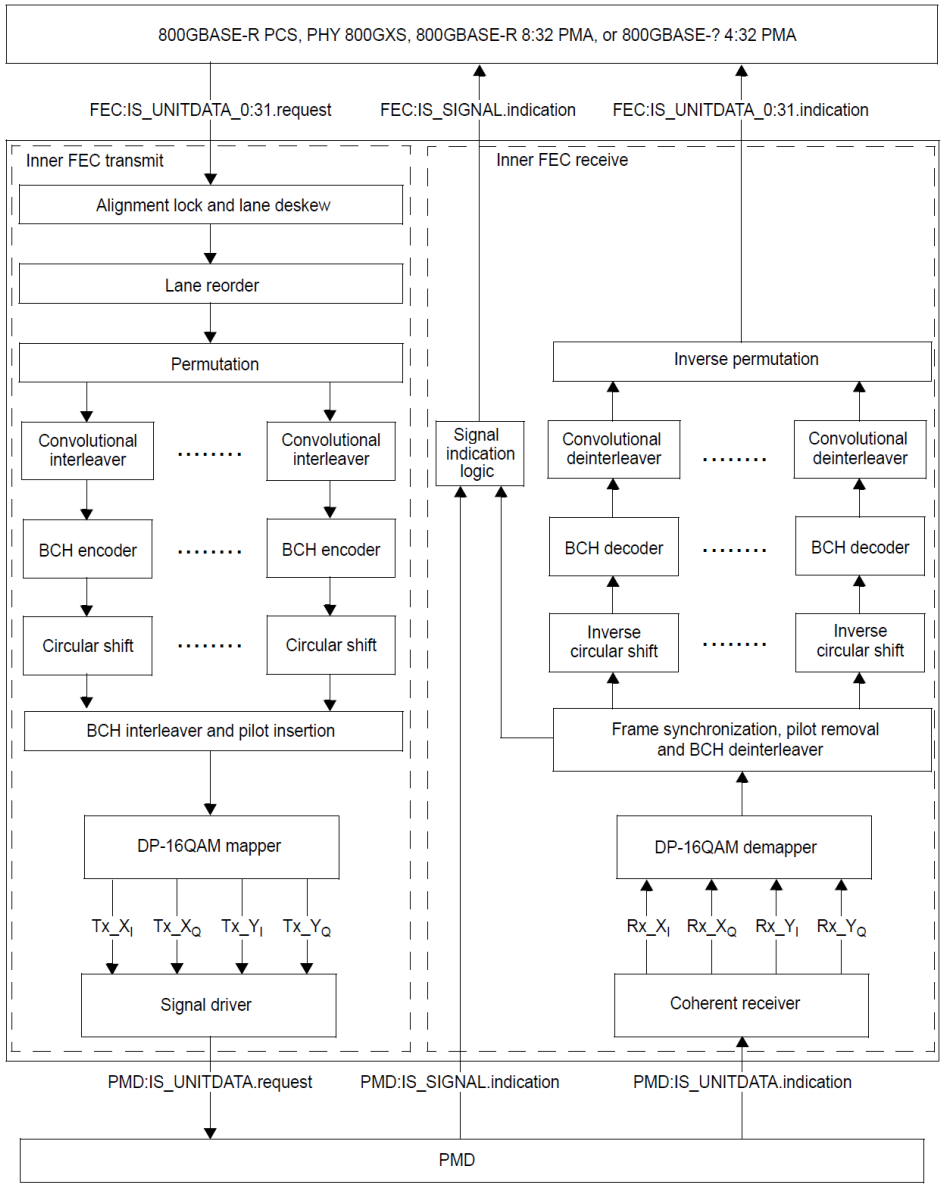
- Convolutional interleaver
  - The DDMP could land on any of the 3 delay lines, resulting in as much as 15360 bits, or **216.8 ns** of uncertainty.
- 1:8 120-b block distribution
  - Same effect as multi-PCS lane distribution. Max timestamp uncertainty could be 960 bits, or **4.5 ns**.
- Circular shift
  - 8 flows with different shifts: 100 bits, or **3.8 ns.**
- Inner FEC encode
  - 8 bits parity bits, or 0.28 ns.
- 8x128b pad insertion
  - 1024 bits, or **4.5 ns**.
- Phase effect between the Outer and Inner FEC*
  - The uncertainty caused by the relative phase between the Outer FEC parity and inner FEC parity bits: 2.2 ps – not worth considering
  - The uncertainty caused by the relative phase between the Outer FEC parity and Inner FEC pad bits: 11.75 ps – not worth considering

* See backup slides for detailed calculations

Proposed solution – use the 802.3cx method

- Reusing 802.3cx idea for dynamic intrinsic delays for all contributors, and always report the path data delays as if the DDMP is at:
  - Line 0 of the convolutional interleaver/deinterleaver;
  - The start of flow 0 of 1:8 120-bit block distribution and 8:1 120-bit block collection;
  - The start of each Inner FEC codeword;
  - The first bit of the payload following each 8*128b pad.
- The maximum and minimum delays are allocated to the Inner FEC transmit and receive side, respectively.
- Circular shift function may require further considerations
  - Two implementations on the receive side may exist: continue shifting $(12 - n)$ RS-FEC symbols in the same direction, or inversely shift $(-n)$ RS-FEC symbols, where n is the number of RS-FEC symbols shifted on the transmit side.
  - Both implementations should be allowed, but they will results in different path data delays as much as 120 bits, or 4.5 ns, which could have the same effect as asymmetric fiber lengths.
  - It should be taken care of when reporting the maximum and minimum path data delays.

Path Data Delay Uncertainties in Clause 184



- Similarly as Clause 177, there are multiple contributors to delay measurement uncertainties:
  - Permutation
  - Convolutional interleaver
  - BCH encoder
  - Circular shift
  - Pilot insertion

- The same proposal on slide #5 is recommended for Clause 184.

Summary

- For Clause 177 and 184 Inner FEC sublayer, PTP timestamp accuracy can be maintained if we follow 802.3cx method.
- The **maximum** delays caused by various processes are allocated to the **transmit** side, and the **minimum** delays are allocated to the **receive** side.
- Associated registers for the Inner FEC sublayers will be needed for Inner FEC Tx/Rx path data delays (and their ability for sub-nanosecond values), like other layers.

Proposed Changes to D1.0

- Add following register sets in Clause 45. (Recommend to use MMD 14)
  - TimeSync Inner FEC capability: 14.1800
    - 14.1800.0: TimeSync receive path data delay ability, in ns
    - 14.1800.1: TimeSync transmit path data delay ability, in ns
    - 14.1800.2: TimeSync receive path data delay ability, in sub-ns
    - 14.1800.3: TimeSync transmit path data delay ability, in sub-ns
    - 14.1800.15:4: Reserved, always “0”.
  - TimeSync Inner FEC transmit path data delay:
    - 14.1801.15:0: Maximum Inner FEC transmit path data delay in ns, lower
    - 14.1802.15:0: Maximum Inner FEC transmit path data delay in ns, upper
    - 14.1803.15:0: Minimum Inner FEC transmit path data delay in ns, lower
    - 14.1804.15:0: Minimum Inner FEC transmit path data delay in ns, upper
    - 14.1809.15:0: Maximum Inner FEC transmit path data delay in sub-ns
    - 14.1810.15:0: Minimum Inner FEC transmit path data delay in sub-ns
  - TimeSync Inner FEC receive path data delay:
    - 14.1805.15:0: Maximum Inner FEC receive path data delay, lower
    - 14.1806.15:0: Maximum Inner FEC receive path data delay, upper
    - 14.1807.15:0: Minimum Inner FEC receive path data delay, lower
    - 14.1808.15:0: Minimum Inner FEC receive path data delay, upper
    - 14.1811.15:0: Maximum Inner FEC transmit path data delay in sub-ns
    - 14.1812.15:0: Minimum Inner FEC transmit path data delay in sub-ns
  - TimeSync Inner FEC configuration
    - 14.1813.13: Data delay measurement point, 0 = DDMP at the beginning of the SFD; 1 = DDMP at the beginning of the first symbol after the SF
- Provide corresponding behavior descriptions in 30.13.1.1 – 30.13.1.14

Thank you!

Backup – Phase effect between Outer and Inner FEC

Inner FEC + Outer FEC phase effect on latency (800GE example)

- **Outer FEC saw-tooth:**
  - Height: 1200 bits (4 codewords, 300 bits of parity each) at the PCS output = 37.5 bits per 26.5625Gbps PCS lane = 1.4118 ns
    - Same as 1200 MDI bits*(514/544)*(256/257) = 1129.4118 MII bits = 1.4118 ns
  - Period : FEC codeword is 4*5440 bits = 20480 MII bits = 25.6 ns
  - Saw-tooth slope = 1.4118 / 25.6 = 0.0551
- **Inner FEC pad block saw-tooth:**
  - Height = 128b per 28.359375 Gbps lane = 4.5135 ns
  - Period = 128b/cw*8712cw per 8*28.359375 Gbps lane = 4915.2ns = 192 Outer FEC code-words.
    - Same as 120b/cw * 8704cw * (514/544) * (256/257) = 3932160 MII bits = 4915.2 ns
    - One inner FEC pad block period = 192 outer FEC periods.
  - Slope = 4.5135 / 4915.2 = 0.000918

- **Overall Inner FEC pad block saw-tooth vs outer FEC effect is minimal**
  The maximum timestamp error effect due to arbitrary phase between the saw-tooths above will be:
  = (Inner-FEC pad saw-tooth height) / (2*(outerFEC periods per inner FEC pad period))
  = 4.5135 ns / (2*192)
  = 11.75 ps. Worth considering? – Probably not.

- **Inner FEC parity bits saw-tooth vs outer FEC:**
  - Height 8 bits per 28.359375 Gbps lane = 0.282 ns
  - Period = 128b per 28.359375 Gbps lane = 4.5135 ns.
    - Expressed in MII bits: 120bits/lane*32lanes/MII*(8704/8712)*(514/544)*(256/257) = 3610.7989 MII bits = 4.5135 ns
    - 64 outer FEC periods = 363 inner FEC periods.
  - Slope = 0.062478
  - The uncertainty between the output FEC parity sawtooth and inner FEC parity sawtooth is
    - Over 363 inner FEC saw-tooths, the RS_FEC sawtooth will fall at 64 different locations with respect to the inner FEC saw-tooth.
    - The max difference from purely additive is when the RS_FEC sawtooth falls at half of a 64th of the inner FEC sawtooth
    - (inner FEC parity bits saw-tooth height) / (2*(outer FEC periods per integer inner FEC periods))
    - 0.282ns / (2*64) = 2.2ps. Definitely not worth considering.