Choosing an Optimum Reference Receiver for 200Gbps/Lane C2M

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Outline

- Background and Introduction
- Update to C2M Link Simulation based on COM 4.5beta3
- Reference Receiver Parameters Study
- Proposed Changes to Table 176E–7

Background and Introduction

- A wide range of reference receiver parameters were used for C2M analysis
- In 802.3dj D1.0, lots of TBDs are gated by C2M IL budget

- Investigation highlights
  - C2M ILdd target: [28:2:34] dB
  - Number of Rx FFE fixed-position taps: [8:4:24]
  - Number of pre-cursor taps: [4:6]
  - Requirement of Rx FFE floating taps: [0:1] banks

Channel Test Cases

- Channel source: [Tools & Channels]

C2M Channel Source	Test Cases
rabinovich_3df_01_2209	3
rabinovich_3df_02_2209	3
rabinovich_3dj_02_230116	1
rabinovich_3dj_03_230116	1
shanbhag_3dj_03_2305	6
akinwale_3dj_02_2307	28
akinwale_3dj_03_2307	27
akinwale_3dj_04_2307	28
lim_3dj_01_230629	1
lim_3dj_02_230629	1
weaver_3dj_elec_02_230831	32
lim_3dj_06_2309	1
gore_3dj_elec_02_231026	18
kareti_3dj_elec_02_240111	60
Total	**210**

- Host package model follows 802.3dj D1.0 Table 179–15
- Module package uses Class A model except z_p(1) = 8 and z_p(2) = 0 for both Test 1 and Test 2

Table 179–15—Device, package, and PCB model parameters

Parameter	Symbol	Value	Units
Device model			
Single-ended device capacitance for stage 1	$C_d^{(1)}$	40×10^{-6}	nF
Single-ended device capacitance for stage 2	$C_d^{(2)}$	90×10^{-6}	nF
Single-ended device capacitance for stage 3	$C_d^{(3)}$	110×10^{-6}	nF
Single-ended device series inductance for stage 1	$L_s^{(1)}$	0.13	nH
Single-ended device series inductance for stage 2	$L_s^{(2)}$	0.15	nH
Single-ended device series inductance for stage 3	$L_s^{(3)}$	0.14	nH
Single-ended bump capacitance	C_b	30×10^{-6}	nF
Class A package model			
Transmission line parameter γ_0	γ_0	5×10^{-4}	1/mm
Transmission line parameter a_1	a_1	8.9×10^{-4}	$ns^{1/2}$/mm
Transmission line parameter a_2	a_2	2×10^{-4}	ns/mm
Transmission line parameter τ	τ	~~6.141×10^{-4}~~ 6.141e-3	ns/mm
Transmission line 1 length, Test 1	$z_p^{(1)}$	33	mm
Transmission line 1 length, Test 2	$z_p^{(1)}$	12	mm
Transmission line 1 characteristic impedance	$Z_c^{(1)}$	87.5	Ω
Transmission line 2 length	$z_p^{(2)}$	1.8	mm
Transmission line 2 characteristic impedance	$Z_c^{(2)}$	92.5	Ω
Single-ended package capacitance at package-to-board interface	C_p	40×10^{-6}	nF
Class B package model			
Transmission line parameter γ_0	γ_0	5×10^{-4}	1/mm
Transmission line parameter a_1	a_1	6.5×10^{-4}	$ns^{1/2}$/mm
Transmission line parameter a_2	a_2	2.93×10^{-4}	ns/mm
Transmission line parameter τ	τ	~~6.141×10^{-4}~~ 6.141e-3	ns/mm
Transmission line 1 length, Test 1, Tx / Rx	$z_p^{(1)}$	45 / 44	mm
Transmission line 1 length, Test 2, Tx / Rx	$z_p^{(1)}$	30 / 29	mm
Transmission line 1 characteristic impedance	$Z_c^{(1)}$	87.5	Ω
Transmission line 2 length	$z_p^{(2)}$	2	mm
Transmission line 2 characteristic impedance	$Z_c^{(2)}$	95	Ω
Transmission line 3 length	$z_p^{(3)}$	1.3	mm
Transmission line 3 characteristic impedance	$Z_c^{(3)}$	100	Ω
Transmission line 4 length	$z_p^{(4)}$	1.5	mm
Transmission line 4 characteristic impedance	$Z_c^{(4)}$	78	Ω
Single-ended package capacitance at package-to-board interface	C_p	40×10^{-6}	nF

COM Configuration

- **Simulator: COM 4.5beta3**

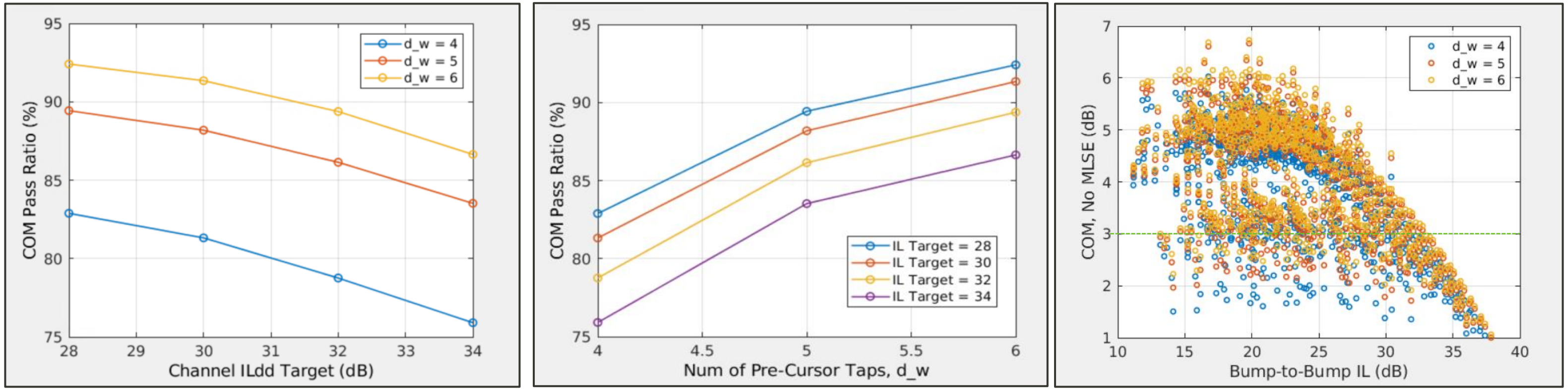
Table 93A-1 parameters			
Parameter	**Setting**	**Units**	**Information**
f_b	106.25	GBd	
f_min	0.05	GHz	
Delta_f	0.01	GHz	
C_d	[0.4e-4 0.9e-4 1.1e-4 ;0.4e-4 0.9e-4 1.1e-4]	nF	[TX RX]
L_s	[0.13 0.15 0.14; 0.13 0.15 0.14]	nH	[TX RX]
C_b	[0.3e-4 0.3e-4]	nF	[TX RX]
R_0	50	Ohm	
R_d	[46.25 46.25]	Ohm	[TX RX]
PKG_NAME	PKG_LowR_CLASSA PKG_Module		TX RX
A_v	0.413	V	
A_fe	0.413	V	
A_ne	0.608 *	V	
z_p select	[1 2]		
L	4		
M	32		
filter and Eq			
f_r	0.58	*fb	
c(0)	0.5		min
c(-1)	[-0.34:0.02:0]		[min:step:max]
c(-2)	[0:0.02:0.12]		[min:step:max]
c(-3)	0		[min:step:max]
c(1)	[-0.2:0.02:0]		[min:step:max]
N_b	1	UI	
b_max(1)	0.75		As/dffe1
b_max(2..N_b)	0		As/dfe2..N_b
b_min(1)	0		As/dffe1
b_min(2..N_b)	0	S	As/dfe2..N_b
g_DC	0	dB	[min:step:max]
f_z	42.5	GHz	
f_p1	42.5	GHz	
f_p2	106.25	GHz	
g_DC_HP	[-6:1:0]		[min:step:max]
f_HP_PZ	1.328125	GHz	
Butterworth	1	logical	include in fr

I/O control		
DIAGNOSTICS	0	logical
DISPLAY_WINDOW	0	logical
CSV_REPORT	0	logical
RESULT_DIR	.\results\CRKR_{date}\	
SAVE_FIGURES	0	logical
Port Order	[1 3 2 4]	
RUNTAG	KR_set1_eval_	
COM_CONTRIBUTION	1	logical
TDR and ERL options		
TDR	1	logical
ERL	1	logical
ERL_ONLY	0	ns
TR_TDR	0.01	
N	4000	logical
TDR_Butterworth	1	
beta_x	0	
rho_x	0.618	
TDR_W_TXPKG	0	UI
N_bx	0	
fixture delay time	[0 0]	
Tukey_Window	1	
Noise, jitter		UI
sigma_RJ	0.01	UI
A_DD	0.02	V^2/GHz
eta_0	1.25E-08	dB
SNR_TX	33	
R_LM	0.95	

Operational		
ERL Pass threshold	10	dB
COM Pass threshold	3	db
DER_0	2.00E-05	
T_r	0.004	ns
FORCE_TR	1	logical
PMD_type	C2C	
EW	1	
MLSE	0	logical
ts_anchor	1	
sample_adjustment	[-16 16]	
Local Search	0	
Filter: Rx FFE		
ffe_pre_tap_len	5	UI
ffe_post_tap_len	12	UI
ffe_pre_tap1_max	1	
ffe_post_tap1_max	1	
ffe_tapn_max	1	
FFE_OPT_METHOD	MMSE	
num_ui_RXFF_noise	4096	
Floating Tap Control		
N_bg	0	0 1 2 or 3 groups
N_bf	4	taps per group
N_f	60	UI span for floating taps
bmaxg	1	max DFE value for floating taps
B_float_RSS_MAX	1	rss tail tap limit
N_tail_start	11	(UI) start of tail taps limit
RXFFE FLOAT CTL	FOM	

** Was 0.45 in lit_3dj_01a_2403*

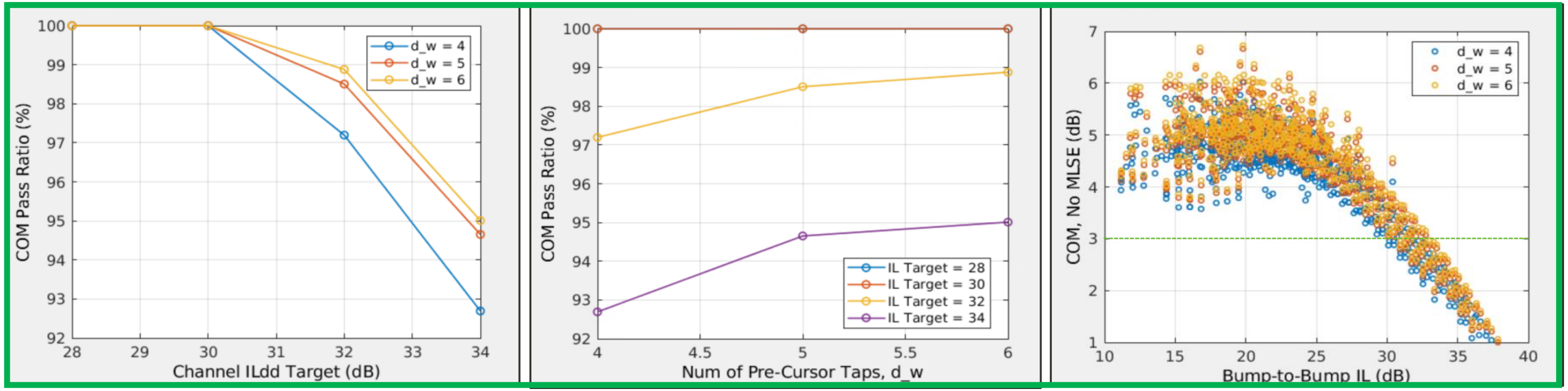
COM vs RX FFE Pre-Tap Length



For this set of data

- N_fix = 8
- N_g = 0
- MLSE = 0

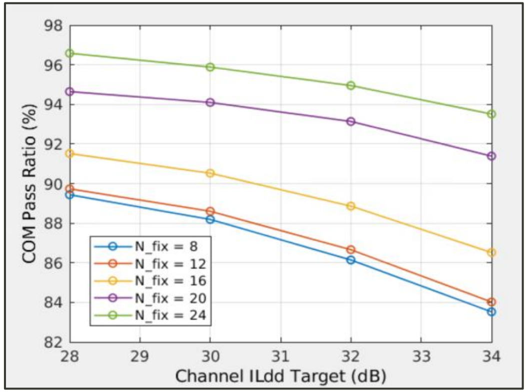
- Further increasing number of pre-taps from 5 is less helpful

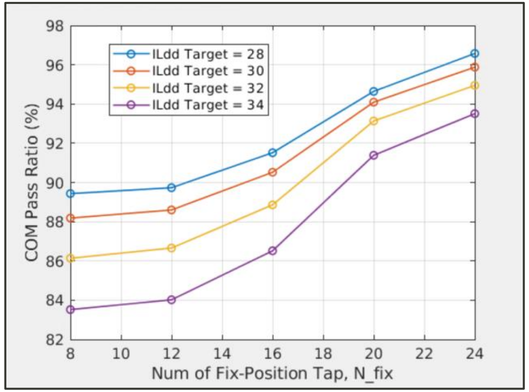


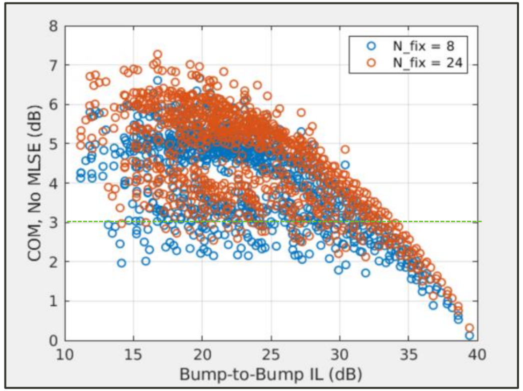
Removed
512 Radix channels

** Pass criteria: COM >= 3dB & Channel bump-to-bump IL <= ILdd target*

COM vs RX FFE Fixed-Tap Length



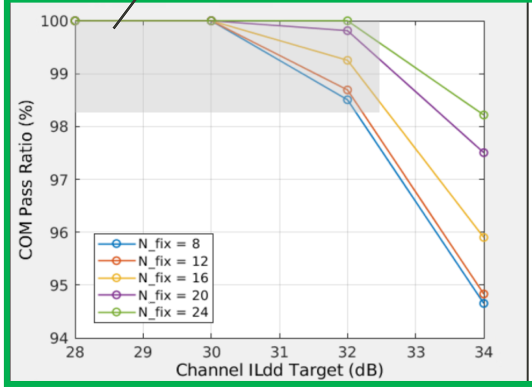


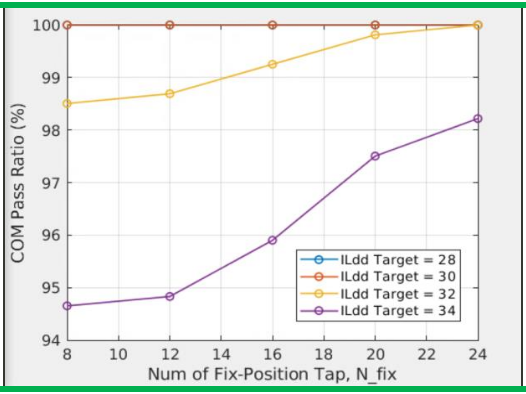


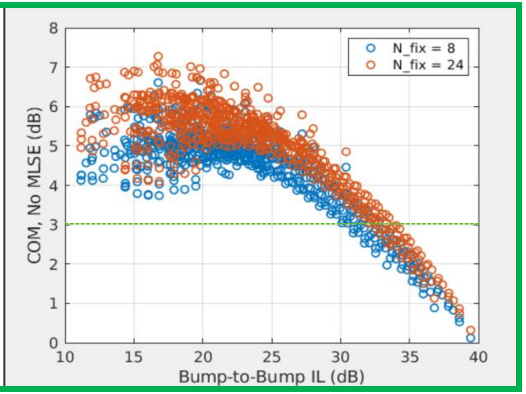
For this set of data

- d_w = 5
- N_g = 0
- MLSE = 0

N_fix = 8 can cover > 98% channels with ILdd target <= 32







Removed 512 Radix channels

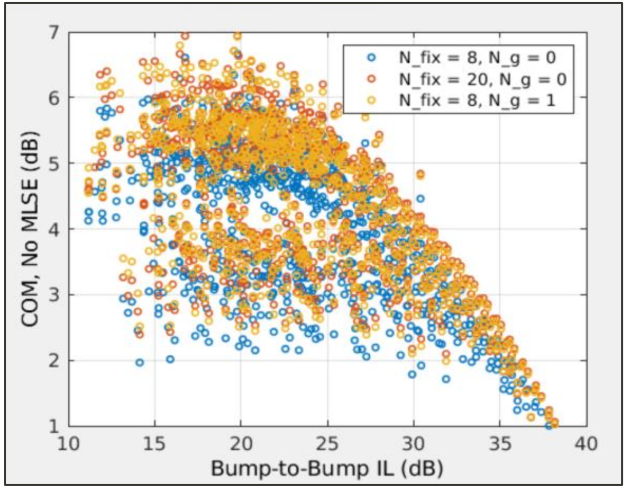
** Pass criteria: COM >= 3dB & Channel bump-to-bump IL <= ILdd target*

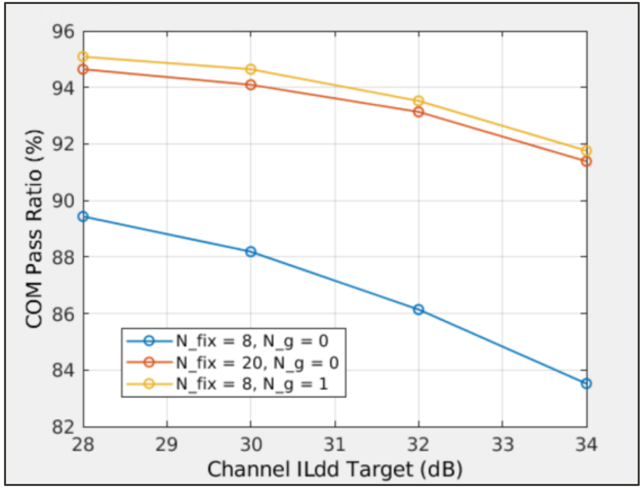
COM with Floating-Tap Enabled

- **Floating taps can provide higher flexibility and can use a fewer taps to achieve comparable performance than using fixed taps only**

For this set of data

- **d_w = 5**
- **N_f = 4**
- **N_max = 60**
- **MLSE = 0**

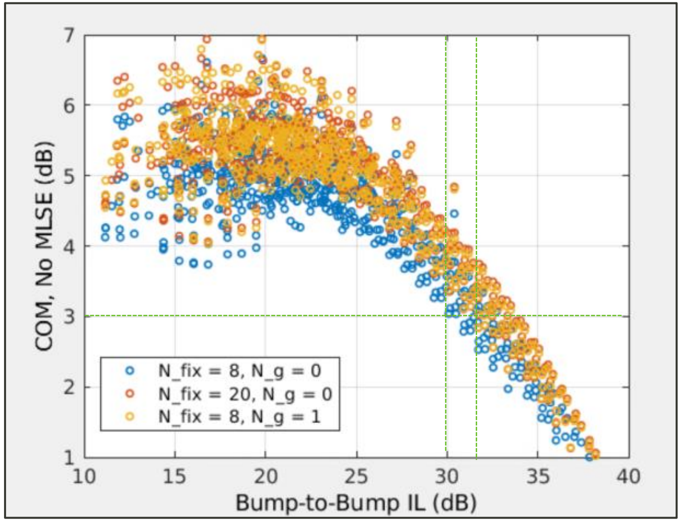




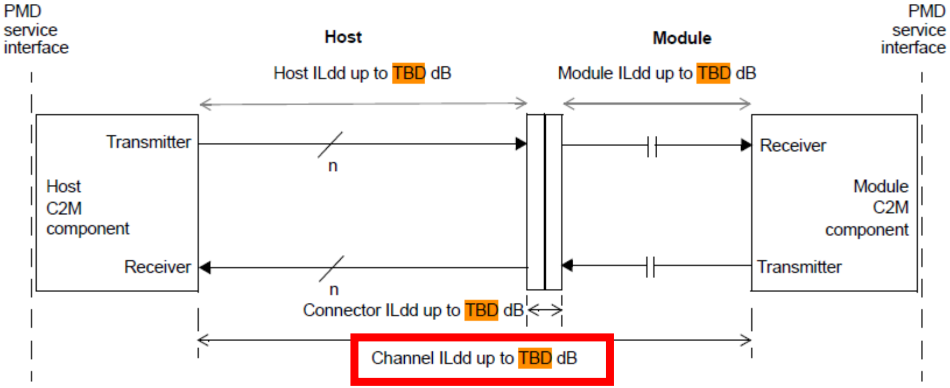
** Pass criteria: COM >= 3dB & Channel bump-to-bump IL <= ILdd target*

Choosing An Optimum Reference Receiver

	d_w	N_fix	N_g*N_f	N_max	MLSE	EQ Power	Associated CH ILdd Budget
FFE Fixed Tap Only	5	8	0	-	0	Low	<= 30 dB
~~FFE Fixed Tap Only~~	5	20	0	-	0	High	<= 32 dB
FFE Fixed Taps + Floating Taps	5	8	1*4	60	0	Med	<= 32 dB



Removed 512 Radix channels



NOTE—The number of lanes n is equal to 1 for 200GAUI-1, 2 for 400GAUI-2, 4 for 800GAUI-4, and 8 for 1.6TAUI-8.

Figure 176E–2—Components of a 200 Gb/s per lane AUI-C2M interface and insertion loss budget at 53.125 GHz

Proposal

- Proposed COM parameter values to Table 176E–7

Parameter	Symbol	Value	Units
Signaling rate	f_b	106.25	GBd
Maximum start frequency	f_{min}	0.05	GHz
Maximum frequency step	Δf	0.01	GHz
Device model TBD		Same with Table 179–15 (Host side)	
Package model TBD	TBD	TBD	
Single-ended reference resistance	R_0	50	Ω
Single-ended transmitter termination resistance	$R_d^{(t)}$	TBD	Ω

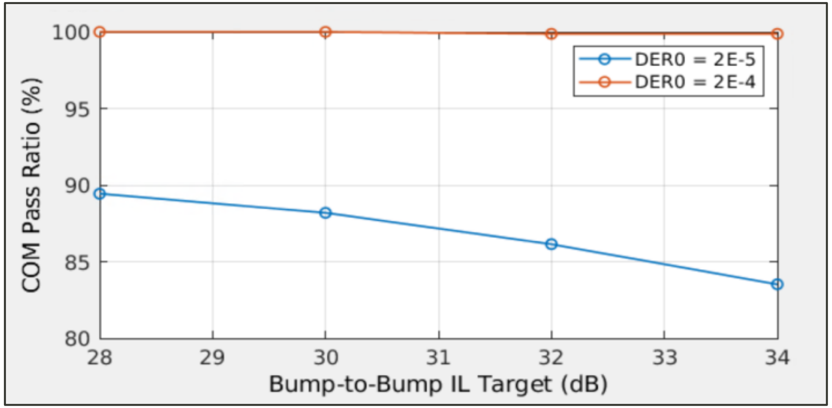
Parameter	Symbol	Value	Units
Number of samples per unit interval	M	32	—
Receiver discrete-time equalizer parameters Number of pre-cursor taps Number of fixed-position taps Number of floating tap groups Number of taps per floating tap group Highest allowed tap index Normalized upper limit on feed-forward coefficient $w(j)$ Normalized lower limit on feed-forward coefficient $w(j)$ Number of feedback taps Normalized upper limit on feedback coefficient b(j) Normalized lower limit on feedback coefficient b(j)	 d_w N_{fix} N_g N_f N_{max} $w_{max}(j)$ $w_{min}(j)$ N_b $b_{max}(j)$ $b_{min}(j)$	 5 8 1 4 60 TBD TBD 1 0.75 0	 — — — — — — — — — —
Target detector error ratio	DER_0	2×10^{-5}	—

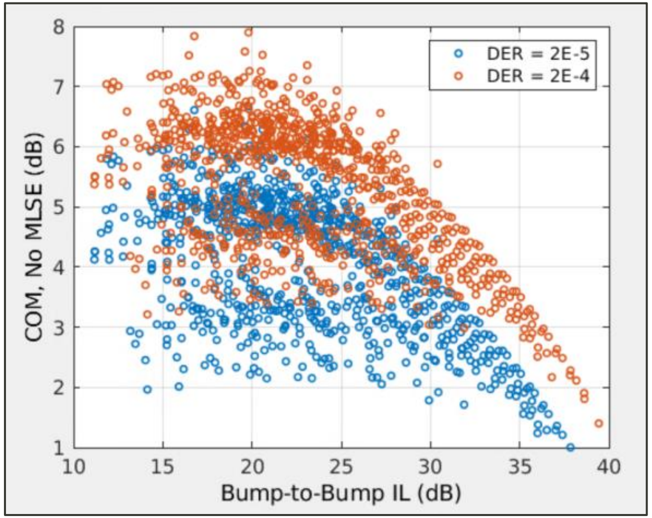
Parameter	Symbol	Value	Units
Single-ended receiver termination resistance	$R_d^{(r)}$	TBD	Ω
Receiver 3 dB bandwidth	f_r	0.58*fb ~62GHz	
Transmitter equalizer, coefficient –3 Minimum value Maximum value Step size	$c(-3)$	TBD	—
Transmitter equalizer, coefficient –2 Minimum value Maximum value Step size	$c(-2)$	0:0.02:0.12	—
Transmitter equalizer, coefficient –1 Minimum value Maximum value Step size	$c(-1)$	-0.34:0.02:0	—
Transmitter equalizer, coefficient 0 Minimum value	$c(0)$	0.5	—
Transmitter equalizer, coefficient 1 Minimum value Maximum value Step size	$c(1)$	-0.2:0.02:0	—
Continuous time filter, gain 1 Minimum value Maximum value Step size	g_1	TBD	 dB dB dB
Continuous time filter, gain 2 Minimum value Maximum value Step size	g_2	-6:1:0	 dB dB dB
Continuous time filter, zero 1 frequency for g_1=0 Continuous time filter, zero 1 frequency for g_2=0	f_{z1} f_{z2}	fb/2.5 fb/80	GHz GHz
Continuous time filter, pole 1 frequency Continuous time filter, pole 2 frequency Continuous time filter, pole 3 frequency	f_{p1} f_{p2} f_{p3}	fb/2.5 fb fb/80	GHz GHz GHz
Transmitter differential peak output voltage Victim Far-end aggressor Near-end aggressor	 A_v A_{fe} A_{ne}	 0.413 0.413 0.608	 V V V
Transmitter transition time	T_r	0.004	ns
Number of signal levels	L	4	—
One-sided noise spectral density	η_0	1.25E-8	V^2/GHz
Transmitter signal-to-noise ratio	SNR_{TX}	33	dB
Random jitter, RMS	σ_{RJ}	TBD	UI
Dual-Dirac jitter, peak	A_{DD}	TBD	UI
Level separation mismatch ratio	R_{LM}	0.95	—

Appendix

COM vs DER0

- For this set of data, d_w = 5, N_fix = 8, N_g = 0, and MLSE = 0
- All the channels can comfortably exceed COM of 3dB with FEC termination (DER0 = 2E-4)





** Pass criteria: COM >= 3dB & Channel bump-to-bump IL <= ILdd target*

Thank you

Questions and Discussions