

PMA with RS-FEC symbol multiplexing test vectors

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This presentation

- Provides PMA sublayer (CL176) interoperability test vectors
- Comment #298 was submitted by the author to include CL176 test vectors in the draft.

<i>Cl</i> 176	<i>SC</i> 176C	<i>P</i> 594	<i>L</i> 1	# 298
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<i>Comment Type</i> T	<i>Comment Status</i> X			
Annex 176C "SM-PMA test vectors" is currently empty.				
<i>SuggestedRemedy</i>				
Add test vectors for 200GBASE-R 8:1, 400GBASE-R 16:2, 800GBASE-R 32:4, and 1.6TBASE-R 16:8 to Annex 176C based on supporting contribution on May interim.				
<i>Proposed Response</i>	<i>Response Status</i> ○			

Background

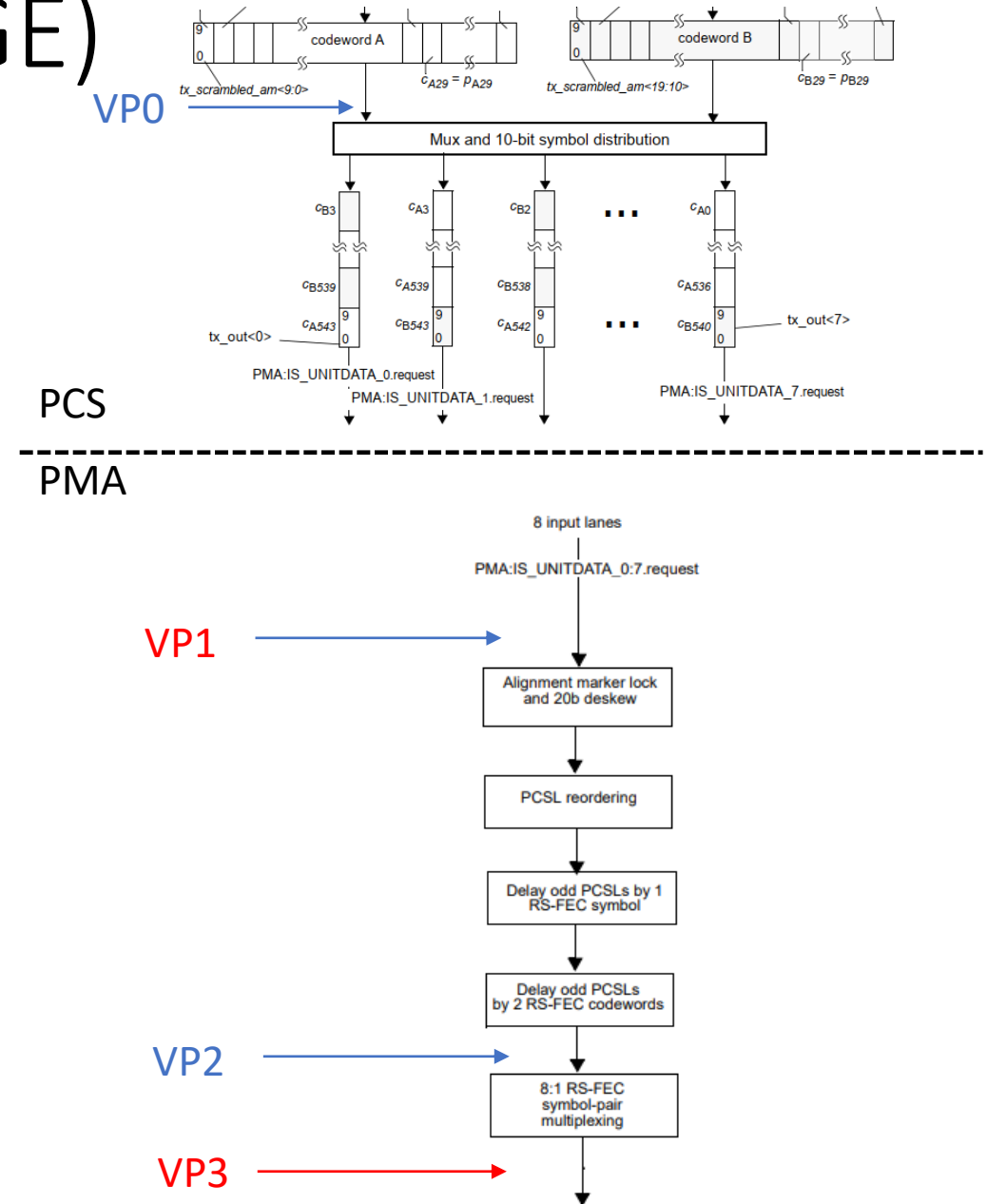
- Clause 176 PMA with RS-FEC symbol muxing was adopted for 200GBASE-R, 400GBASE-R, 800GBASE-R and 1.6TBASE-R using 200G/lane AUIs or PMDs
- RS-FEC symbol muxing ([ran 3dj 01a 2303.pdf](#)) was adopted ([March 2023 Plenary, Motion #4](#)).
- 4x RS-FEC codewords interleaving for 200GE and 400GE using 200G/lane AUIs or PMDs ([he 3dj 02a 2307](#)) was adopted ([July 2023 Interim, Motion #10](#)).

Test vectors - general

- The PMA test vectors can be used during development to check for interoperability.
- Test vectors input
 - Valid PCS data with AM which enables checking for interoperability with PCS.
 - The PCS data is with zero skew between PCS lanes, which can result from a direct connection to a PCS. This is an assumption for vectors generation, in practice other cases are also possible.
- Test vectors address following sections of CL176 (based on draft 1.0):
 - 200GBASE-R 8:1 (CL 176.5.1)
 - 400GBASE-R 16:2 (CL 176.6.1)
 - 800GBASE-R 32:4 (CL 176.7.1)
 - 1.6TBASE-R 16:8 (CL 176.8.1)
- Acronym VP (Vector Point) is used for reference points for which vectors are available.

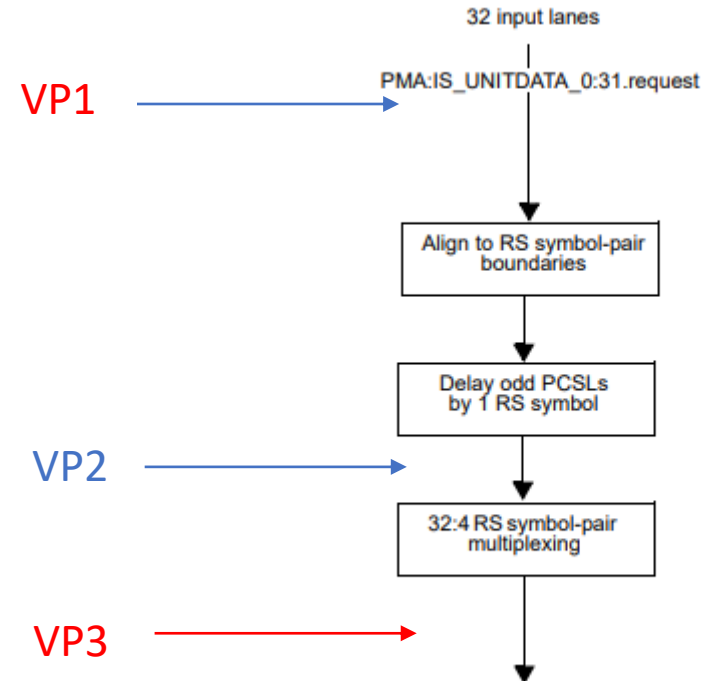
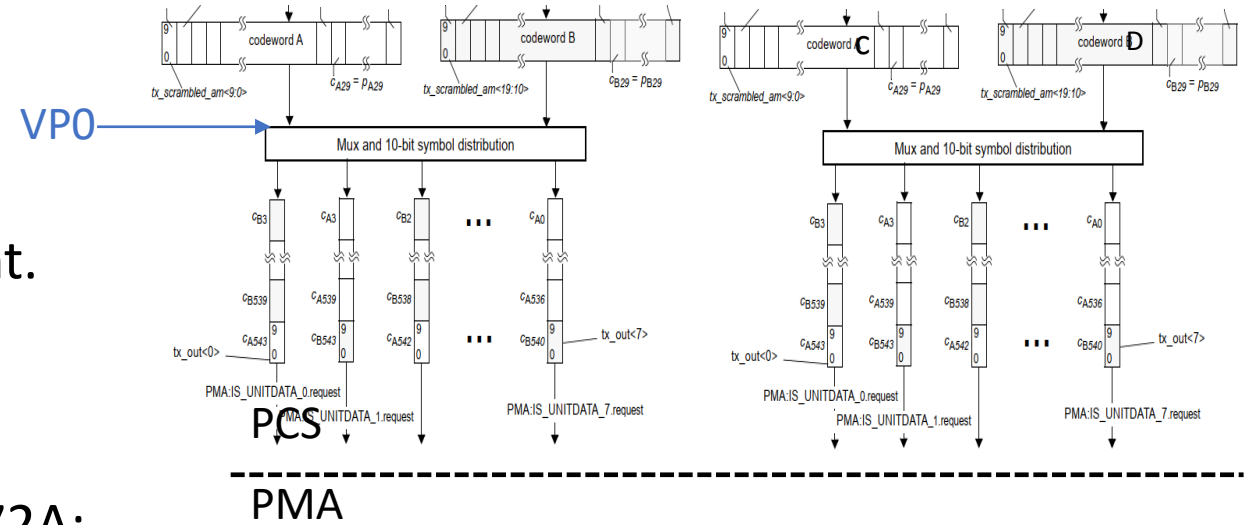
Vector points (200GE/400GE)

- Test vectors are given for test points on the right.
 - **VP1** and **VP3** are required for interoperability.
 - **VPO** and **VP2** are given as a reference for debug.
- VPO is identical to Annex 119A extended by 2 additional CWs.
- Assumptions are same as 802.3 Annex 119A:
 - First CW has AM block.
 - Constant transmission of Idle control characters.
 - Scrambler AM padding PRBS9 generator seed: $P_{\langle 0:8 \rangle} = 0x100$.
 - AM block $tx_am_sf_{\langle 2:0 \rangle} = \{0, 0, 0\}$.
 - Scrambler seed $S_{\langle 0:57 \rangle} = 0x24E6959D0FA5DBD$
- 8:1 symbol-pair mux for PMA lane 'n' is done between PCS lanes $\{n*8, n*8+1, .., n*8+7\}$.



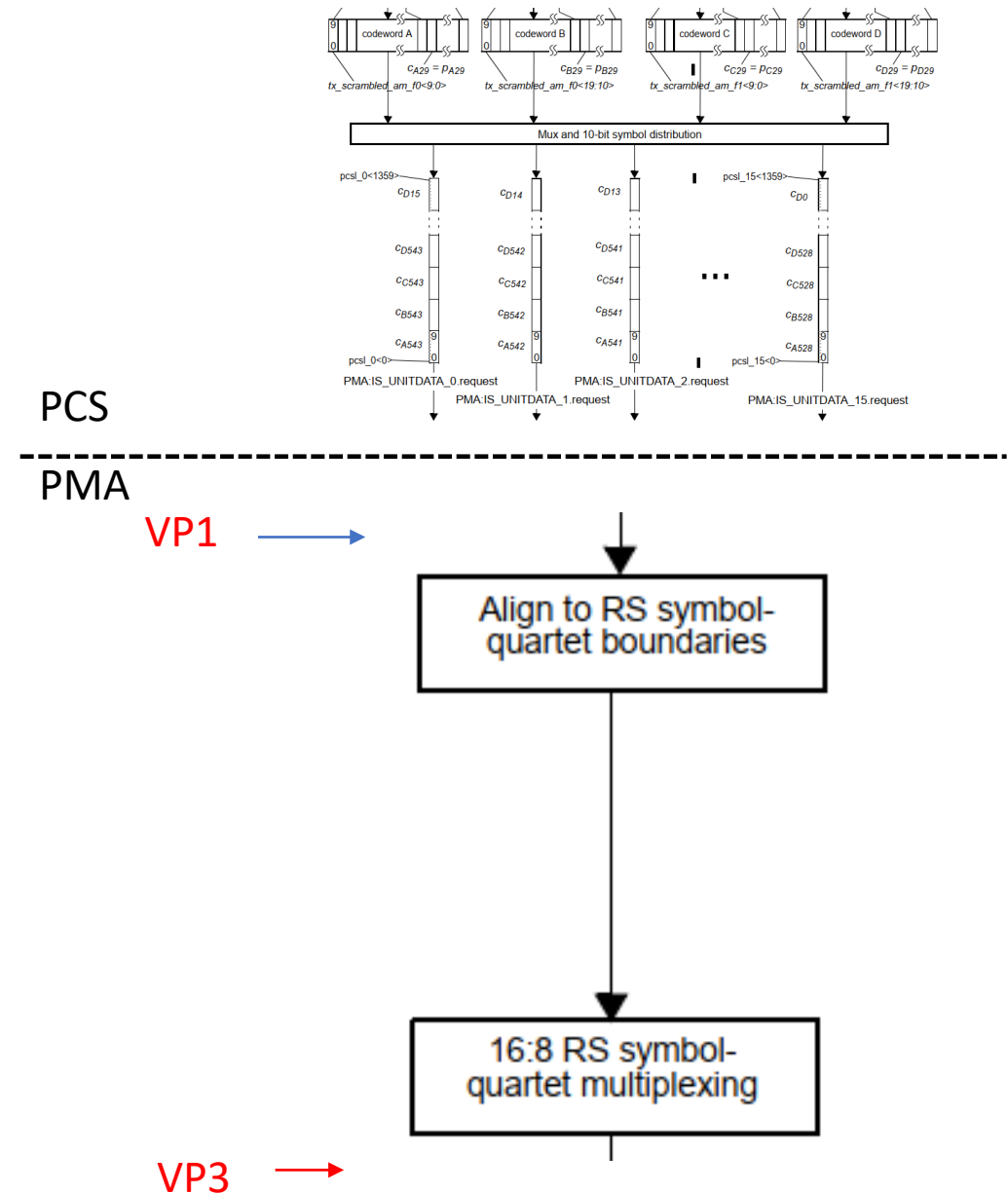
Vector points (800GE)

- Test vectors are given for test points on the right.
 - **VP1** and **VP3** are required for interoperability.
 - **VP0** and **VP2** are given as a reference for debug.
- **VP0** is identical to Annex 172A.
- **VP0** assumptions are same as 802.3df Annex 172A:
 - First CW has AM block.
 - Constant transmission of Idle control characters.
 - Scrambler AM padding PRBS9 generator seed: $P\langle 0:8 \rangle = 0x100$.
 - AM block $tx_am_sf\langle 2:0 \rangle = \{0, 0, 0\}$.
 - Flow 0 scrambler seed $S\langle 0:57 \rangle = 0x24E6959D0FA5DBD$
 - Flow 1 scrambler seed $S\langle 0:57 \rangle = 0x1FB58857D81624F$
- 8:1 symbol-pair mux for PMA lane 'n' is done between PCS lanes $\{n*4, n*4+16, n*4+1, n*4+16+1 \dots, n*4+3, n*4+16+3\}$.



Vector points (1.6TE)

- Test vectors are given for test points on the right.
 - **VP1** and **VP3** are required for interoperability.
 - VP1 relies on 802.3dj draft 1.0 Annex 175A.
 - VP2 is not required since there is no odd lanes delay for 1.6T.
- 2:1 symbol-quartet mux for PMA lane 'n' is done between PCS lanes {n*2, n*2+1}.



Test vector format

- For all VPs except VP0 transmission order inside a line is from left to right top to bottom.
- For VP0 bits ordering is same as in Annex119A. Inside a 10b symbol bits are transmitted from LSB to MSB, and 10b symbols are transmitted from left to right.
- VP0:**
 - Same as defined in Annex 119A (hex stream with 320 bits / 80 hex per line)
 - Separate files for codeword A and codeword B (2 codewords per file, 34 lines)

1st symbol

```

1 A6A9AA6A9A64992649921486284BD26519565D946D5B56D5B57D936ED8B6CF7EFA842EDE6024F1DB
2 63156BC9A159A5EDB273FD0CCBB63B810BD2EA92401C8F6204458108BF4D44C2D1675209D8331CC8
  
```

2nd symbol

- VP1-2:**
 - Text file per PMA output lane.
 - Each line is 80 bits, binary form, belongs to each input PCS lane.
 - X is used for don't care, caused by adding delay on odd lanes.

Port	input lane 0	input lane 1	input lane 2	input lane 3	input lane 4	input lane 5	input lane 6	input lane 7	
200GE	PMA lane 0	PCS lane 0	PCS lane 1	PCS lane 2	PCS lane 3	PCS lane 4	PCS lane 5	PCS lane 6	PCS lane 7
400GE	PMA lane 0	PCS lane 0	PCS lane 1	PCS lane 2	PCS lane 3	PCS lane 4	PCS lane 5	PCS lane 6	PCS lane 7
	PMA lane 1	PCS lane 8	PCS lane 9	PCS lane 10	PCS lane 11	PCS lane 12	PCS lane 13	PCS lane 14	PCS lane 15
800GE	PMA lane 0	PCS_lane0	PCS_lane16	PCS_lane1	PCS_lane17	PCS_lane2	PCS_lane18	PCS_lane3	PCS_lane19
	PMA lane 1	PCS_lane4	PCS_lane20	PCS_lane5	PCS_lane21	PCS_lane6	PCS_lane22	PCS_lane7	PCS_lane23
	PMA lane 2	PCS_lane8	PCS_lane24	PCS_lane9	PCS_lane25	PCS_lane10	PCS_lane26	PCS_lane11	PCS_lane27
	PMA lane 3	PCS_lane12	PCS_lane28	PCS_lane13	PCS_lane29	PCS_lane14	PCS_lane30	PCS_lane15	PCS_lane31
1.6TE	PMA lane 0	PCS lane 0	PCS lane 1						
	PMA lane 1	PCS lane 2	PCS lane 3						
	PMA lane 2	PCS lane 4	PCS lane 5						
	PMA lane 3	PCS lane 6	PCS lane 7						
	PMA lane 4	PCS lane 8	PCS lane 9						
	PMA lane 5	PCS lane 10	PCS lane 11						
	PMA lane 6	PCS lane 12	PCS lane 13						
	PMA lane 7	PCS lane 14	PCS lane 15						

first

```

1 01011001010100100110010010100000101001101010110110011011011010111100110100000011 Input lane 0
2 01011001010100100110010000100000101001101010110110011011110011001011010011110111 Input lane 1
3 0101100101010010011001000110001010100110101011011001101101111101111100110011111 Input lane 2
4 01011001010100100110010001011010101001101010110110011011001000010110000100000001
5 01011001010100100110010010000111101001101010110110011011100110000101010010001010
6 01011001010100100110010001001111101001101010110110011011011100100100100011110010
7 01011001010100100110010010111100101001101010110110011011011101110100001000111001
8 0101100101010010011001000100010101001101010110110011011010011000110101101101110 Input lane 7
9 0011000110010100001100101111110011001110000000010111011100011001000100101000110 Input lane 0
10 0111111000011001101001011000010010000010001000110011010001011000001001110010000
  
```

last

Test vector format

- **VP3**
 - Text file per PMA lane
 - Each line is 160 bits
 - X is used for don't care, caused by adding delay on odd lanes.

```
1 01011001010100100110xxxxxxxxxxxxxxxxxxxx01011001010100100110xxxxxxxxxxxxxxxxxxxx01011001010100100110xxxxxxxxxxxxxxxxxxxx01011001010100100110xxxxxxxxxxxxxxxxxxxx
2 01001010000010100110xxxxxxxxxxxxxxxxxxxx01000110001010100110xxxxxxxxxxxxxxxxxxxx01001000011110100110xxxxxxxxxxxxxxxxxxxx01001011110010100110xxxxxxxxxxxxxxxxxxxx
3 10101101100110110110xxxxxxxxxxxxxxxxxxxx1010110110011011011xxxxxxxxxxxxxxxxxxxx10101101100110111001xxxxxxxxxxxxxxxxxxxx1010110110011011011xxxxxxxxxxxxxxxxxxxx
4 10111100110100000011xxxxxxxxxxxxxxxxxxxx1110111110011001111xxxxxxxxxxxxxxxxxxxx10000101010010001010xxxxxxxxxxxxxxxxxxxx01110100001000111001xxxxxxxxxxxxxxxxxxxx
```

Test vectors folder content

The test vectors is divided into 4 folders, each contains files as listed below.

- 200GBASE-R 8:1
 - vp0_cws_[a..b].txt
 - vp1_lane0.txt
 - vp2_lane0.txt
 - vp3_lane0.txt
- 400GBASE-R 16:2
 - vp0_cws_[a..b].txt
 - vp1_lane[0..1].txt
 - vp2_lane[0..1].txt
 - vp3_lane[0..1].txt
- 800GBASE-R 32:4
 - vp0_cws_[a..d].txt
 - vp1_lane[0..3].txt
 - vp2_lane[0..3].txt
 - vp3_lane[0..3].txt
- 1.6TBASE-R 16:8
 - vp1_lane[0..7].txt
 - vp3_lane[0..7].txt

Summary

- 200G per lane PMA (CL176) interoperability test vectors are proposed.
- Proposed test vectors:

https://www.ieee802.org/3/dj/public/24_05/loewenthal_3dj_02_2405