

# 802.3dj D1.0 Comment Resolution Logic Track

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# Introduction

- This slide package was assembled by the 802.3dj editorial team to provide background and detailed resolutions to aid in comment resolution.

# Clause 177, Inner FEC Sync Comment # 505

| Cl 177   | SC 177.6  | P 262                  | L 5      | # 505                 |
|--|-----------|------------------------|----------|-----------------------|
| Ren, Hao   |           | Huawei                 |          |                       |
| <i>Comment Type</i>  | <b>TR</b> | <i>Comment Status</i>  | <b>D</b> | <i>Inner FEC Sync</i> |
| In Figure 177—8, the input variable of state FS_LOCK_INIT is not correct. It would cause a FS lock error.  |           |                        |          |                       |
| <i>Suggested Remedy</i>  |           |                        |          |                       |
| FS_LOCK_INIT state should be entered after all the 8 flows obtain their inner FEC codeword boundaries and inner FEC flow 0 is identified, when fs_lock is false.   |           |                        |          |                       |
| Propose change:<br>Change the input variable from '!all_synced' to 'all_synced * !fs_lock'.  |           |                        |          |                       |
| Change the definition of all_synced<br>from<br>'A Boolean variable that is set to true when sync_flow<x> is true for all eight flows and is set to false when sync_flow<x> is false for any x.'<br>to<br>'A Boolean variable that is set to true when inner FEC flow 0 is identified and is set to false when sync_flow<x> is false for any x.'<br>(in page 258 line 48-50)                              |           |                        |          |                       |
| <i>Proposed Response</i>   |           | <i>Response Status</i> | <b>W</b> |                       |
| PROPOSED ACCEPT IN PRINCIPLE.  |           |                        |          |                       |
| Change the condition for FS_LOCK_INIT state from "!all_synced" to "all_synced*!fs_lock"  |           |                        |          |                       |
| Change the definition of variable "all_synced" from:<br>"A Boolean variable that is set to true when sync_flow<x> is true for all eight flows and is set to false when sync_flow<x> is false for any x."<br>to:<br>" A Boolean variable that is set to true when sync_flow<x> is true for all eight flows AND inner FEC flow 0 is identified, and is set to false when sync_flow<x> is false for any x." |           |                        |          |                       |

# Clause 177, Inner FEC Sync Comment # 505

Change the definition of variable “all\_synced” in 177.6.2.1 as follows:

all\_synced

A Boolean variable that is set to true when sync\_flow<x> is true for all eight flows AND inner FEC flow 0 is identified, and is set to false when sync\_flow<x> is false for any x.

Change Figure 177-8 as follows:

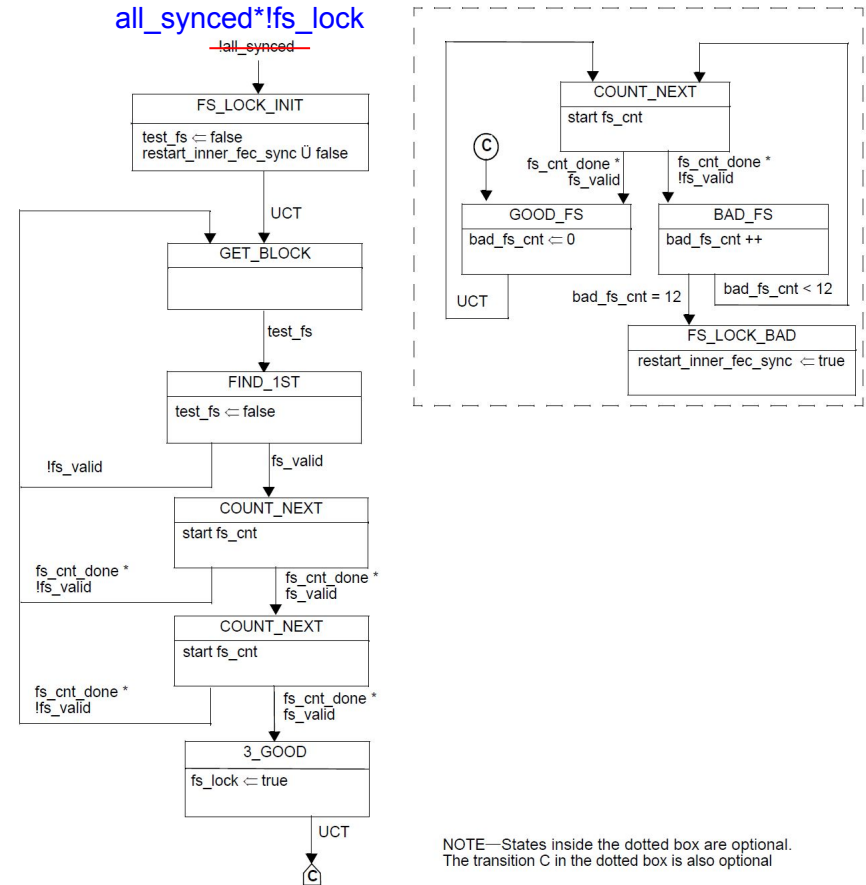


Figure 177-8—Inner FEC pad detection state diagram

# Clause 73, Priority Table Comment #149

## 802.3-2022

Table 73–5—Priority Resolution

| Priority | Technology                   | Capability                              |
|----------|------------------------------|---|
| 1        | 200GBASE-KR4 or 200GBASE-CR4 | 200 Gb/s 4 lane <b>highest priority</b> |
| 2        | 100GBASE-KR2 or 100GBASE-CR2 | 100 Gb/s 2 lane                         |
| 3        | 100GBASE-CR4                 | 100 Gb/s 4 lane                         |
| 4        | 100GBASE-KR4                 | 100 Gb/s 4 lane                         |
| 5        | 100GBASE-KP4                 | 100 Gb/s 4 lane                         |
| 6        | 100GBASE-CR10                | 100 Gb/s 10 lane                        |
| 7        | 50GBASE-KR or 50GBASE-CR     | 50 Gb/s 1 lane                          |
| 8        | 40GBASE-CR4                  | 40 Gb/s 4 lane                          |
| 9        | 40GBASE-KR4                  | 40 Gb/s 4 lane                          |
| 10       | 25GBASE-KR or 25GBASE-CR     | 25 Gb/s 1 lane                          |
| 11       | 25GBASE-KR-S or 25GBASE-CR-S | 25 Gb/s 1 lane, short reach             |
| 12       | 10GBASE-KR                   | 10 Gb/s 1 lane                          |
| 13       | 10GBASE-KX4                  | 10 Gb/s 4 lane                          |
| 14       | 5GBASE-KR                    | 5 Gb/s 1 lane                           |
| 15       | 2.5GBASE-KX                  | 2.5 Gb/s 1 lane                         |
| 16       | 1000BASE-KX                  | 1 Gb/s 1 lane, lowest priority          |

## 802.3df-2024

(includes additions from 802.3ck)

Table 73–5—Priority Resolution

| Technology                   | Capability                              |
|------------------------------|---|
| 800GBASE-KR8 or 800GBASE-CR8 | 800 Gb/s 8 lane <b>highest priority</b> |
| 400GBASE-KR4 or 400GBASE-CR4 | 400 Gb/s 4 lane                         |
| 200GBASE-KR2 or 200GBASE-CR2 | 200 Gb/s 2 lane                         |
| 200GBASE-KR4 or 200GBASE-CR4 | 200 Gb/s 4 lane                         |
| 100GBASE-KR1 or 100GBASE-CR1 | 100 Gb/s 1 lane                         |
| 100GBASE-KR2 or 100GBASE-CR2 | 100 Gb/s 2 lane                         |
| 100GBASE-CR4                 | 100 Gb/s 4 lane                         |
| 100GBASE-KR4                 | 100 Gb/s 4 lane                         |
| 100GBASE-KP4                 | 100 Gb/s 4 lane                         |
| 100GBASE-CR10                | 100 Gb/s 10 lane                        |
| 50GBASE-KR or 50GBASE-CR     | 50 Gb/s 1 lane                          |
| 40GBASE-CR4                  | 40 Gb/s 4 lane                          |
| 40GBASE-KR4                  | 40 Gb/s 4 lane                          |
| 25GBASE-KR or 25GBASE-CR     | 25 Gb/s 1 lane                          |
| 25GBASE-KR-S or 25GBASE-CR-S | 25 Gb/s 1 lane, short reach             |
| 10GBASE-KR                   | 10 Gb/s 1 lane                          |
| 10GBASE-KX4                  | 10 Gb/s 4 lane                          |
| 5GBASE-KR                    | 5 Gb/s 1 lane                           |
| 2.5GBASE-KX                  | 2.5 Gb/s 1 lane                         |
| 1000BASE-KX                  | 1 Gb/s 1 lane, lowest priority          |

# Clause 73, Priority Table

## Comment #149

### 802.3dj D1.0

Table 73–5—Priority Resolution

| Technology                          | Capability  |
|-------------------------------------|---|
| <u>1.6TBASE-KR8 or 1.6TBASE-CR8</u> | 1.6 Tb/s 8 lane <input type="text"/>                          |
| <u>800GBASE-KR4 or 800GBASE-CR4</u> | 800 Gb/s 4 lane   |
| <u>800GBASE-KR8 or 800GBASE-CR8</u> | 800 Gb/s 8 lane <input type="text" value="highest priority"/> |
| <u>400GBASE-KR2 or 400GBASE-CR2</u> | 400 Gb/s 2 lane   |
| <u>400GBASE-KR4 or 400GBASE-CR4</u> | 400 Gb/s 4 lane   |
| <u>200GBASE-KR1 or 200GBASE-CR1</u> | 200 Gb/s 1 lane   |
| <u>200GBASE-KR2 or 200GBASE-CR2</u> | 200 Gb/s 2 lane   |
| <u>200GBASE-KR4 or 200GBASE-CR4</u> | 200 Gb/s 4 lane   |
| <u>100GBASE-KR1 or 100GBASE-CR1</u> | 100 Gb/s 1 lane   |
| ...                                 |   |

Add “highest priority” here.

# Clause 177, State Diagram Conventions

## Comment #492

### 177.6 Detailed functions and state diagrams

#### 177.6.1 State diagram conventions

The body of this subclause is composed of state diagrams, including the associated definitions of variables, functions, and counters. Should there be a discrepancy between a state diagram and descriptive text, the state diagram prevails.

The notation used in the state diagrams follows the conventions of 1.2, along with the extensions listed in 21.5. The notation ++ after a counter or integer variable indicates that its value is to be incremented.

#### 177.6.2 State variables

##### 177.6.2.1 Variables

###### all\_synced

A Boolean variable that is set to true when sync\_flow<x> is true for all eight flows and is set to false when sync\_flow<x> is false for any x.

###### fs\_cnt\_done

Boolean variable that indicates that fs\_cnt has reached its terminal count.

#### 177.6.2.3 Counters

###### bad\_cw\_cnt

Counts the number of invalid Inner FEC codewords based on the output of CAL\_SYNDROME function. A codeword is considered invalid when its syndrome is non-zero.

###### bad\_fs\_cnt

Counts the number of consecutive FS that don't match the expected values.

###### cw\_cnt

Counts the number of Inner FEC codewords processed.

###### fs\_cnt

Counts the interval of Inner FEC codewords between two adjacent pads.

###### valid\_cw\_cnt

Counts the number of valid Inner FEC codewords based on the output of CAL\_SYNDROME function. A codeword is considered valid when its syndrome is zero.

# Clause 177, State Diagram Conventions

## Comment #492

### 21.5.3 State transitions

The following terms are valid transition qualifiers:

- a) Boolean expressions
- b) An event such as the expiration of a timer: `timer_done`
- c) An event such as the reception of a message: `PMA_UNITDATA.indication`
- d) An unconditional transition: `UCT`
- e) A branch taken when other exit conditions are not satisfied: `ELSE`

Any open arrow (an arrow with no source block) represents a global transition. Global transitions are evaluated continuously whenever any state is evaluating its exit conditions. When a global transition becomes true, it supersedes all other transitions, including `UCT`, returning control to the block pointed to by the open arrow.

### 73.10.2 State diagram timers

All timers operate in the manner described in 14.2.3.2.

#### `autoneg_wait_timer`

Timer for the amount of time to wait before evaluating the number of link integrity test functions with `link_status=OK` asserted. The `autoneg_wait_timer` shall expire 25 ms to 50 ms from the assertion of `link_status=OK` from the PCS.

#### `break_link_timer`

Timer for the amount of time to wait in order to assure that the link partner enters a Link Fail state. The timer shall expire 60 ms to 75 ms after being started.

#### `clock_detect_min_timer`

Timer for the minimum time between detection of differential Manchester clock transitions. The `clock_detect_min_timer` shall expire 4.8 ns to 6.2 ns after being started or restarted.

### 14.2.3.2 State diagram timers

All timers operate in the same fashion. A timer is reset and starts counting upon entering a state where “start\_x\_timer” is asserted. Time “x” after the timer has been started, “x\_timer\_done” is asserted and remains asserted until the timer is reset. At all other times, “x\_timer\_not\_done” is asserted.



# Clause 177, State Diagram Conventions

## Comment #492

### 91.5.4.2.1 Variables

`all_locked`

A Boolean variable that is set to true when `amps_lock<x>` is true for all `x` and is set to false when `amps_lock<x>` is false for any `x`.

`amp_counter_done`

Boolean variable that indicates that `amp_counter` has reached its terminal count.

`1st_ram_counter_done`

Boolean variable that indicates that `1st_ram_counter` has reached its terminal count.

`1st_ramps_counter_done`

Boolean variable that indicates that `1st_ramps_counter` has reached its terminal count.

`fec_lpi_fw`

Boolean variable that controls the behavior of the Transmit LPI and Receive LPI state diagrams. This variable is set to true when the local PCS is configured to use the fast wake mechanism and set to false otherwise.

`ram_counter_done`

Boolean variable that indicates that `ram_counter` has reached its terminal count.

...