

# 1.6Tbps output jitter decomposition associated with high loss AUI-C2M channel conditions

## Version 1.2

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**Based on draft release of IEEE 802.3dj™/D1.0/1.1/1.2**

**Abstract: Performing JNu operations near the limits of current channel profiles is a highly technical proposition, and may require some methodology revisions. This contribution will offer an overview of current state of the art jitter decomposition methods and offer some technical proposals designed to reduce the channel based jitter amplification impact on random jitter.**

## Supporters/Collaborators (Version 1.2)

**Mike Dudek (Marvell)**

**Luke Wang (Credo)**

**Mark Kimber (Semtech)**

**Adee Ran (Cisco)**

**Geoff Zhang (AMD)**

**Richard Mellitz (Samtec)**

## Reference:

Previous IEEE P802.3dj version 1.2. [https://www.ieee802.org/3/dj/public/24\\_05/calvin\\_3dj\\_01b\\_2405.pdf](https://www.ieee802.org/3/dj/public/24_05/calvin_3dj_01b_2405.pdf)

## Instrumentation used in this contribution

### M8042A/M8050A PG

- No Tx de-emphasis

### M8067A-005/003-Trace (1mm)

- 31.1dB @53.125GHz – (35mm + 185mm Traces )
- 2X pair of 1mm 8” phase matched cables (1.2dB each)
- Net TP1a test channel loss 33.5dB

### UXR 1104B Real-Time scope

- DSP/SW Clock Recovery
- ~SIRC: 60GHz 4<sup>th</sup> order Bessel Thomson rolling off to -9dB @ 90GHZ

### N1000A+N1046A Sampling scope

- Prototype Clock Recovery
- SIRC: 60GHz 4<sup>th</sup> order Butterworth

## Overview

The draft 1.0 P802.3dj comment resolution sessions have indicated interest in consolidating physical layer Jitter operations at C2M and CR interfaces.

The question of whether 12Edge Jitter operations can be accurately evaluated in a worst case AUI-C2M (33dB) configuration is the focus of this contribution.

Slew rate decreases by 2 when you cut bandwidth by a factor of 2. However, the noise only drops by  $\sqrt{2}$ . So the jitter due to noise increases by  $\sqrt{2}$

The operations demonstrated in this contribution focus on both Real-Time instrumentation (Keysight UXR 1104B), digital clock recovery (1<sup>st</sup> order 4MHz) and a 60GHz 4<sup>th</sup> order Bessel, as well as its Equivalent-Time counterpart (DCA N1046/N1071) with early experimental CDR capability.

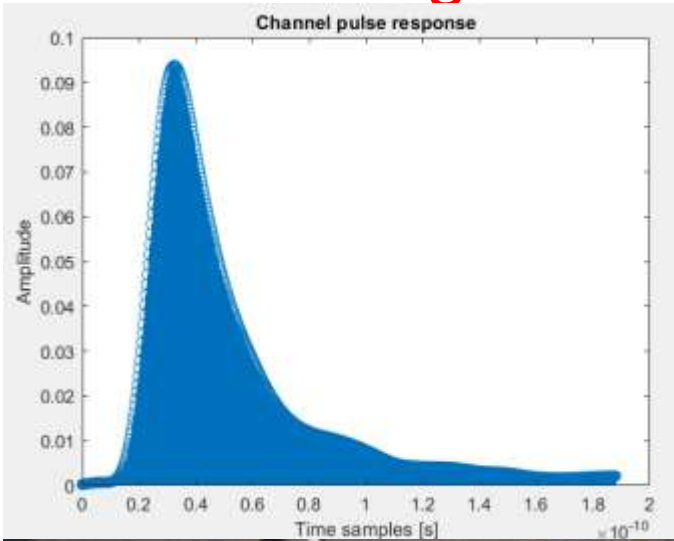
Signal generation in this contribution is with a Keysight M8042A PG transmitting a PRBS13Q test pattern, no TX EQ, with a single **ended amplitude** of 300mV at the source.



The signal path interconnect is all performed via 1mm interconnects.



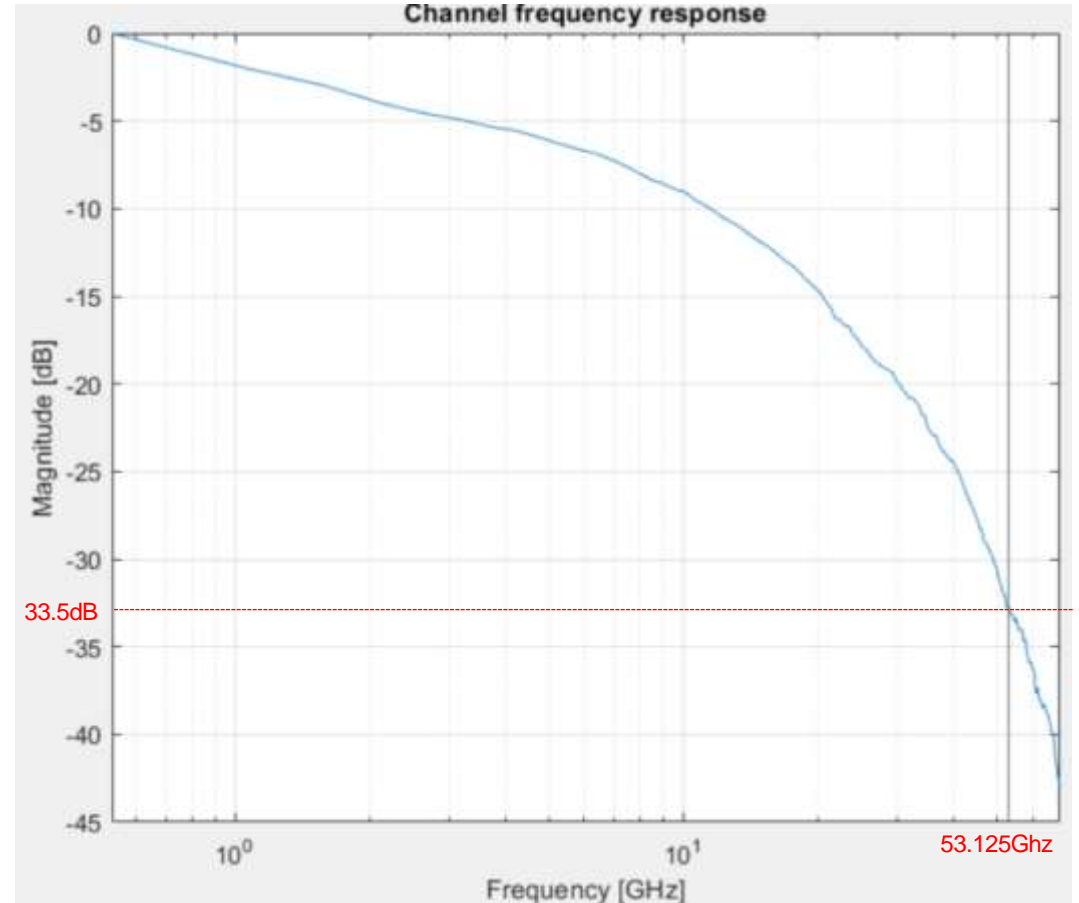
# Channel configuration and Real-Time instrument used in this study:

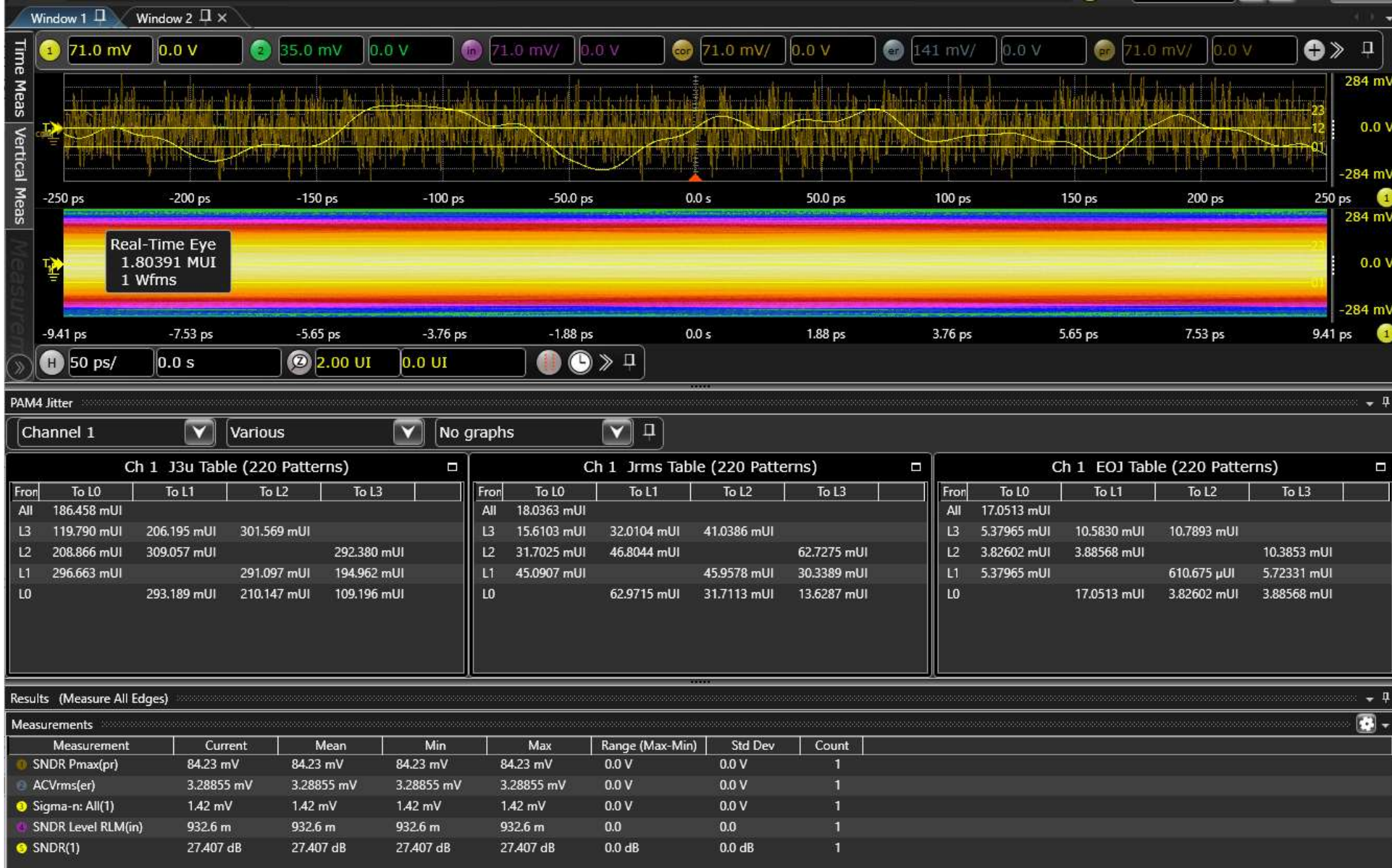


Closest attainable physical proxies for (35mm + 185mm) C2M/TP1a targeting (HL-HL)  $\sim 33$ dB

Reference : [https://www.ieee802.org/3/dj/public/23\\_11/lusted\\_3dj\\_04\\_2311.pdf](https://www.ieee802.org/3/dj/public/23_11/lusted_3dj_04_2311.pdf) pg 5

PR  $\rightarrow$  SR  $\rightarrow$  IR  $\rightarrow$  (FFT)  $\Rightarrow$





# Output jitter (max) analysis

Draft Amendment to IEEE Std 802.3-2022  
IEEE P802.3dj 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force

IEEE Draft P802.3dj/D1.0  
10 April 2024

Table 179-7—Summary of transmitter specifications at TP2 (continued)

Parameter	Subclause reference	Value	Units
Transmitter steady-state voltage, $v_f$ (min)	179.9.4.1.2	TBD	V
Host designation Host-Low		TBD	V
Host designation Host-Nominal		TBD	V
Host designation Host-High		TBD	V
Transmitter steady-state voltage, $v_f$ (max)	179.9.4.1.2	0.6	V
Linear fit pulse peak ratio, $R_{peak}$ (min)	179.9.4.1.2	TBD	—
Host designation Host-Low		TBD	—
Host designation Host-Nominal		TBD	—
Host designation Host-High		TBD	—
Level separation mismatch ratio $R_{LM}$ (min)	179.9.4.2	0.95	—
Transmitter output waveform			
absolute value of step size for all taps (min)	179.9.4.1.4	0.005	—
absolute value of step size for all taps (max)	179.9.4.1.4	0.025	—
value at minimum state for $c(-3)$ (max)	179.9.4.1.5	-0.06	—
value at maximum state for $c(-2)$ (min)	179.9.4.1.5	0.12	—
value at minimum state for $c(-1)$ (max)	179.9.4.1.5	-0.34	—
value at minimum state for $c(0)$ (max)	179.9.4.1.5	0.5	—
value at minimum state for $c(1)$ (max)	179.9.4.1.5	-0.2	—
Signal-to-noise-and-distortion ratio, SNDR (min)	179.9.4.6	31.5	dB
Signal-to-residual-intersymbol-interference ratio, $SNR_{ISI}$ (min)	179.9.4.3	26.7	dB
Output jitter (max)	179.9.4.7	TBD	UI

1  
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From	To L0	To L1	To L2	To L3
All	186.458 mUI			
L3	119.790 mUI	206.195 mUI	301.569 mUI	
L2	208.866 mUI	309.057 mUI		292.380 mUI
L1	296.663 mUI		291.097 mUI	194.962 mUI
L0		293.189 mUI	210.147 mUI	109.196 mUI

J3U<sub>03</sub> is formed from a composite of targeted L3->0 and L0->3 uncorrelated edge jitter. The composite result has some questions but the the individual values are solid.

Similarly EOJ<sub>03</sub> is formed from a composite of targeted L3->0 and L0->3 Even/Odd jitter elements. The composite value here is WIP, but the individual L3->0 and L0->3 values are correct.

Draft Amendment to IEEE Std 802.3-2022  
IEEE P802.3dj 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force

IEEE Draft P802.3dj/D1.1  
11 July 2024

Table 176E-1—Summary of host output specifications at TP1a (continued)

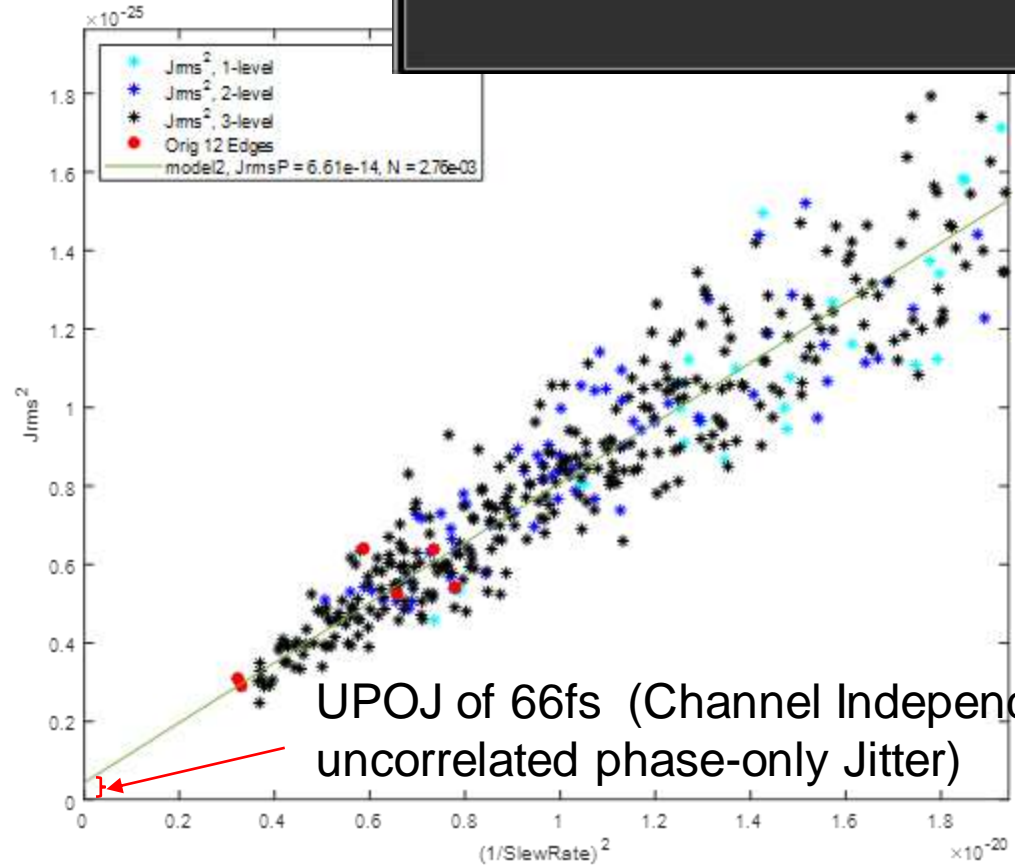
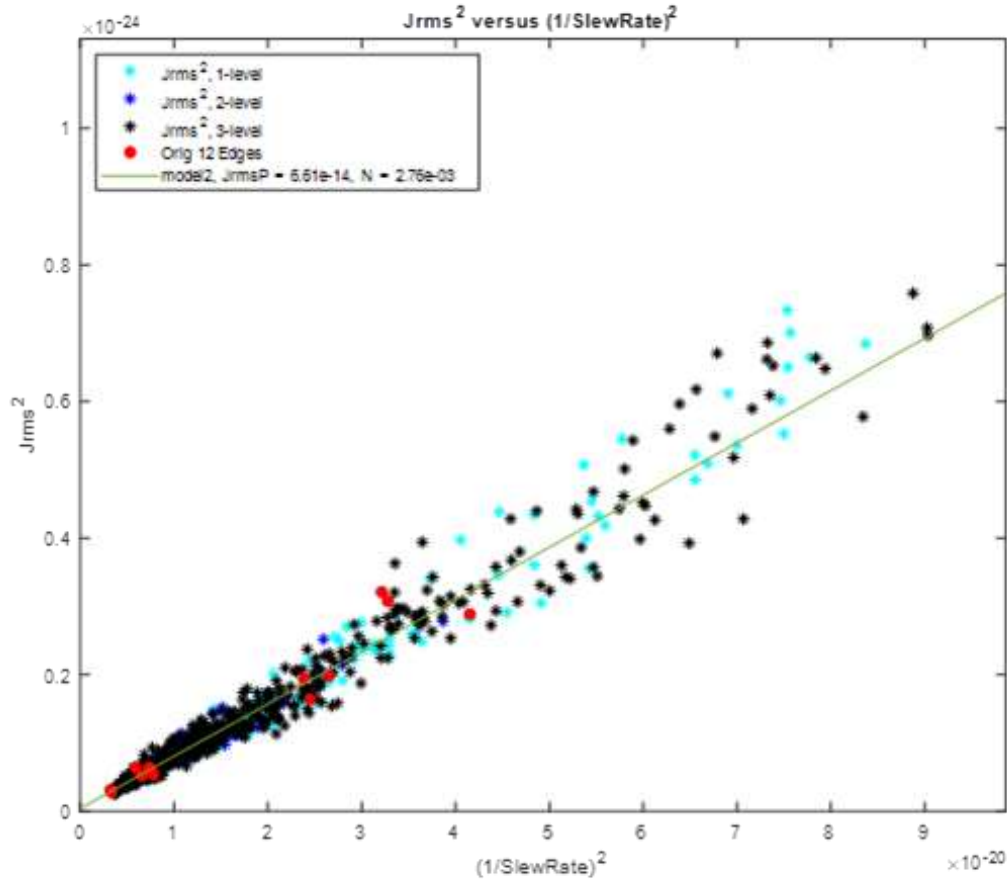
Output jitter (max)	176E.6.9		
J <sub>RMS03</sub>		0.023	UI
EOJ <sub>03</sub>		0.025	UI
J4u <sub>03</sub>		0.135	UI

From	To L0	To L1	To L2	To L3
All	17.0513 mUI			
L3	5.37965 mUI	10.5830 mUI	10.7893 mUI	
L2	3.82602 mUI	3.88568 mUI		10.3853 mUI
L1	5.37965 mUI		610.675 μUI	5.72331 mUI
L0		17.0513 mUI	3.82602 mUI	3.88568 mUI

# Output jitter (max) $J_{RMS_{03}}$ analysis

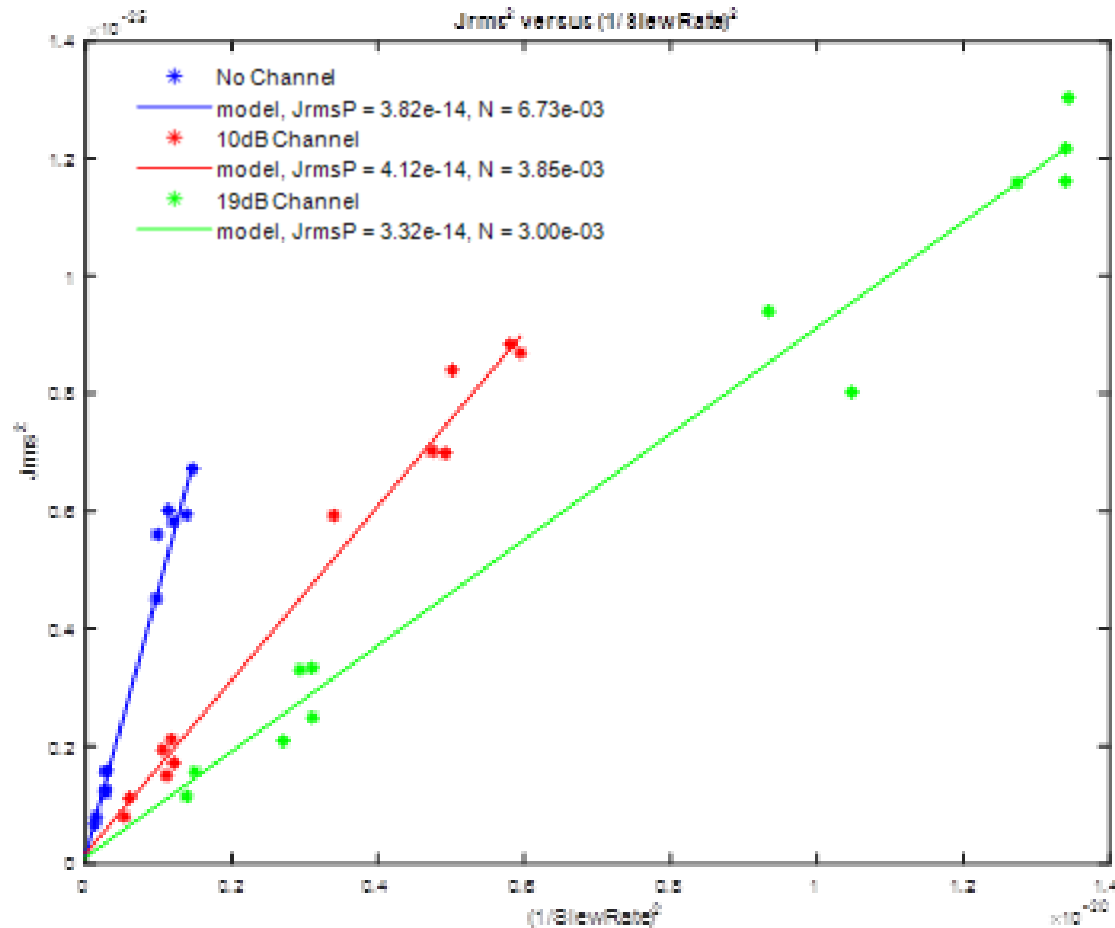
Comments from the May 2024 Interim session recommended a method of refining our  $J_{RMS_{03}}$  to reduce the impact of channel induced random noise amplification (UPOJ: Uncorrelated Phase-only Jitter)

From	To L0	To L1	To L2	To L3
All	18.0363 mUI			
L3	15.6103 mUI	32.0104 mUI	41.0386 mUI	
L2	31.7025 mUI	46.8044 mUI		62.7275 mUI
L1	45.0907 mUI		45.9578 mUI	30.3389 mUI
L0		62.9715 mUI	31.7113 mUI	13.6287 mUI





# UPOJ: Uncorrelated Phase-only Jitter

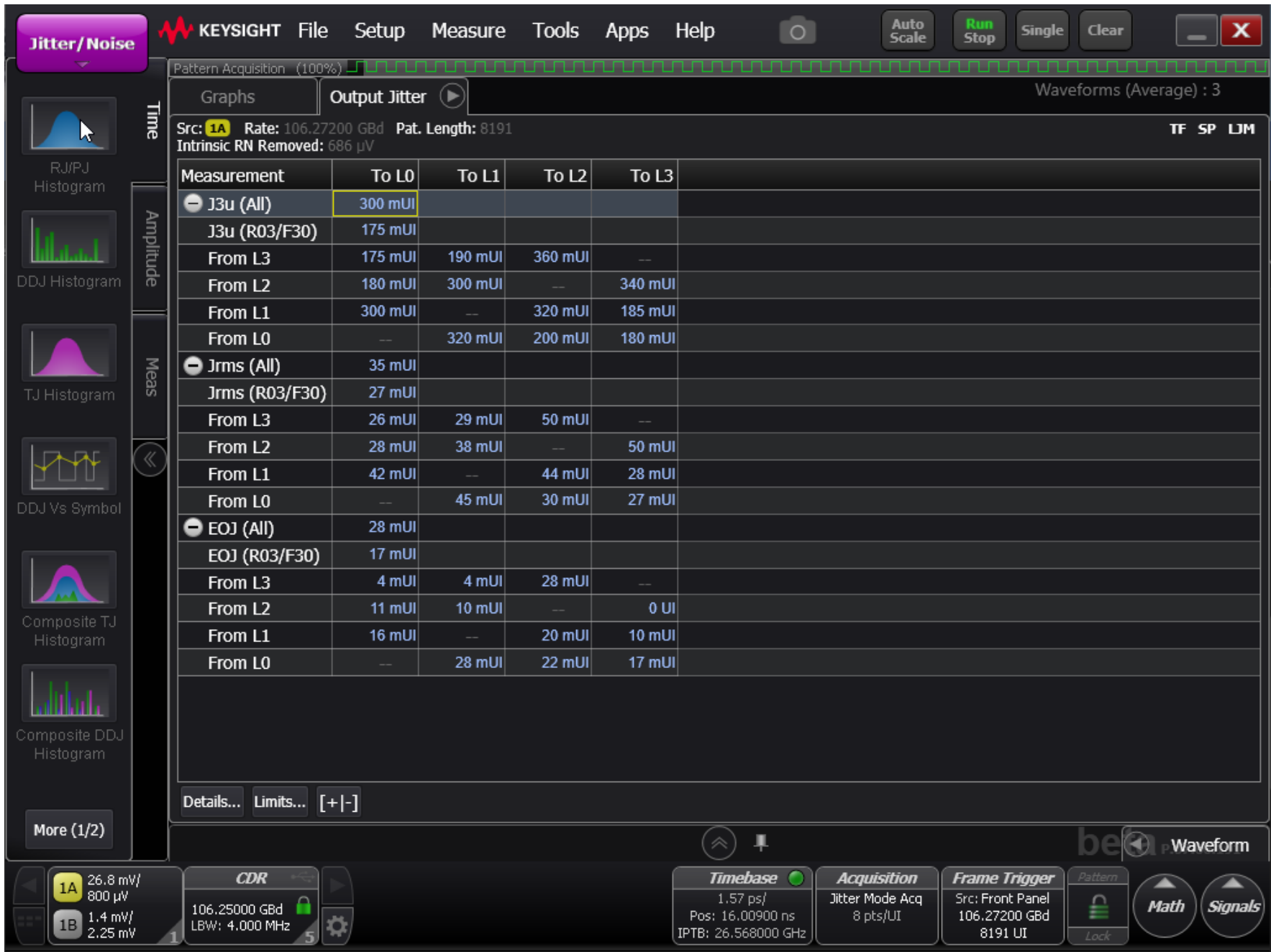


The uncorrelated phase only jitter (UPOJ), when extrapolated back to the y-intercept (via linear regression), observes relatively stable UPOJ values ranging from 38fs, 41fs to 33fs. This process clearly benefits from more statistical sample points (previous slide), but nicely converges to a reasonable UPOJ number which appears to be channel independent.

## Channel configuration and Equivalent-Time (ET) instrument used in this study:

- Physical Clock Recovery (CR) with early experimental systems are complex at TP1a (106GBd at 33.5dB), but reliable at TP2 (24dB).
- Driven with a 600mV Differential Tx signal.
- Low return loss channel (-15dB max)
- Phase Detector sensitivity in the CR is operating at it's design limits.





# J3u comparison at 33dB

- This is two separate systems Real-Time (RT) and Equivalent-Time (ET) with the same model of generator and same model of ISI structures.
- “today” We are seeing similar jitter decomposition at 33dB on RT and ET based instrumentation.
- J3u03 on ET of 175mUI –vs- 186mUI on RT is typical variance.

Measurement	To L0	To L1	To L2	To L3
⊖ J3u (All)	300 mUI			
J3u (R03/F30)	175 mUI			
From L3	175 mUI	190 mUI	360 mUI	—
From L2	180 mUI	300 mUI	—	340 mUI
From L1	300 mUI	—	320 mUI	185 mUI
From L0	—	320 mUI	200 mUI	180 mUI
⊖ Jrms (All)	35 mUI			
Jrms (R03/F30)	27 mUI			
From L3	26 mUI	29 mUI	50 mUI	—
From L2	28 mUI	38 mUI	—	50 mUI
From L1	42 mUI	—	44 mUI	28 mUI
From L0	—	45 mUI	30 mUI	27 mUI
⊖ EOJ (All)	28 mUI			
EOJ (R03/F30)	17 mUI			
From L3	4 mUI	4 mUI	28 mUI	—
From L2	11 mUI	10 mUI	—	0 UI
From L1	16 mUI	—	20 mUI	10 mUI
From L0	—	28 mUI	22 mUI	17 mUI

From	To L0	To L1	To L2	To L3
All	186.458 mUI			
L3	119.790 mUI	206.195 mUI	301.569 mUI	
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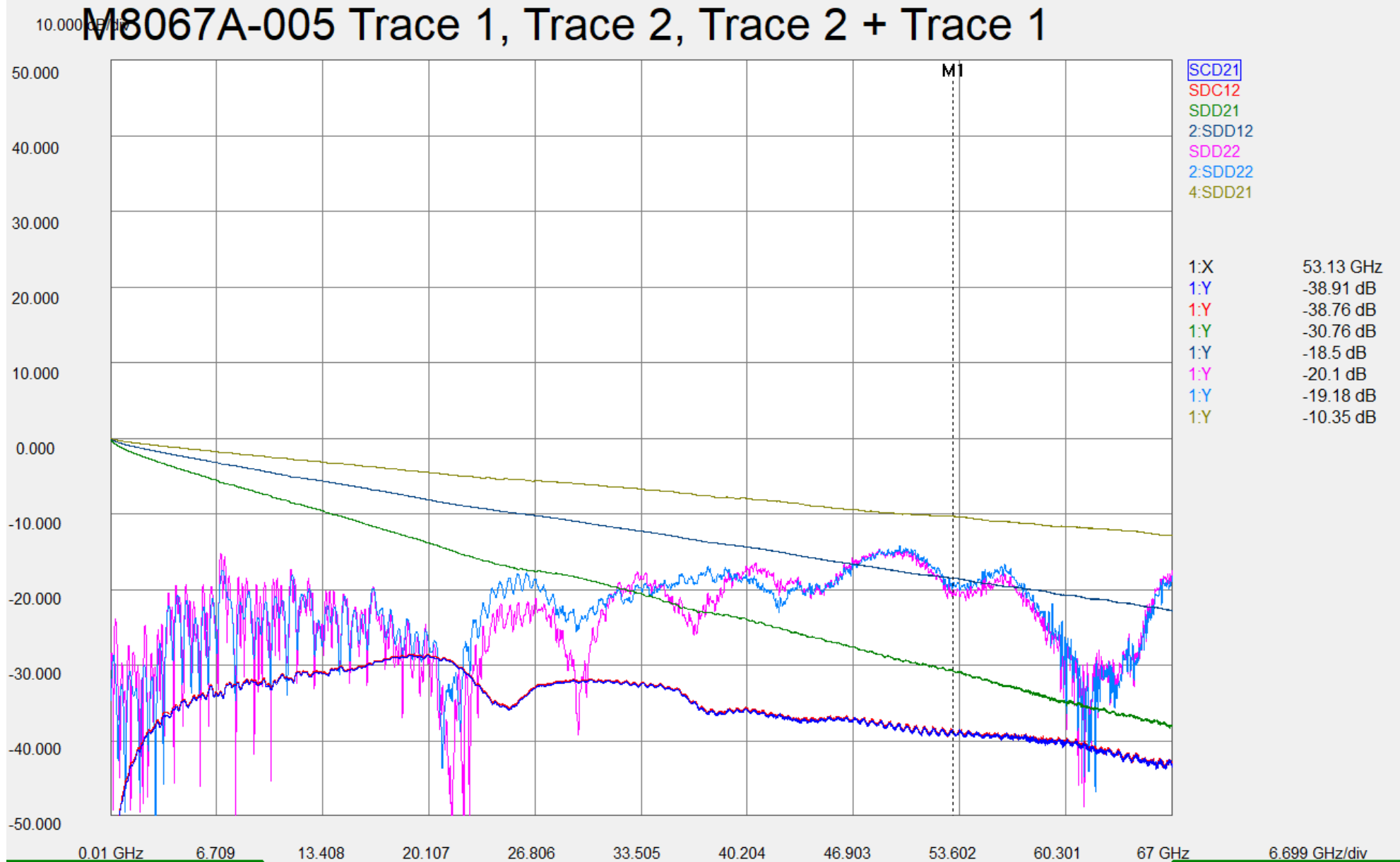
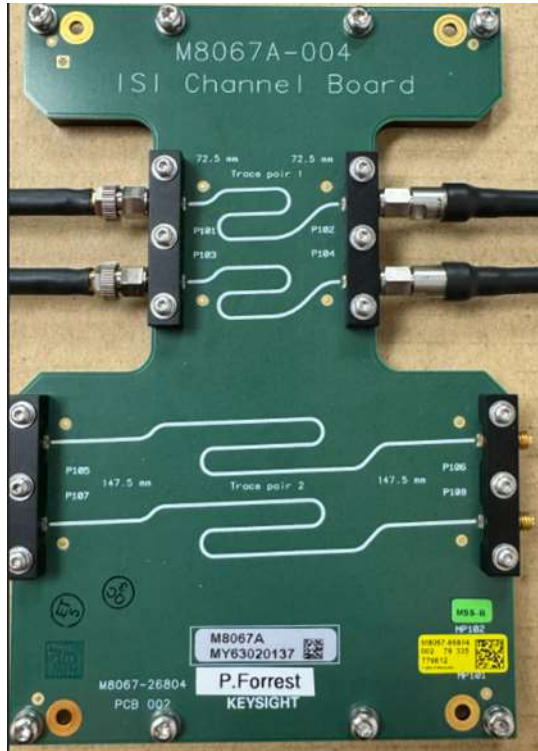
## Summary

- With an un-equalized 600mV differential signal launch through a 33.5dB signal path representing a worst case TP1a condition, observing proper 1<sup>st</sup> order 4MHz CDR and 60GHz 4BT Reference Receiver with no TX EQ, Jitter (Clause 162.9.4.7) can effectively be performed.
- Delicate noise management efforts are needed to reduce/remove the channel amplification effects on random noise originating in transmitters.
- Single level and two level transitions (defined in Clause 162.9.4.7) suffer from SNR losses after 33dB, and are marginally useful. The three level transitions are easily extracted however and extraction of  $J_{3u_{03}}$ ,  $J_{RMS_{03}}$  and  $E_{OJ_{03}}$  are all viable validation methods using evolutionary steps from prior Clause 179 and 162.9.4.7 methods.
- Steps to isolate true DUT phase jitter by eliminating the vertical noise contribution from the jitter are demonstrated here and offer an accurate (albeit sensitive) method of determining  $J_{RMS}$ -“uncorrelated phase only jitter (UPOJ)” behavior. This needs additional effort to refine and to extend to the  $J_{3u}$  operations.

Thank you

# Backup

- M8067A-005 ISI trace Performance



# Backup “Support of 178.9.2 Transmitter characteristics”

Draft Amendment to IEEE Std 802.3-2022  
IEEE P802.3dj 200 Gb/s, 400 Gb/s, 800 Gb/s, and 1.6 Tb/s Ethernet Task Force

IEEE Draft P802.3dj/D1.1  
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Unless otherwise specified, transmitter signal measurements are made for each lane separately using a fourth-order Bessel-Thomson low-pass response with a 3 dB bandwidth of 60 GHz, with AC-coupled connection from TP0v to the test equipment.

- Tx: 300 mV SE amplitude. 106.25GHz clock recovery. PRBS13Q (IEEE/PRBS13Q\_Lane0\_bit). 4PAM Gray coded. No de-emphasis. No impairments.
- Channel: 35 mm ISI board (approx.. 6.5 dB channel loss at 53 GHz counting cables).
- Real-Time instrumentation test case.

Test case	VEC [dB]	J3u all [mUI]	Jrms all [mUI]
No BW limit (113 GHz brick)	7.79	153	18.3
70 GHz brick	6.94	160.6	17.4
60 GHz Butter. 75 GHz brick	6.06	137.8	15.4
60 GHz Bessel. 90 GHz brick	5.67	125.2	15.2