KEYSIGHT

1.6Tbps Vertical Eye Closure associated with high loss AUI-C2M channel conditions Version 1.0

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Based on draft release of IEEE 802.3dj™/D1.x

Abstract: Performing VEC operations near the limits of current channel profiles requires precision EQ tuning and noise management. This contribution will offer an overview of VEC post COM 4.6b2 MMSE tuning and contrast the incremental values of MLSE under these high loss conditions.

Supporters/Collaborators (Version 1.0)

Reference:

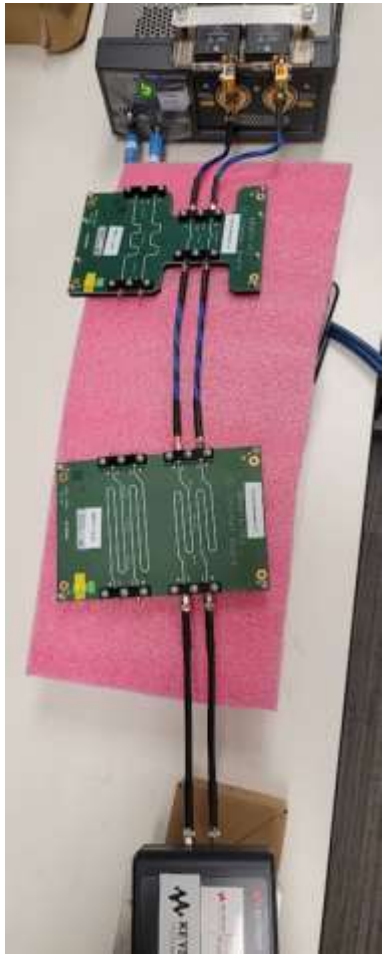
Previous IEEE P802.3dj version 1.2. https://www.ieee802.org/3/dj/public/24_05/calvin_3dj_01b_2405.pdf

Instrumentation used in this contribution

- M8042A/M8050A PG
  - No Tx de-emphasis 300mV SE/ 600mV Diff
- M8067A-005/003-Trace (1mm)
  - 31.1dB @53.125GHz – (35mm + 185mm Traces)
  - 2X pair of 1mm 8” phase matched cables (1.2dB each)
  - Net TP1a test channel loss 33.5dB
- UXR 1104B Real-Time scope
  - DSP/SW Clock Recovery
  - ~SIRC: 60GHz 4th order Bessel Thomson rolling off to -9dB @ 90GHZ
- N1000A+N1046A Sampling scope
  - Prototype Clock Recovery
  - SIRC: 60GHz 4th order Butterworth
- COM Version: com_ieee8023_93a_460beta2
  - TDMODE (PR imported from instruments, spreadsheet in supporting material)

Overview

The draft 1.1 P802.3dj specifications omits familiar Vertical Eye Closure (VEC) operations. Many have asked whether VEC can be computed under aggressive C2M channel configurations at 33dB of loss. This presentation is a collection of experiments and observations related to this question.

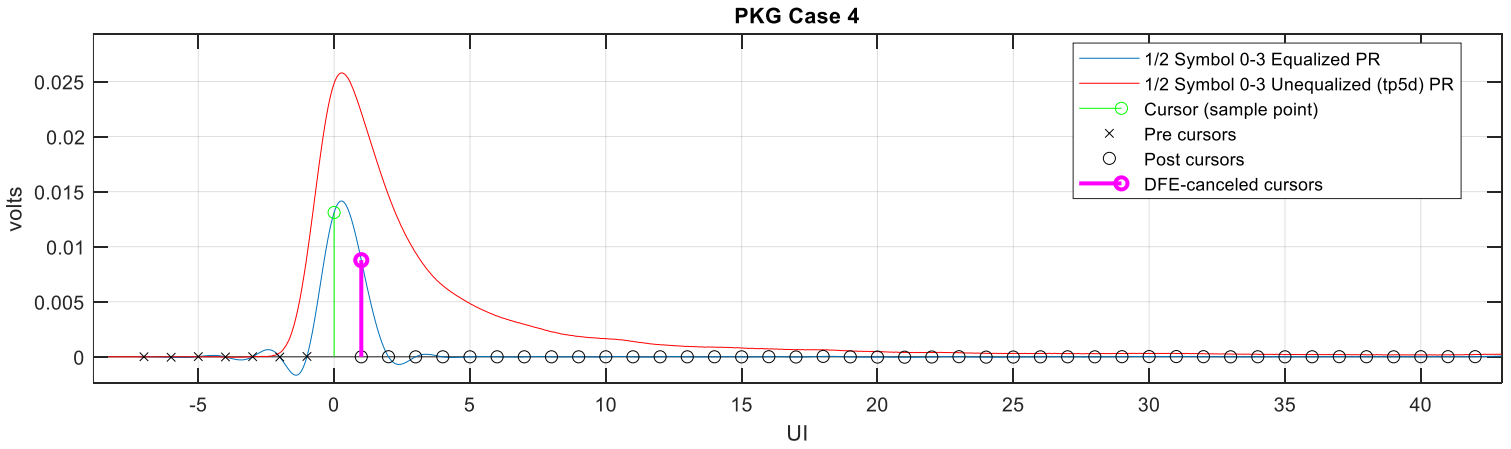


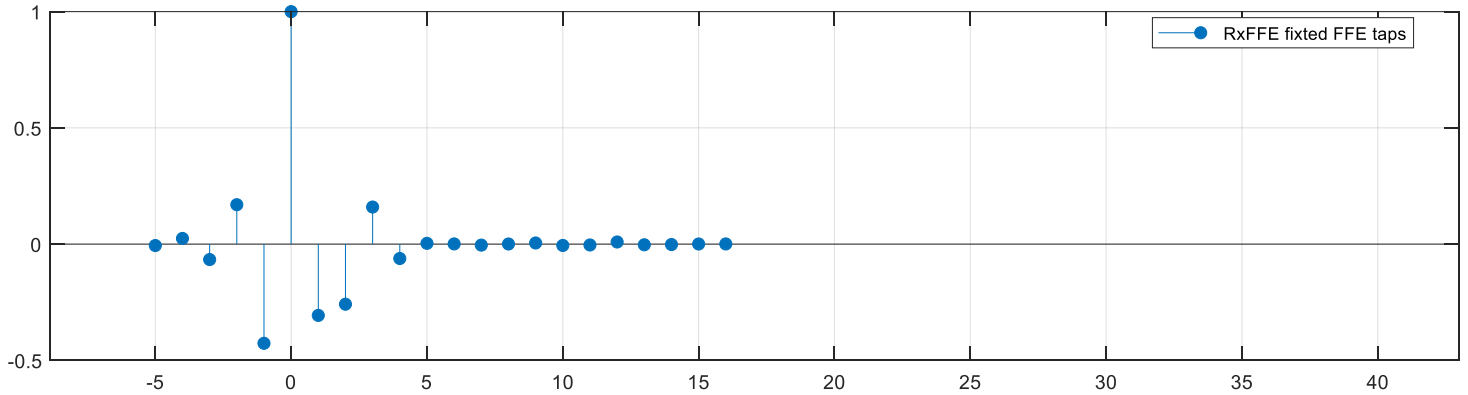
The operations demonstrated in this contribution focus on both Real-Time instrumentation (Keysight UXR 1104B), digital clock recovery (1'st order 4MHz) and a 60GHz 4'th order Bessel Thomson (4BT) response with brickwall at 90GHZ. This configuration operates with an approximate ENOB of 5.2 dB at this bandwidth.

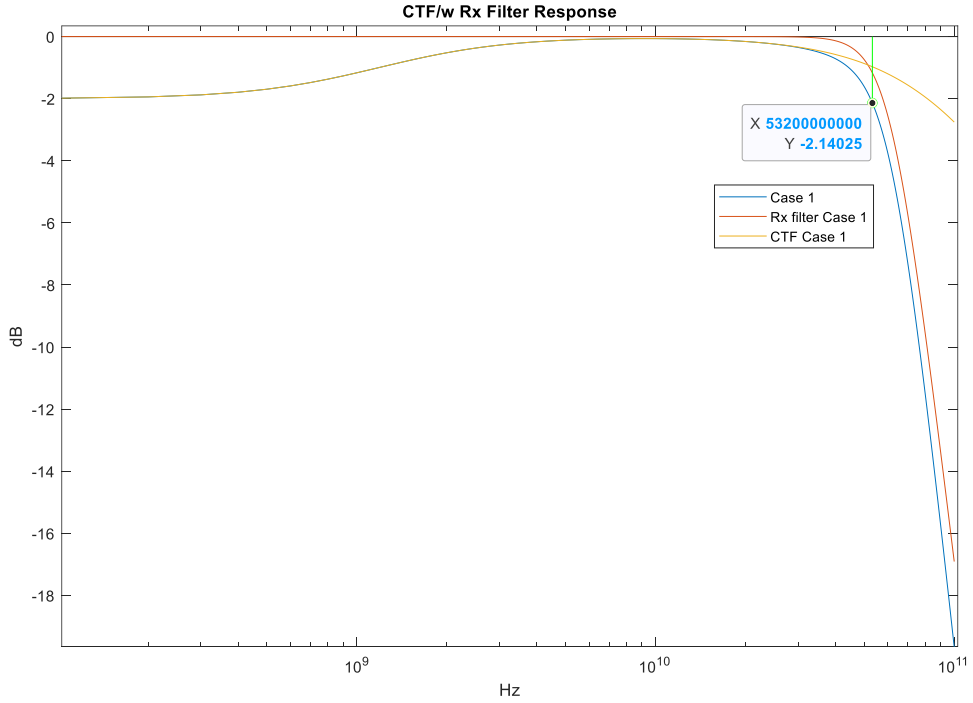
The Equivalent-Time counterpart (DCA N1046/N1071AETA) with early release CDR capability. This configuration applies a precision phase and magnitude controlled reference receiver also with a 4BT bandwidth of 60GHz. The comparable ENOB of this system on nominally 7dB.

Signal generation in this contribution is with a Keysight M8042A PG transmitting a PRBS13Q test pattern, no TX EQ, with a single **ended amplitude** of 300mV at the source.

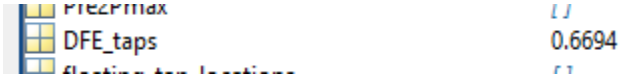
Com Results 220mm (Source Synchronous/Explicit Clock) 33dB





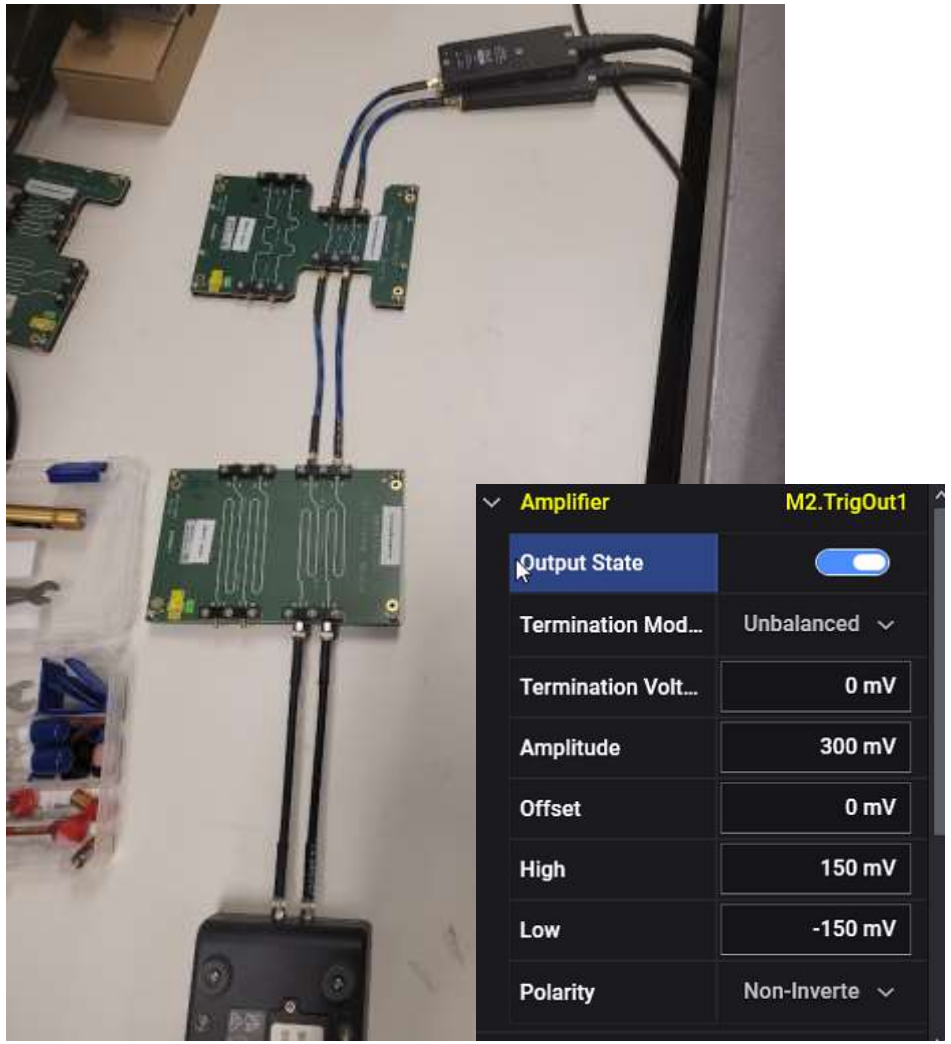


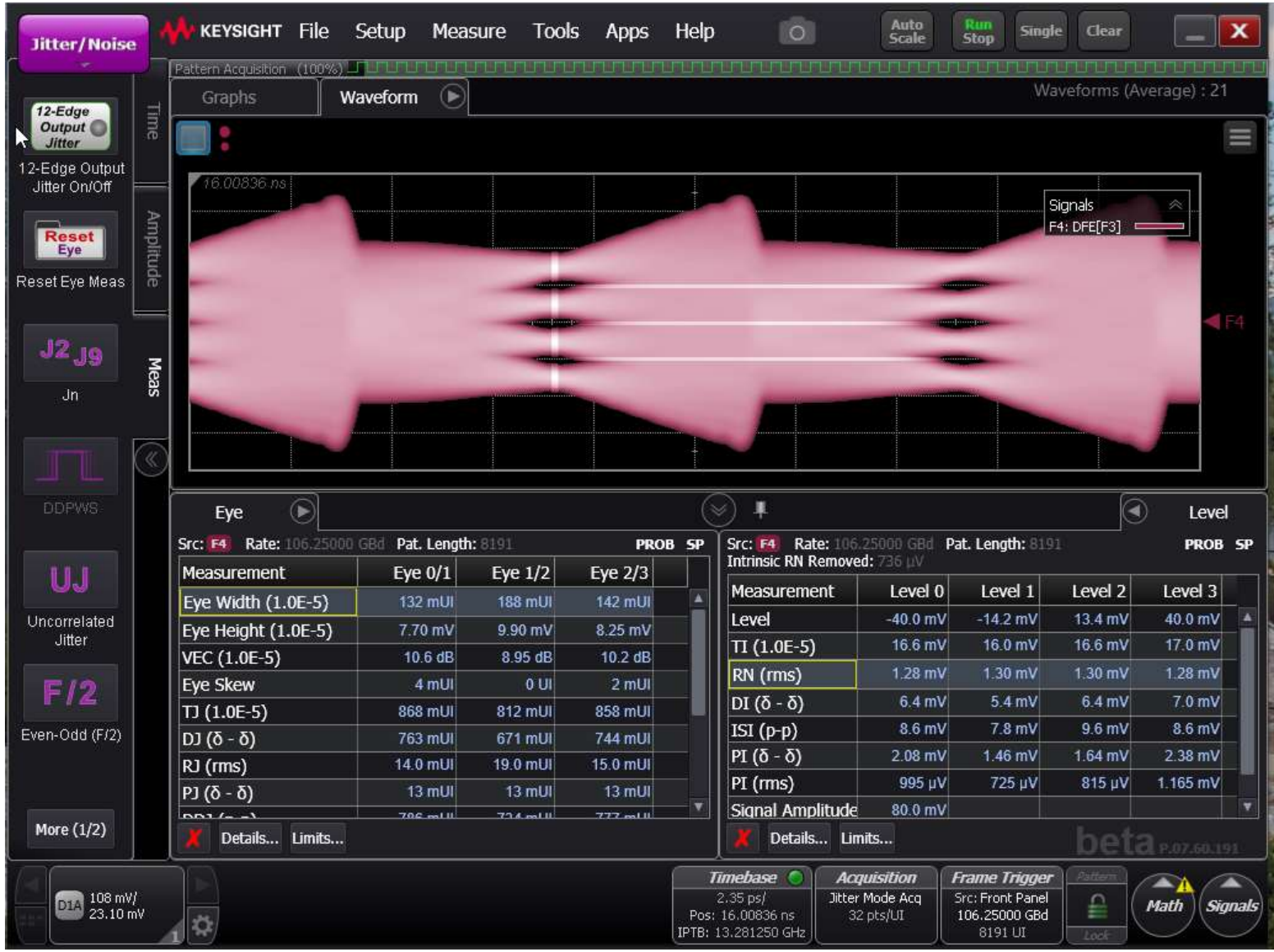
CTLE(0,-2)
RXFFE shown above
DFE (0.67 com, … dca)



Equivalent-Time 33dB VEC, source synchronous clocked (not spec'd)

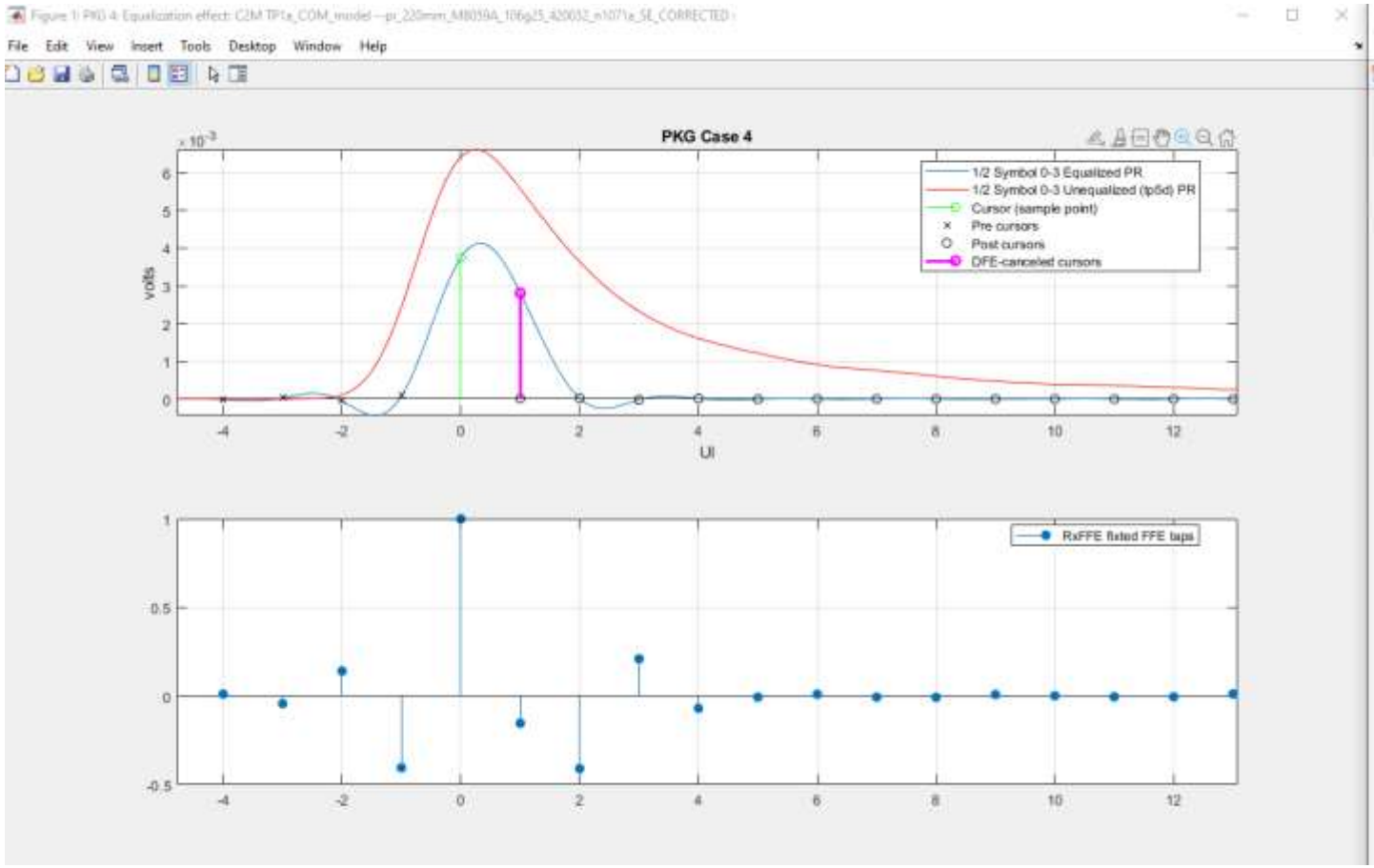
(35mm + 185mm) mm case [33dB]

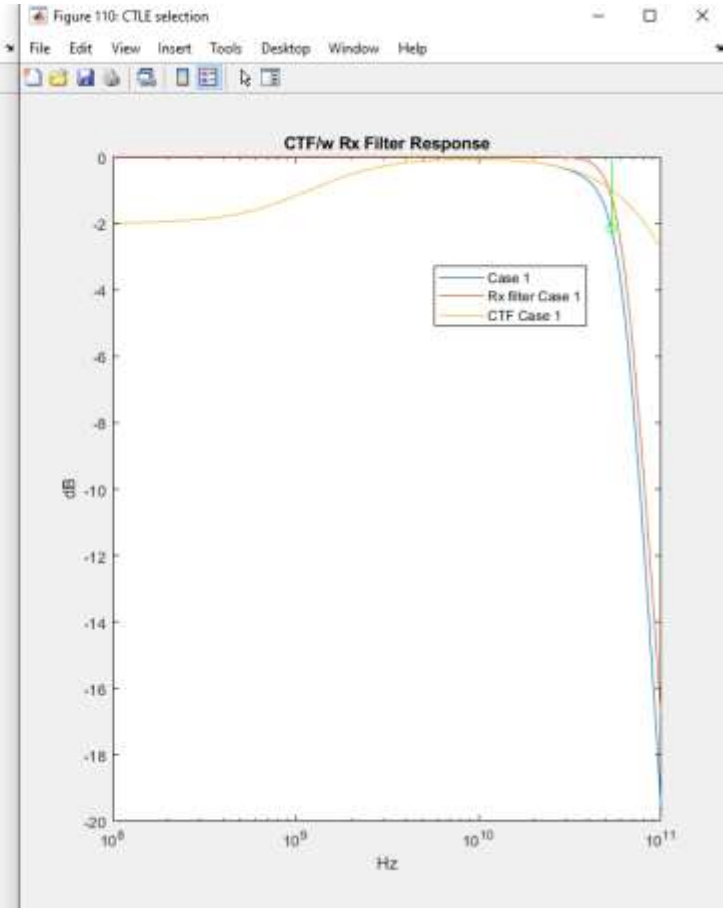




PRBS13Q, no TXEQ, 220mm trace M8067A-00

Com Results 220mm (Recovered Clock) 33dB





Pre2Pmax	[ ]	
DFE_taps	0.7500	

Pulse response taps, normalized by main cursor amplitude (10.4mV):

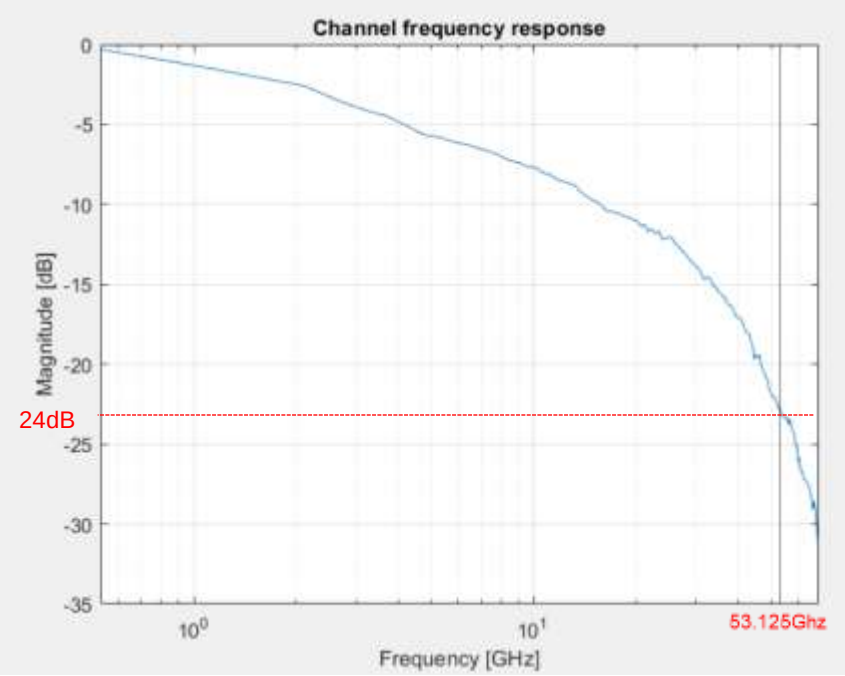
0.661452

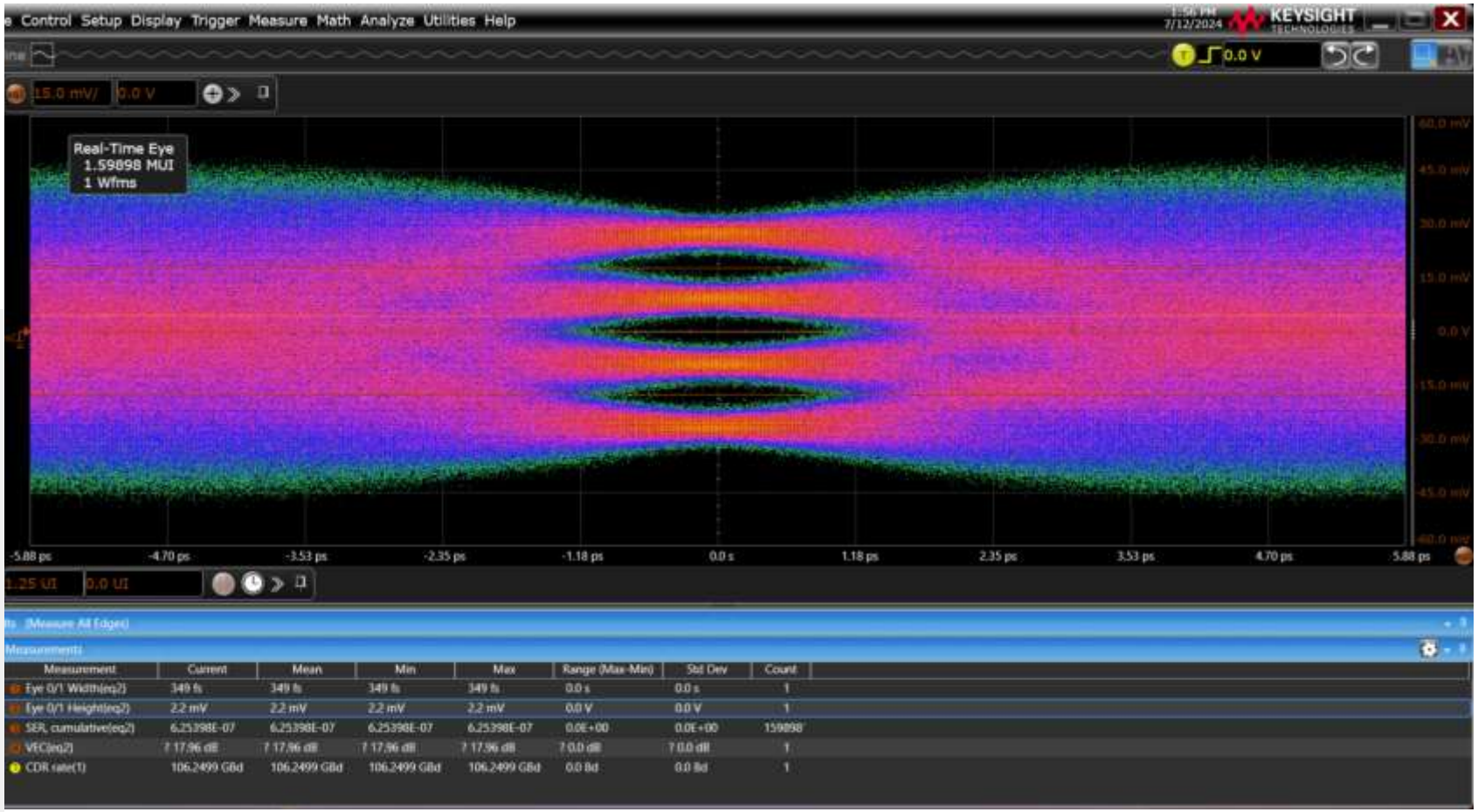
VEC Results 220mm 31dB using N1071AETA Early Technology CDR unit

- The N1071AETA CDR unit needs additional investigation, and a follow-up contribution will be needed to fully determine this CDR's sensitivity limits. The 33dB is compounded by an additional 20/80 signal distribution network that is leaving very little energy for the phase detector to lock.

Real-Time 24dB VEC

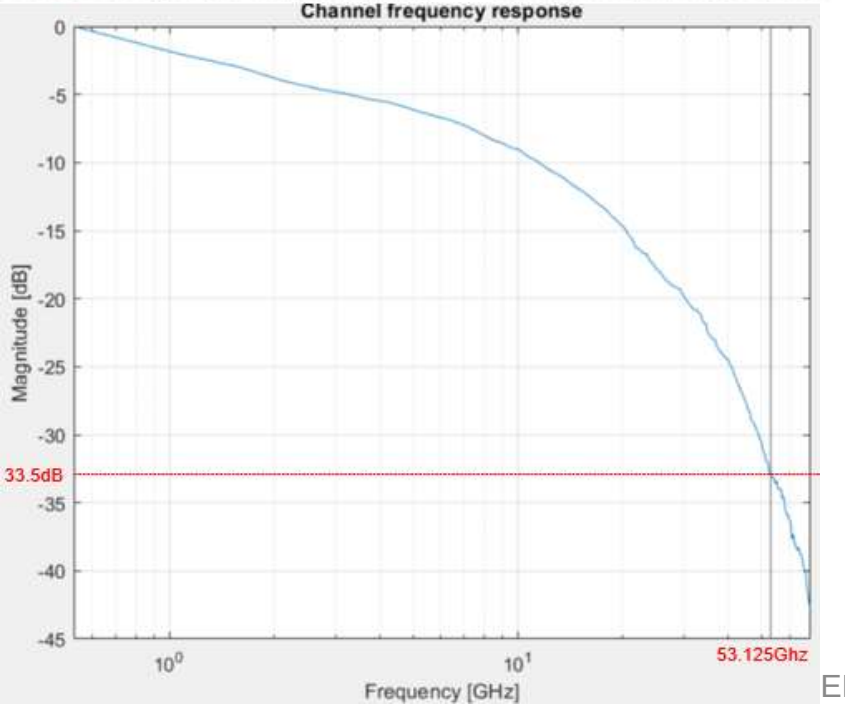
```
VEC_COM =

    7.0328


VEC_MLSE =

    7.0437


dVEC =

   -0.0109

 Die to die loss =  dB
run time = 0.404101 min
WC All cases  PASS ... VEC = 7.044 dB
WC All cases  PASS ... EH = 8.104 mV
WC All cases  PASS ... COM = 5.105 dB
WC All cases DER = 2.794e-08 at COM threshold
 redo string is: eval(['My_var_0 = ' getappdata(0,'cmd_str')])
```

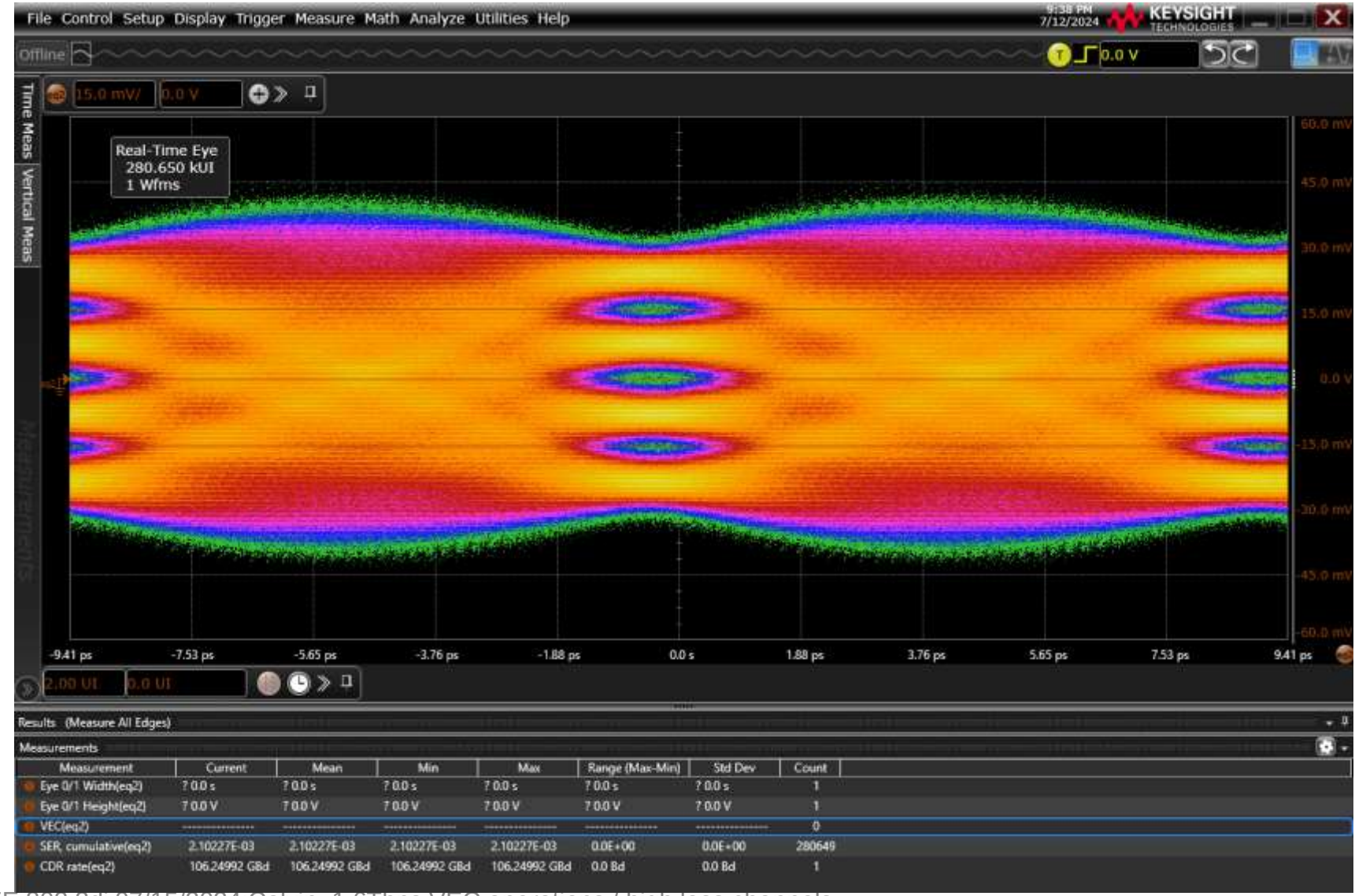




Real-Time 33dB VEC

```
VEC_COM =

    8.7541

VEC_MLSE =

    7.9876

dVEC =

    0.7665

 Die to die loss =  dB
run time = 0.396597 min
WC All cases  PASS ... VEC = 7.988 dB
WC All cases  PASS ... EH = 6.673 mV
WC All cases  PASS ... COM = 4.418 dB
WC All cases DER = 9.992e-07 at COM threshold
 redo string is: eval(['My_var_0 = ' getappdata(0,'cmd_str')])
```





Summary

- 600mV differential signal launch through a 33.5dB signal path representing a worst case TP1a condition. This contribution shows Clock Recovery operations on both Equivalent Time(ET) and Real Time(RT) architectures here.
- Low initial signal levels (600mV) and 33.5dB of channel loss constitutes a very challenging setting to do high precision COM and VEC operations.
- The only experiment that could be deemed a success here is the 33dB explicit clocking configuration which did showcase passing COM and VEC results and close simulation to physical layer correlation.
- N1071AETA Early Technology CDR operating at the end of a 33dB channel, will be examined and possibly a modified signal path split will be required. (50/50 rather than 20/80) for high sensitivity applications.
- Real-Time instrumentation was not successful with VEC at 33dB either. Efforts to perform better noise management are needed to improve the SNR at these losses. Part of this may be attributed to instrument ETA_Zero challenges as well as lower ENOB compared to the ET configuration.

Thank you

Backup

- M8067A-005 ISI trace Performance